SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

LOW POWER LOW VOLTAGE MODEM ANALOG FRONT-END STLC7550

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CONTENTS

I - OVERVIEW

STLC7550 is a single chip analog-front-end (AFE) designed to implement modems up to 56Kbps.

It has been designed for host processing application in which the modulation software (V.34, 56Kbps) is performed by the main application processor : Pentium, Risc or DSP as well as PC Modem with DSP.

The main target of this device is stand alone applications as Hand-Held PC (HPC), Personal Digital Assistants (PDA), Webphones, Network Computer, Set Top Boxes for Digital Television (Satellite and cable).

To comply with such applications STLC7550 is powered nominally at 3V. 30mW maximum power dissipation is well suited for battery operations. In case of battery low, STLC7550 will continue to work even at a 2.7V level.

STLC7550 provides clock generator for all sampling frequencies requested for V.34bis and 56Kbps applications.

This AFE can also be used for PC mother boards or add-ons cards or stand alone Modems. It is compatible with previous STLC7546 designs and can be powered at 5V.

II - COMPATIBILITY WITH STLC7546

STLC7550 has been designed to be compatible with STLC7546 application.

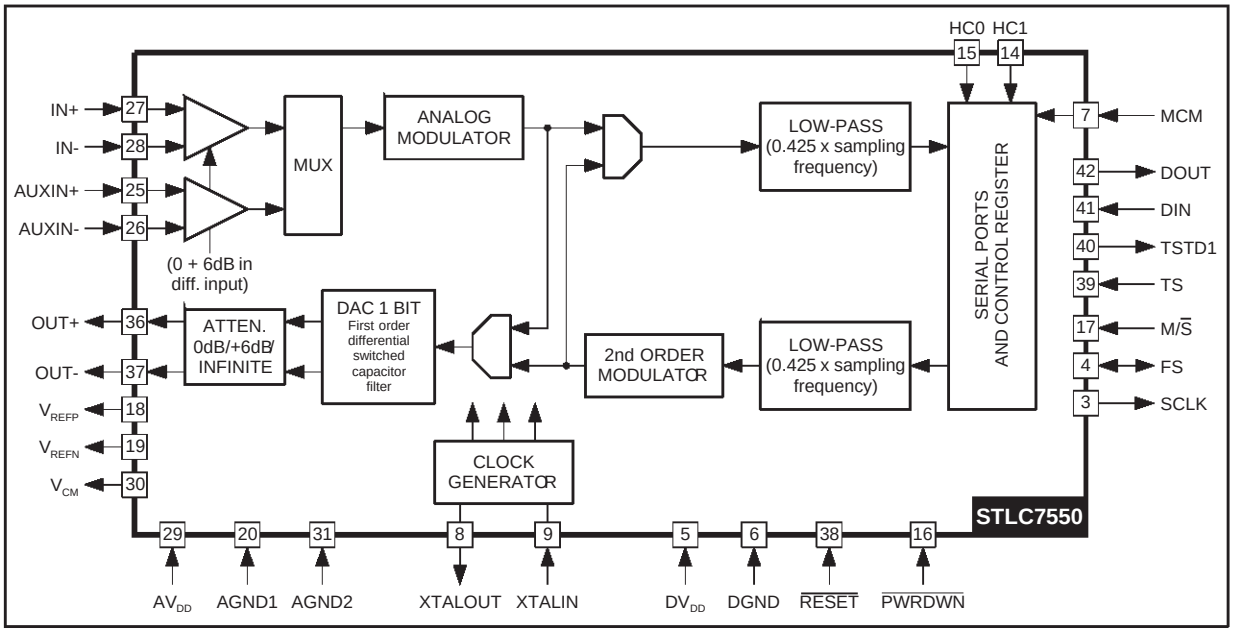
Additional features in STLC7550 are described hereafter.

- a master/slave mode to allow a dual codec structure,
- an integrated programmable frequency generator that makes STLC7550 codec able to generate all V.34bis and 56Kbps sampling frequencies. (see Chapter III - Clock Generator),
- an on-chip crystal oscillator,
- a low power consumption of 30mW @ 3V. STLC7550 has been targeted for 3V application, however it has a power supply range of 2.7 to 5.5 that allows it to work also in previous 5V (or 3V) STLC7546 designs,
- Stand-by mode power consumption less than 3µW @3V.

Figure 2 gives the implementation of STLC7550 as a STLC7546 codec.

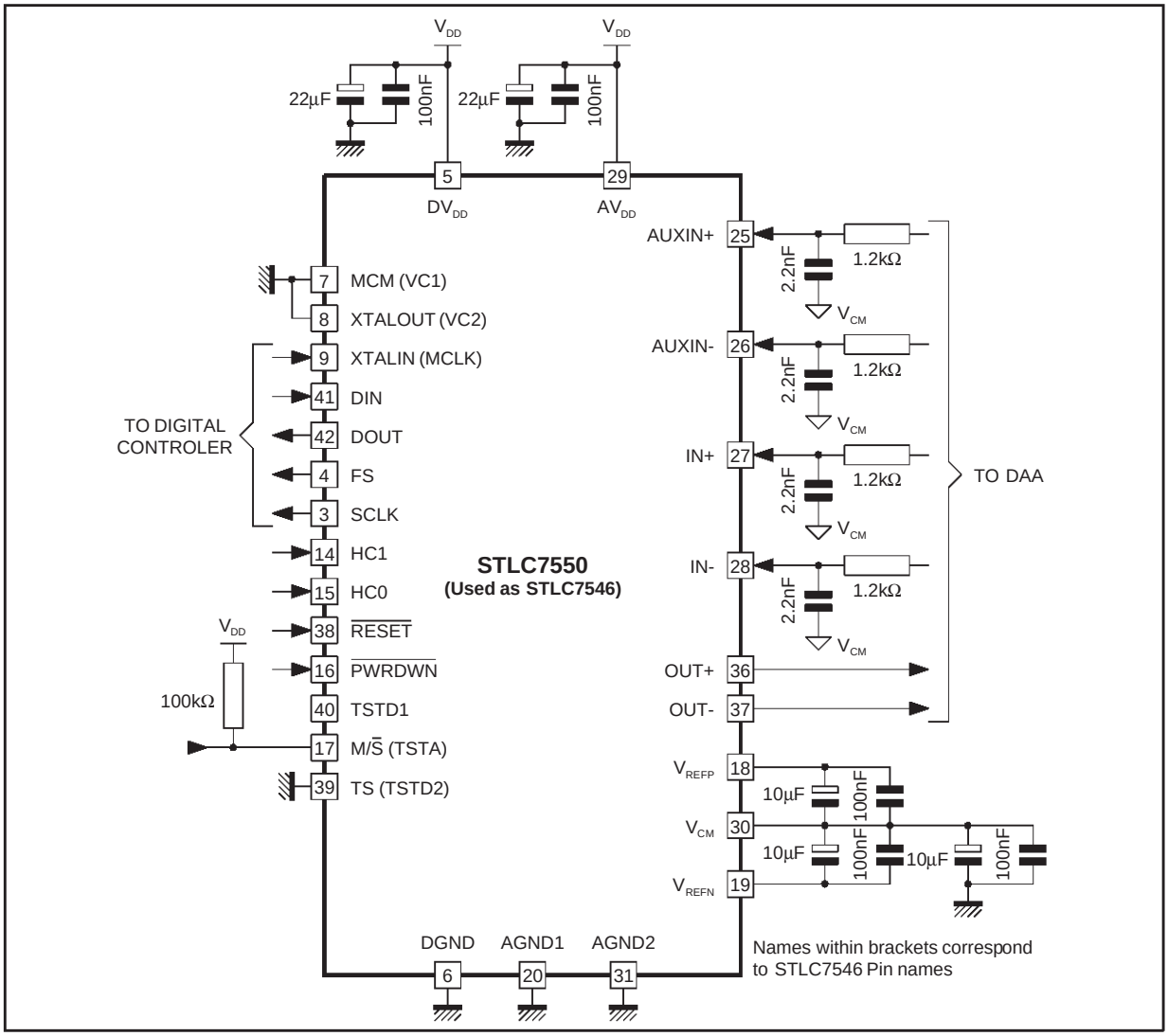
Note that STLC7550 M/$\overline{S}$ Pin must be connected to Vdd, and that there is no compatibility for test modes (STLC7546 test pins and registers are used for additional features in STLC7550).

Figure 1



II - COMPATIBILITY WITH STLC7546 (continued)

Figure 2 : Implementation of STLC7550 as a STLC7546 Codec



III - CLOCK GENERATOR

III.1 - Clock Generator Modes

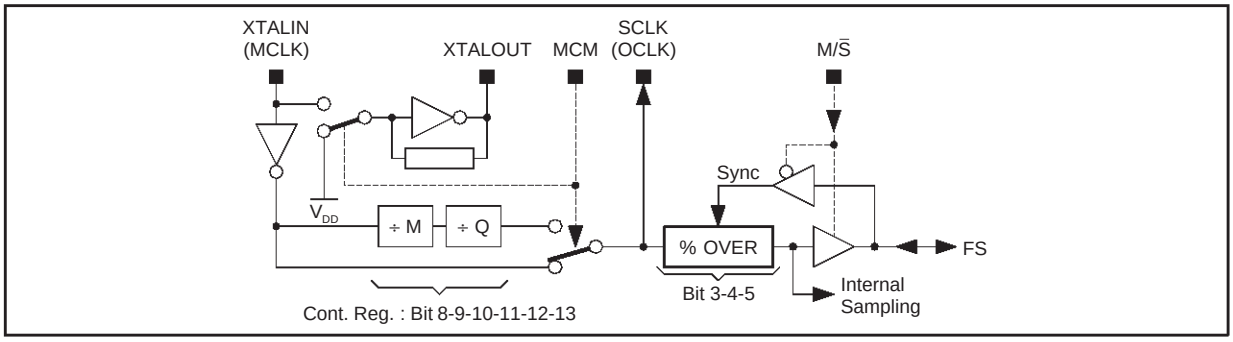
Figure 3 gives the clock generator architecture. Depending on the MCM input state, two modes are available (see Table 1).

Table 1 : Clock generator modes

MCM	XTALIN	XTALOUT	SCLK	FS	Description
0	XTALIN pin should be driven by an Fsx OVER clock, with Fs the required sampling frequency.	Not used. Should be left open, or can be connected to ground for compatibility with STLC7546.	XTALIN	XTALIN/ OVER	STLC7546 mode. Sampling frequencies are generated externally.
1	Connected to a crystal (e.g. 36.864MHz)		XTALIN/ (MxQ)	XTALIN/ (OVERxMxQ)	All V.34 and 56Kbps frequencies are generated internally by STLC7550, by programming OVER, M and Q registers.

III - CLOCK GENERATOR (continued)

Figure 3 : Clock Generator



III.2 - Crystal Oscillator

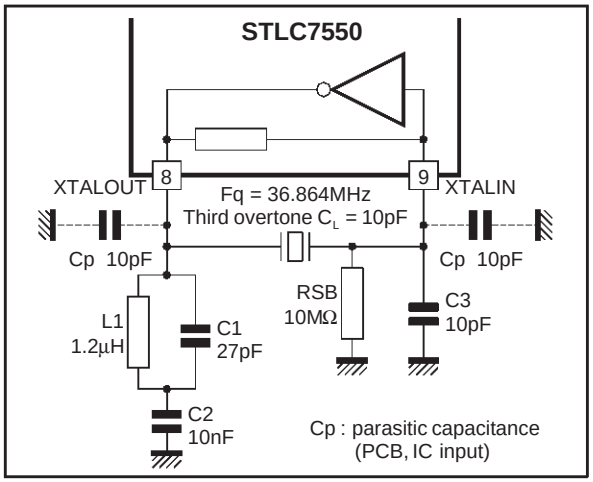
When Pin MCM is set to 1, the master clock is provided by a crystal oscillator connected between the XTALIN and XTALOUT Pins.

The nominal frequency of the oscillator is 36.864MHz. At this frequency, both third overtone and fundamental mode crystals are available.

III.2.1 - Third Overtone Crystal Oscillator

Figure 4 gives the schematic for an oscillator using a 36.864MHz third overtone crystal with a load capacitance C_L of 10pF. The design is a 'Pierce' structure with an additional inductor at the output side for right start-up at the third overtone.

Figure 4 : Oscillator Schematic for 3rd Harmonic Mode Crystals.



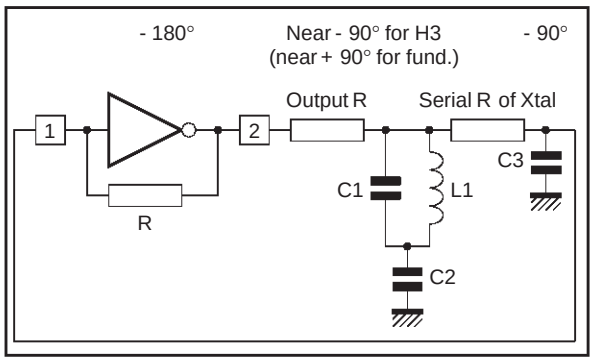
RSB is optional. This resistor influences the stand by mode current consumption ISB : without RSB ISB ≤ 15 µA with RSB = 10MΩ ISB ≤ 1 µA. In order to complete the start-up condition (i.e. at nominal frequency the loop gain has a phase angle of 0 degrees and a module greater than 1), feedback components must provide a -180 degrees phase shift to the STLC7550 inverter action :

- 1st RC cell: output R of inverter / total output capacitance,
- 2nd RC cell: serial R of crystal / total input capacitance.

When the oscillator is running, current is exchanged through the crystal between its load capacitors, with always inverted phase voltages across them.

When a serial resonant crystal is used in such an oscillator, resulting frequency is always greater than target frequency, and a too high capacitor value should be necessary to converge. For this range of frequencies (35 to 50MHz), a third overtone crystal specified with parallel 10pF load is suggested. Then, the basis capacitor's values of the "Pierce" design are 20pF each; if crystal is specified with higher C_L, resulting capacitors can become too high for the oscillator starting up. If an overtone crystal is used in a classic "Pierce" structure without inductor, resulting frequency will be around the fundamental. If an inductive reactance is forced lower than the capacitance's one for the fundamental (see Figure 5), it cancels the start up condition of the oscillator (+90 instead of -90 into a feedback cell). For the third harmonic's frequency of the crystal, using properties of the LC cell, inductor's impedance is lower than capacitance's one. Then, resulting reactance is forced by the capacitance, and the goal is reached.

Figure 5 : Third Overtone Oscillator Simplified Schematic



III - CLOCK GENERATOR (continued)

Computing of application's schematic values (see Figure 4)

The crystal is supposed to be specified as: 36.864MHz, third overtone, CL = 10pF.

Input capacitance of the oscillator has to be twice CL, therefore 20pF made by :
- parasitic value Cp from the chip and from the board layout, supposed to be about 10pF
- capacitor C3 (10pF)

On the output side, it is necessary to take care of the inductor to compute the value of C2. The L1,C1 cell prevents the crystal to oscillate at its fundamental frequency. The cell cut-off frequency (Fc) is typically set near 2/3 of the third overtone :

$$(1)\ f_C = \frac{2}{3} \cdot f_Q \ \text{ with } \ f_C = \frac{1}{2\pi \sqrt{L1 \cdot (C1 + Cp)}}$$

Fc value is not critical. A value too close to f_Q is not recommended, because of the too high impedance reached which can open the feedback network of the oscillator.

The L1,C1 cell is also optimized to balance equivalent capacitance at both crystal pins at f_Q. For this purpose, at third overtone frequency, the L1,C1 cell should be equivalent to the C3 capacitor. This gives the following condition :

$$Z_{L,C} = Z_{C3} \text{ with } Z_{C3} = \frac{1}{j(C_3 + C_p) \cdot \omega'} \text{ and}$$

$$Z_{L,C} = L1 /\!/ C1 = \frac{jL1 \cdot \omega}{1 - L_1 \cdot (C_1 + C_p) \cdot \omega^2}$$

Using relation (1) with $\omega_Q = 2\pi \cdot f_Q$, this condition can be reduced to :

$$(2)\ C_1 + C_p = \frac{C_3 + C_p}{1 - (\frac{2}{3})^2} = \frac{C_3 + C_p}{0.55} = 2CL$$

The closest standard value are :

C3 = 10pF
C1 = 27pF
L1 = 1.2µH

Bypass capacitor's value is not critical (10nF to 100nF). C2=10nF

The final frequency will depend on the evaluation of parasitic capacitors. An accuracy of ± 10ppm is possible.

Note that all oscillator components should be mounted close to the codec with direct traces to the XTALIN, and XTALOUT Pins.

Specifications for components values of STLC7550 third overtone oscillator are :

Crystal :
- a serial resistor R_S 50Ω. If higher, oscillator start-up may be compromised.
- third overtone, parallel resonant mode
- frequency tolerance: ± 50ppm (Frequency and Temperature)
- a load capacitance CL around 10pF. If CL is higher, resulting capacitors can become too high for the oscillator starting up.

Inductor :
- L1 value : ± 10%
- DC resistance < 0.3Ω
- Wirewound inductor recommanded

Capacitors :
C1,C2 : ± 10%

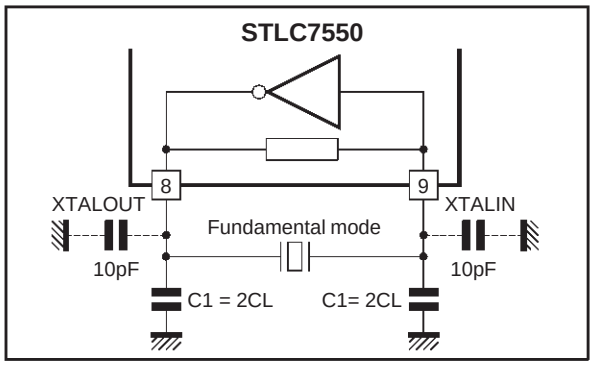
III.2.2 - Fundamental mode crystal oscillator

Figure 6 gives the "Pierce" structure for an oscillator using a 36.864MHz fundamental mode crystal.

C1 + Cp value is chosen as two times the crystal load capacitance CL.

Crystal specifications are :
- a serial resistor R_S 50Ω. If higher, oscillator start-up may be compromised.
- fundamental, parallel resonant mode
- frequency tolerance : ± 50ppm (Frequency and Temperature)
- a load capacitance CL (10pF type for this frequency crystal range). If CL is higher, resulting capacitors can become too high for the oscillator starting up.

Figure 6 : Oscillator Schematic for Fundamental Mode Crystals.



IV - SERIAL INTERFACE

IV.1 - Control Mode

STLC7550 has only one 16-bit control register which makes the codec easy to program.

The codec presents two different modes :

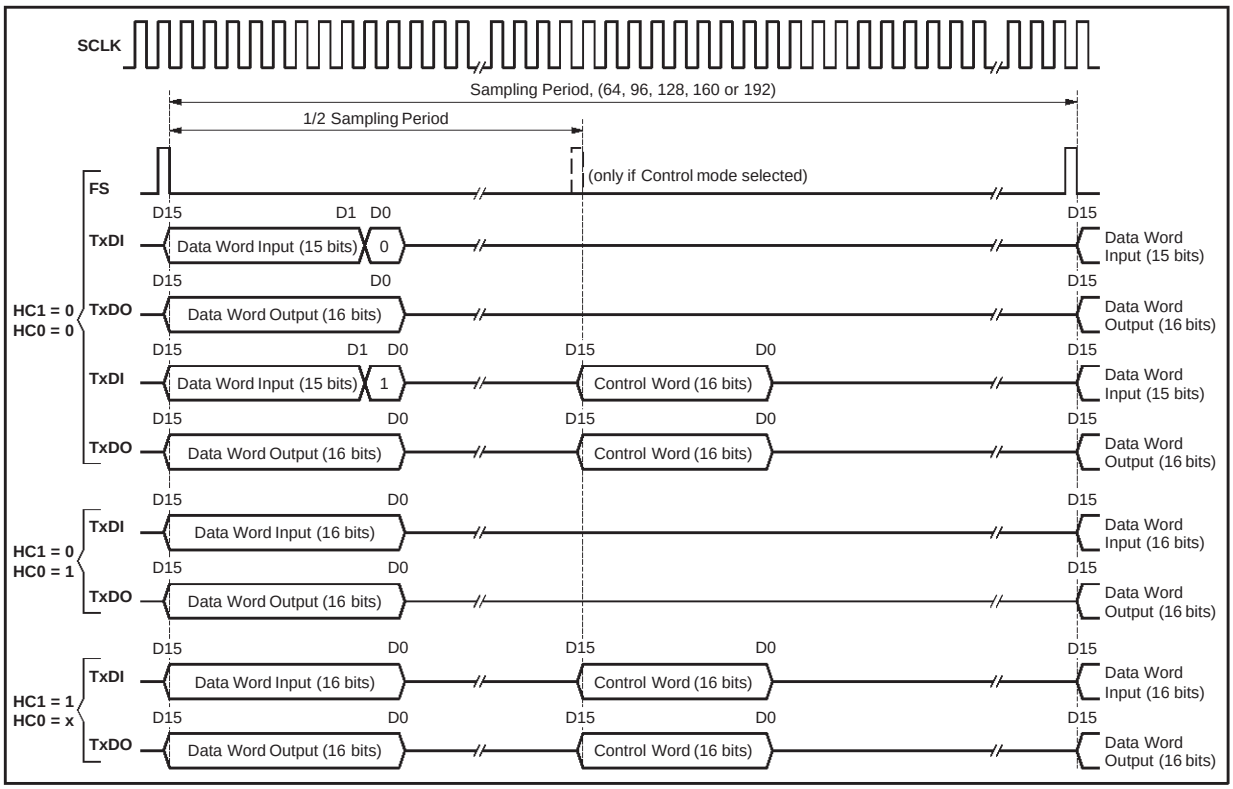
- a Data mode where only data are exchanged in the frame (Data Word Input and Data Word Output).
- a Control mode where data are followed by Control words for register access (Control Word to program the control register, and Register Word to read the register state).

The mode (Data or Control) can be selected either by software or hardware (see Figure 7) :

- Software : HC1 = HC0 = 0 and LSB of Data Word Input select the mode :
- LSB = 0 : Data mode LSB = 1 : Control mode
- Hardware : HC0 = 1 and HC1 select the mode :
- HC1 = 0 : Data mode HC1 = 1 : Control mode

Note that in Software control mode, Data Word input is on 15 bits only. After the codec has been configured it can be convenient to switch to the Hardware Data Mode (HC0 = 1, HC1 = 0) to get a full 16 bits data exchange.

Figure 7 : Chronogram of Serial Interface for Data and Control Modes (Pin TS = 0).



IV - SERIAL INTERFACE (continued)

IV.2 - Master/Slave Mode

Digital interface can be synchronized by either STLC7550 (Master mode) or by an other device (Slave Mode).

- In Master mode, the codec generates the FS signal (FS Pin is an output), with half period extra synchronization pulse for control frame if needed.
- In Slave mode, the codec receives the synchronization signal FS on the Pin FS (set as input). Half period extra synchronization pulse for control frame should be also present on FS input when needed. However since codec programming requires only one frame (only one control register), the 1/2 Sampling period pulse is not mandatory. In that case programming will be done on the next FS pulse and only one data sample will be lost.

IV.3 - TS Pin

When TS = 0 data are assigned to the first 16 bits after falling edge of FS (7546 mode) otherwise data are in bits 17 to 32. (Note that the case $M/\overline{S}$ = 1 with TS = 1 is reserved for life-test). This feature allows dual codec application. An example is given on Figure 8, and the resulting chronogram of the serial interface is given on Figure 9.

Note : when programming either codec in software mode, both codecs should be in fact programmed at the same time. As FS is the same for both, the secondary pulse can be interpreted as a main pulse by the codec that is not being programmed with a complete loss of synchronisation. In hardware mode this problem is not present because HC0 and HC1 control both codecs at the same time.

Figure 8 : Dual Codec Application

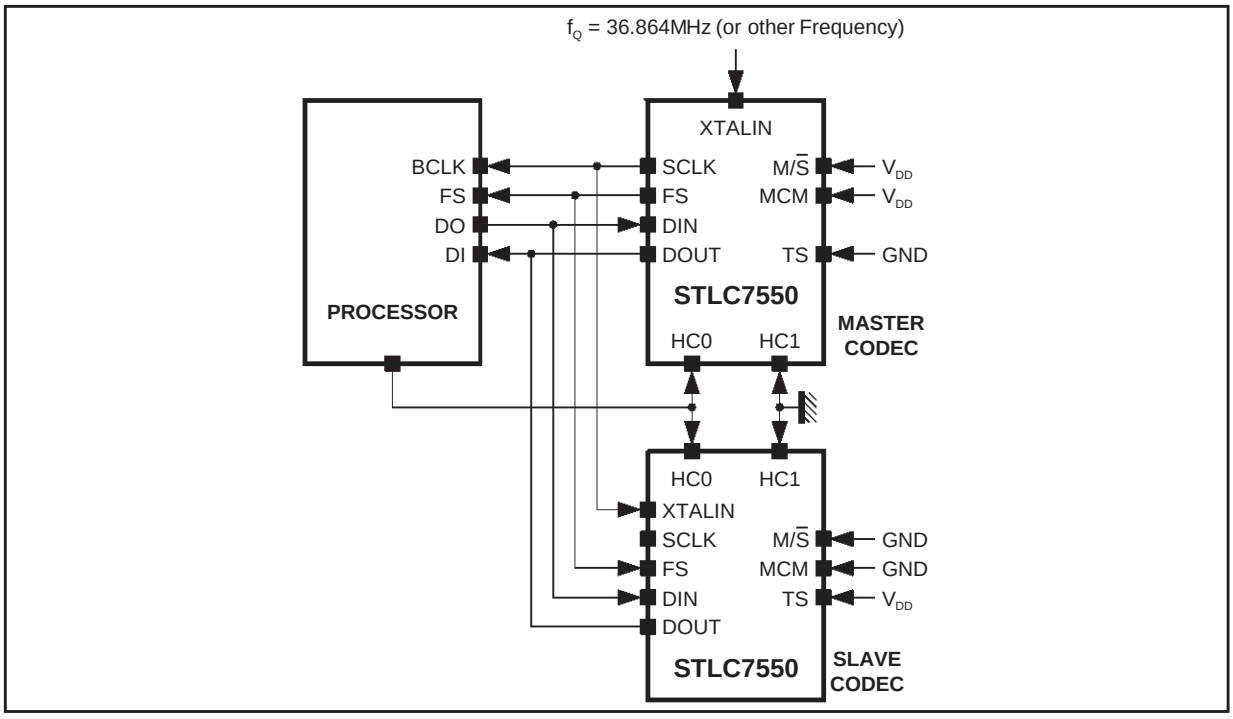
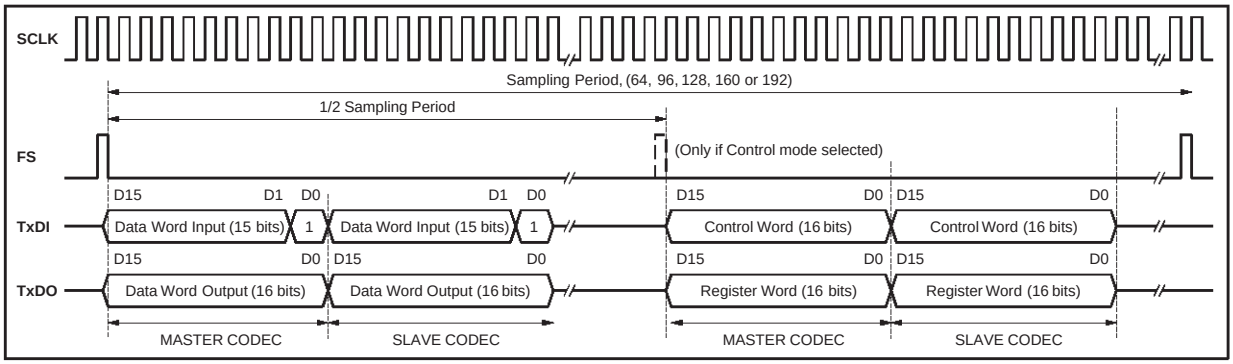


Figure 9 : Example of Serial Interface Chronogram for Dual Codec Application (HC0 = 0, HC1 = 0)



IV - SERIAL INTERFACE (continued)

IV.4 - Reset and Powerdown (see Figure 10)

Serial Interface

Table 2 : Serial interface state during Reset and Powerdown

	Master Mode (M/S = 1)		**Slave Mode** (M/S = 0)	
	MCM = 1	**MCM = 0**	**MCM = 1**	**MCM = 0**
SCLK	V_{DD}	$\overline{MCLK}$	V_{DD}	$\overline{MCLK}$
FS	GND	GND	Hi Z	Hi Z
DOUT	Hi Z	Hi Z	Hi Z	Hi Z

Control Register

When Reset Pin is set to 0, the codec is set to the state given in Table 3. In powerdown mode (PWRDWN = 0), no change is done on the configuration register, and so the previous programming is preserved.

Table 3 : Reset State

Bits	Reset Value	Reset State
D0	0	-
D1	0	Main receive input
D2	0	0dB receive gain
D3	0	Over = 160
D4	0	
D5	0	
D6	0	Infinite Transmit attenuation
D7	0	
D8	1	M = 4
D12	0	
D13	0	
D9	1	Q = 6
D10	0	
D11	0	
D14	0	No Test mode
D15	0	

V - TRANSMIT AND RECEIVE FILTER STAGES

V.1 - Transmit D/A Section

V.1.1 - Architecture (see Figure 11)

The complete D/A section is composed of the following filter stages :

- transmit low pass filter (interpolating filter) with combination of FIR + IIR as well sinx/x compensation,
- digital second order noise shaper,
- single pole analog low pass filter.

V.1.2 - Frequency Response

In band frequency response *(0-5kHz)*

Figures 12 and 13 show the transmit frequency response of the complete transmit channel.
The measurement have been done with a RODHE & SCHWARZ AUDIO ANALYZER 2Hz-300kHz UPD. The sampling frequency is 9.6kHz and oversampling ratio is 160. Figure 12 is the frequency response with a accurate scale which shows that thanks to the sinx/x compensation, the frequency response is flat in the frequency band [0-0.425 x Fs]. Figure 13 shows the filter performances.

Out of band spectrum

Figure 14 gives the output signal measured at the differential outputs OUT+/OUT-. The total noise level is this frequency band is -27dBV. In order to comply which the out of band noise specification, measured on the phone line, an external second order continuous time filter is necessary. Figure 15 shows the phone line spectrum measured with our demoboard using the filter characteristics described on Chapter VI of this application note. The total noise level in the 100kHz band is -63dBV.

V.2 - Receive A/D Section (see Figure 16)

The A/D channel performs the decimation function using 2 filters, one FIR and one IIR. The cut-off frequency is 0.425 x sampling frequency.

Figure 10 : Reset and Powerdown Exit Time

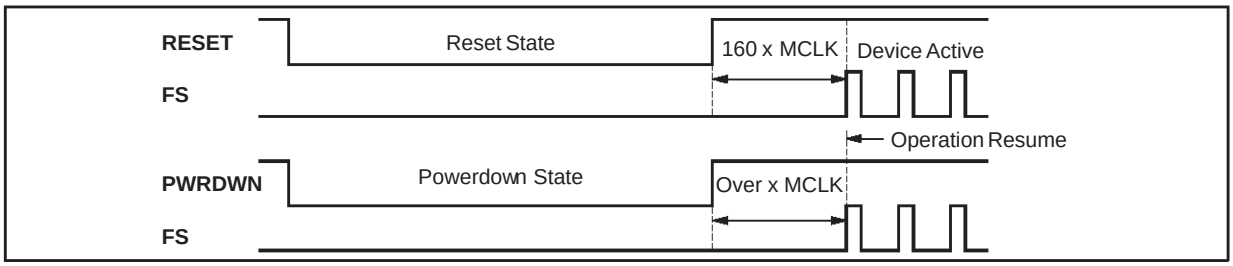
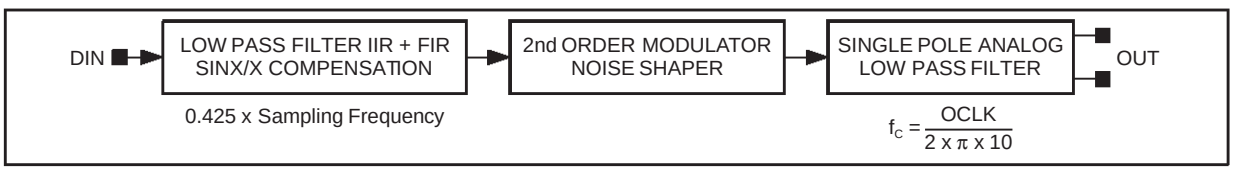
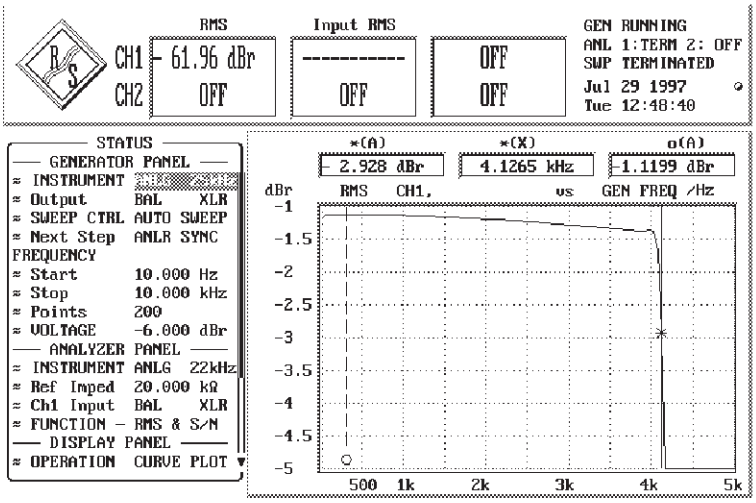


Figure 11



V - TRANSMIT AND RECEIVE FILTER STAGES (continued)

Figure 12 : Frequency Response (0-5kHz) Flat thanks to sinx/x compensation



AN930-12.PCX

Figure 13 : Tx Filter Efficiency

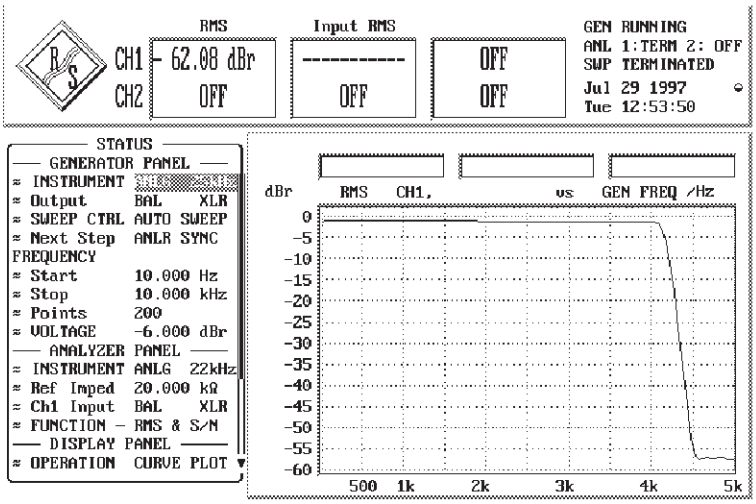


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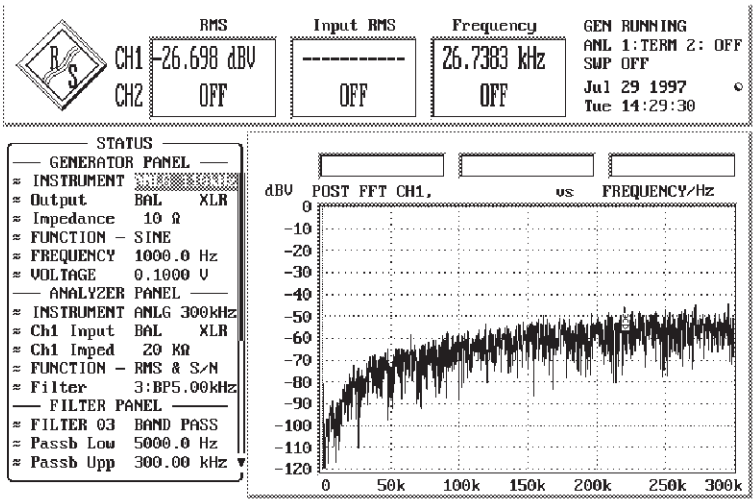
Figure 14 : Out of Band Signal at the Codec Output



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V - TRANSMIT AND RECEIVE FILTER STAGES (continued)

Figure 15 : Out of Band Signal on the Phone Line

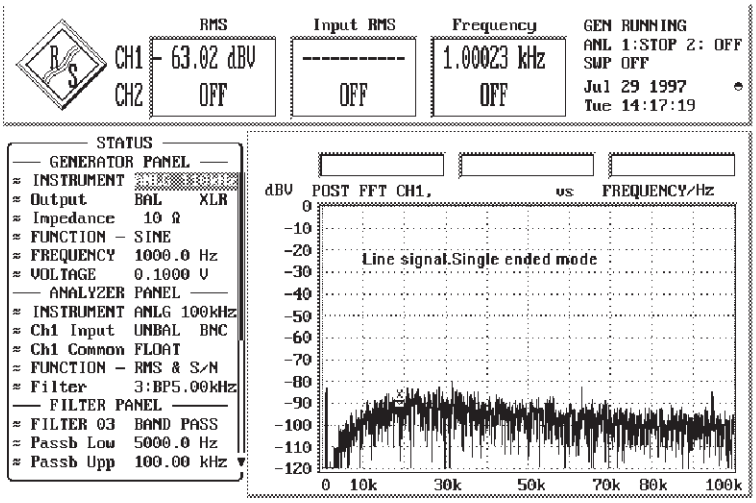

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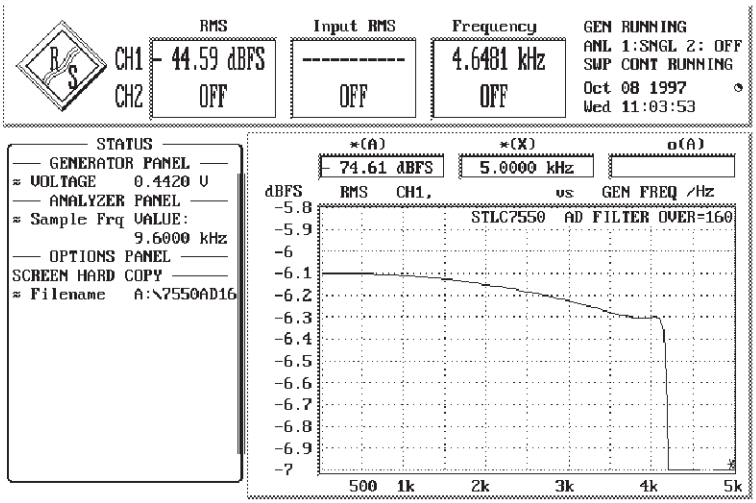
Figure 16 : AD Section Filter (over = 160)



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VI - LINE INTERFACE

STLC7550 is targeted for V.34bis standard and 56kbps new standard and for low-power application. Line interface has to present :

- good performances to allow high speed communication,
- a supply around 3V only,
- small size to allow the modem to fit in portable applications for which low-power solutions are usually dedicated.

An overview of the proposed modem line interface is shown on Figure 17. The STLC7550 transmit and receive signals from the phone line via a duplexor (that isolates modem from phone line, filters and amplifies signal) and a bridge (to allow the modem to work even Tip and Ring are inverted). Then the line is taken with a ON HOOK/OFF HOOK switch, and by driving a constant current (current driver block). A ring detect block signals to the digital controller via the RING signal incoming calls. The different blocks are detailed hereafter.

VI.1 - Duplexor

VI.1.1 - Differential Duplexor

This duplexor is also called hybrid for it interfaces the 2-wire bi-directional phone line in two separate differential and unidirectional lines to the codec (Transmit and Receive). A differential duplexor for the modem part is given on Figure 18. Hybrid performances are mainly depending on a good impedance matching with the phone line and a good Transmit rejection on the Receive input (loss).

Figure 17 : Line Interface Overview

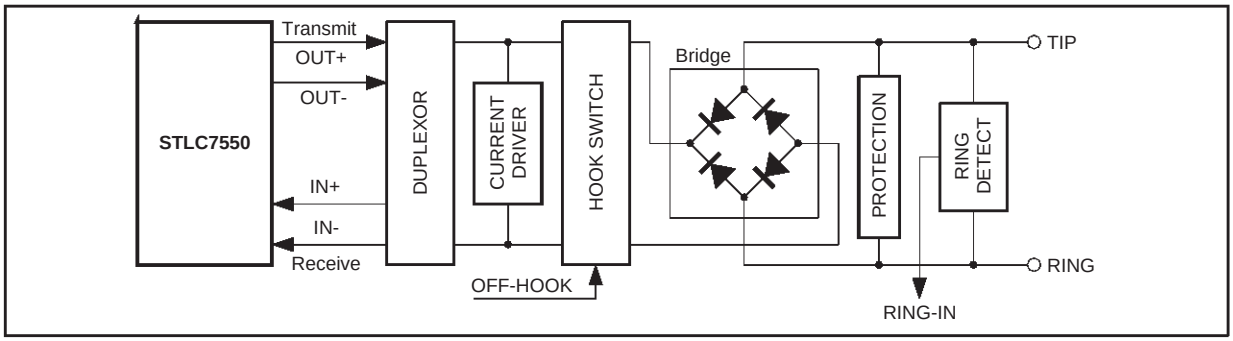
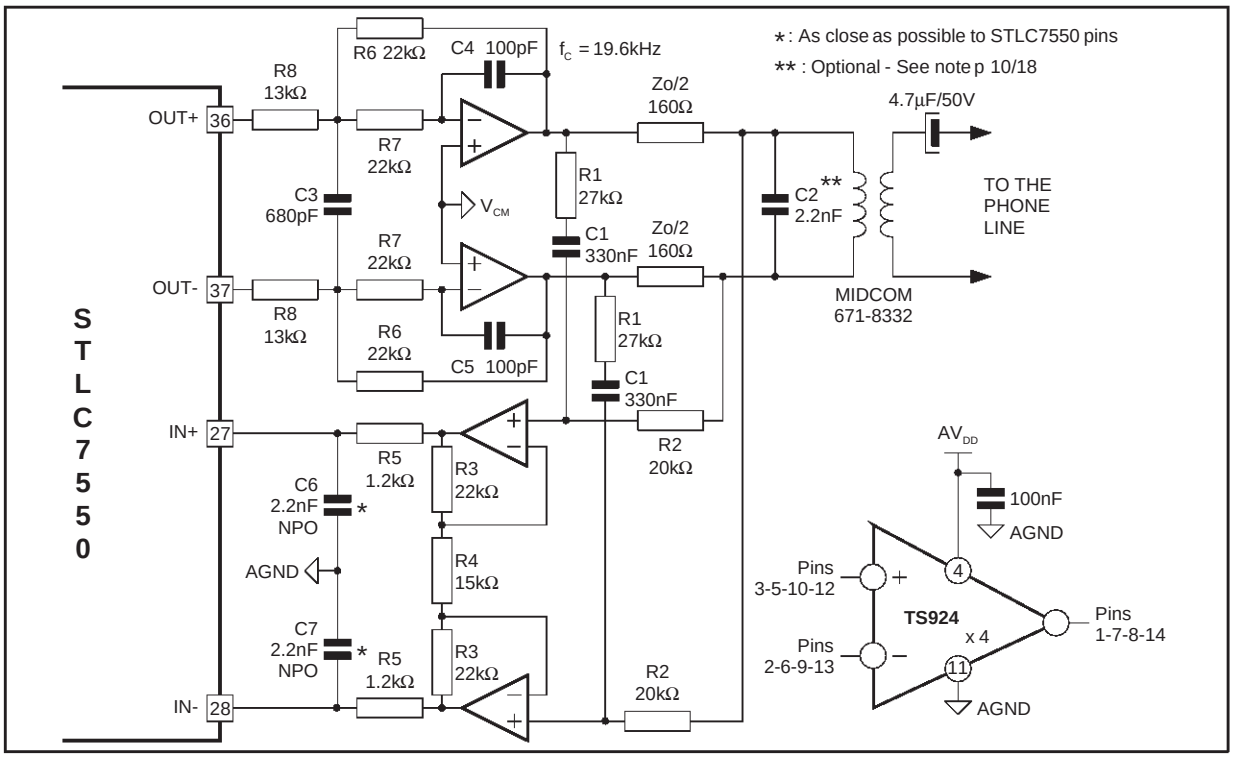
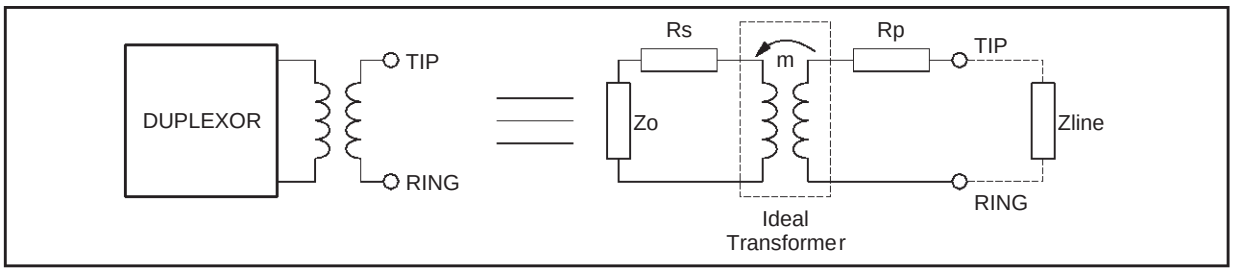


Figure 18 : Differential Duplexor



VI - LINE INTERFACE (continued)

Figure 19 : Line Interface Equivalent Model



A. Phone Line Impedance Matching

Impedance mismatches between line and DAA cause reflections and interference between Transmit and Receive signals giving echoes that limit modem speed. The impedance matching is related to the phone line impedance (Zline) - that depends on the country, line length, and the signal frequency. The following schematics are targeted for Zline = 600Ω. See paragraph VI.1.4 for an example with complex impedance.

Figure 19 shows the equivalent model of a line interface, where Zo is the duplexor equivalent impedance, R_P and R_S the transformer resistance, and Zline the phone line impedance.

The impedance matching condition is :

$$R_P + Z_O/m^2 + R_S/m^2 = Zline \quad [1]$$

Application :

The MIDCOM 671-8332 transformer used gives the following performances :

- R_P = 155Ω, R_S = 150Ω
- turns ratio m = 1 ± 1%
- longitudinal balance : 40dB min.
- total harmonic distortion : 82dB
- insertion loss : 3.0dB Typ.

Zline = 600Ω

[1] = Z_O = (Zline-Rp) . m^2 - R_S = 295Ω

Impedance recommended by MIDCOM is 316Ω.

We take $Z_O/2$ = 160Ω.

**Note : the capacitor C2 is used to add a third external pole for DAC-channel noise rejection. Nevertheless, it can increase electrical echo on receive section. It is dependent on the phone line type.

B. Transmit Rejection

For full duplex communication a Transmit signal rejection on the Receive part is made by resistor R1 and R2. In that way, only the incoming phone line signal is present on the Receive output.

The loss of Transmit signal is given by (see Figure 20) :

$$LOSS = \frac{V_{Receive}}{V_{Transmit\ (No\ signal\ received)}} \quad [2]$$

$$= 20 \cdot Log\left(\frac{Z_{EQ}}{Z_{EQ}+Z_O} \cdot \frac{R1}{R1+R2} - \frac{R2}{R1+R2}\right)$$

with Zeq being the equivalent impedance of the phone line impedance seen from the secondary of the transformer.

Maximum loss is achieved when :

$$\frac{Z_{EQ}}{Z_{EQ}+Z0} = \frac{R2}{R1} \quad [3]$$

Application :

R2 = 20kΩ, Zo = 320Ω

$Z_{EQ} = R_S + Rp \cdot m^2 + Zline.m^2$ = 905Ω

[3] => R1 = $(Z_{EQ} + Z0) \cdot R2/Z_{EQ}$ = 27.07kΩ.

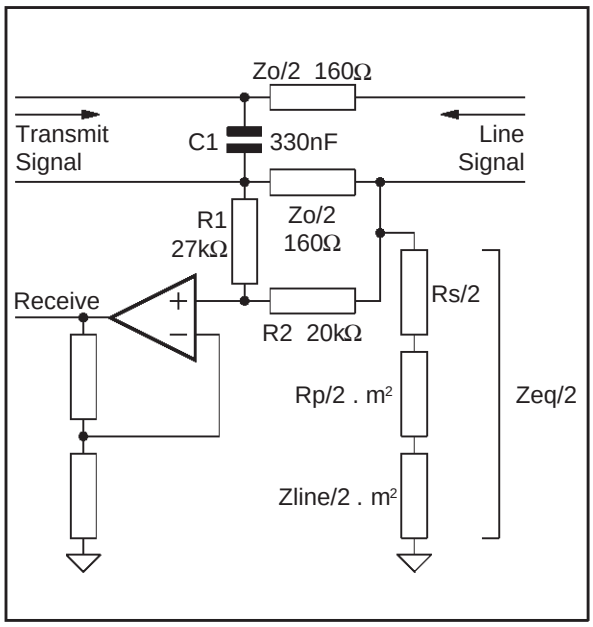
We take R1 = 27kΩ.

[2] => Loss = -59dB (theoretical value, resistor values should be certified at 1% for good performances).

C1 = 330nF.

C1, R1 improves the low frequency response. These values depend on the transfer function of the transformer. Filter transfer function made by C1, R1 must compensate for the loss in transformer at low frequencies. If a compensation is not needed, the capacitor C1 can be suppressed.

Figure 20 : Transmit Rejection simplified AC Schematic



VI - LINE INTERFACE (continued)

C. Transmit Filter *(see Figure 21)*

A two-pole continuous time external filter must follow the output pin in order to remove quantization noise. The filter characteristics are :

Transfer function with :

$$H = G_T \cdot \frac{1}{1 + 2 \cdot x \cdot s + s^2} \text{ with } s = j \frac{\omega}{2\pi \cdot f_C}$$

DC gain :

$$GT = \frac{R6}{R8}$$

Overvoltage factor :

$$x = \frac{1}{2} \cdot \left(\sqrt{\frac{R7}{R6}} + \sqrt{\frac{R6}{R7}} + \frac{\sqrt{R6 \cdot R7}}{R8} \right) \cdot \sqrt{\frac{C4}{2 \cdot C3}}$$

Cutoff frequency :

$$f_C = \frac{1}{2\pi \sqrt{R_7 \cdot R_6 \cdot C_4 \cdot 2 \cdot C_3}} \text{ with } f_C > 2 \cdot f_S \text{ [4]}$$

f_C must be at least twice the value of the sampling frequency.

The filter also amplifies (with a gain G_T) the Transmit signal to compensate the loss (L_T) due to the divider made of resistor Z0 and equivalent line impedance Z_{EQ}. The gain condition that makes the codec maximum output level A_C to match with maximum phone line level A_L is :

$$A_C \cdot L_T \cdot G_T = m \cdot A_L$$

$$\text{with } G_T = \frac{R_6}{R_8} \text{ and } L_T = \frac{Z_{line}}{Z_O + Z_{EQ}} \text{ [5]}$$

For low-power application, op-amp supply is limited to 3V and can be a limitation. It is advised to use Rail to Rail op-amp dedicated to 3V application. Op-amp should never saturate, i.e. the op-amp output signal peak-to-peak level should lie within the supply range : $A_C \cdot G_T < 3V$ [6]

Application

DTMF level is considered as the highest level to be transmitted. Levels used in this application are :

- High group tone level : -9dBV + 2/-2.5 ($1V_{PP}$)
- Low group tone level : -11dBV + 2.5/-2 ($0.80V_{PP}$)
- The level of the tone in the high group must be 1dB to 4dB higher than the level of the tone in the low group.

In consequence maximum DTMF signal level is within 1.38 and $2.32V_{PP}$. The maximum phone line level is set to 2.2V (corresponding to a 0dBm single tone).

$2 \cdot A_L = 2.2V_{PP}$ ($2 \cdot A_L$ because of differential structure)
$\Rightarrow A_L = 1.1V_{PP}$
Z0 = 320Ω, Zline = 600Ω, Z_{EQ} = 905Ω, [5] gives $L_T = 0.490$, A_C =1.25V, m = 1
[5] gives $G_T = m \cdot A_L / (A_C \cdot L_T) = 1.795 = +5dB$

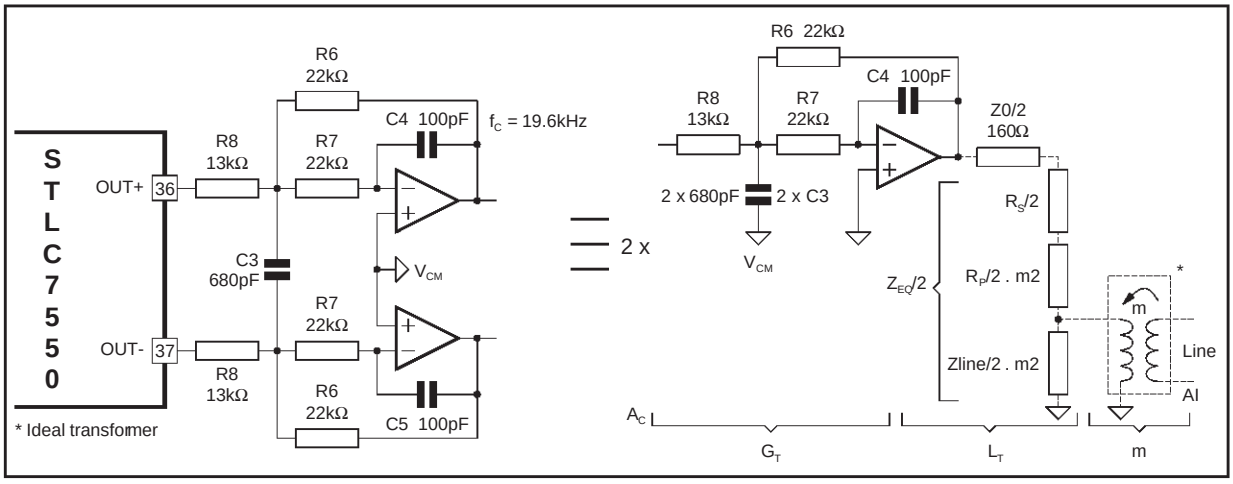
Choosing R6 = 22kΩ gives R8 = 13kΩ (STLC7550 minimum load is 10kΩ) and $G_T = 2$

[6] $A_C \cdot G_T = 2.5V_{PP} < 3V$ Op-Amp are not saturated

Note : The maximum line level during V.34 communication is around $1.2V_{PP}$. This gives a maximum signal level on codec output pin around $0.6V_{PP}$ $[1.2/(2 \cdot G_T \cdot L_T)]$ that gives a good dynamic with no distortion.

Sampling frequency : 9.6kHz gives f_C # 19.2kHz choosing R7 = 22kΩ, C3 = 680pF and C4 = 100pF, [4] gives f_C = 19.6kHz

Figure 21 : Transmit Filter



VI - LINE INTERFACE (continued)

D. Receive Amplifier

Receive amplifier compensate with a gain G_R :

- the loss L_R due to the resistor R1 and R2 divider,
- the loss L_T due to the transformer, composed by the resistor Z_O and the transformer impedance $R_S + Rp \cdot m2$

The gain condition that makes the maximum line level A_L match with the maximum STLC7550 input level A_S is :

Application :

m = 1

Maximum line level : 0dBm,

$2 \cdot A_L$ = 0dBm = 2.2V_{PP}, A_L = 1.1V_{PP},

R1 = 27kΩ, R2 = 20kΩ, L_R = 0.57,

Z_O = 320Ω, R_S = 150Ω, Rp = 155Ω, L_T = 0.512,

A_S =1.25V_{PP}

$G_R = A_S/(A_L \cdot L_R \cdot L_T)$ = 3.89 = 11.8dB

We take R3 = 22kΩ and R4 = 15kΩ, gives G_R = 3.93 = +11.90dB.

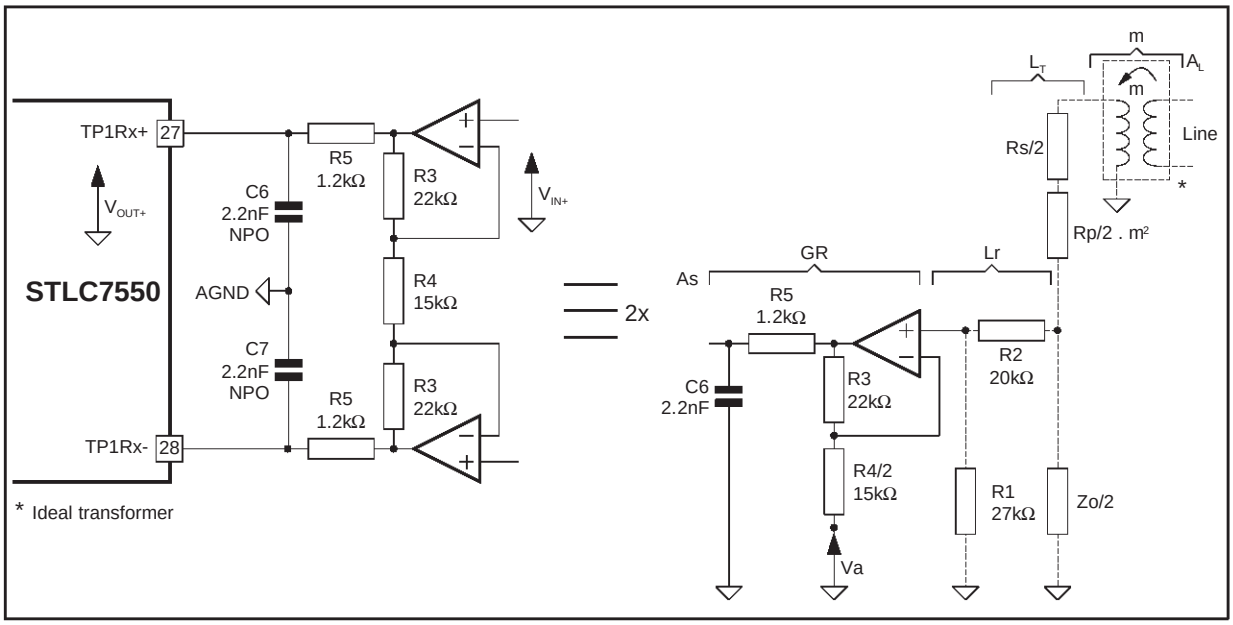
Note : The maximum line level during V.34 communication is around 1.2V_{PP}. This gives a maximum signal level on codec input pin around 0.68V_{PP} [(1.2 /2). $L_R \cdot L_T \cdot G_R$)] that gives a good dynamic with no distortion.

Resistor R4 has also the function of balancing signal TP1Rx+ and TP1Rx- to improve symmetry.

Note : Va is the average voltage between V_{OUT}+ and Vout- that represents the output asymmetry. In ideal conditions it should be equal to 0.

The single pole anti-aliasing filter (R5, C6) removes high frequency noises. C6 must be put as close as possible to the chip. The cut-off frequency must be lower than one half of the oversampling frequency (i.e. lower than 460kHz).

Figure 22 : Receive Amplifier



VI - LINE INTERFACE (continued)

VI.1.2 - Low Cost DAA using A 1:1 Transformer

A duplexor for low-cost application is proposed on Figure 23. Performance depends mainly on a good impedance matching with the phone line and a good Transmit rejection on the Receive input (loss).

A. Phone Line Impedance Matching

See VI.1.1 Differential duplexor.

=> $Z_O = 320\Omega$

B. Receive Amplifier

The amplifier gain G_R (fixed by R5 and R7) is chosen to compensate the loss (L_R) given by the divider composed by resistor Z_O and transformer impedance (R_S + Rp · m2), with $V_{transmit}$ = 0 (see Figure 24). The condition to make maximum line level AL match with maximum codec input level A_S is :

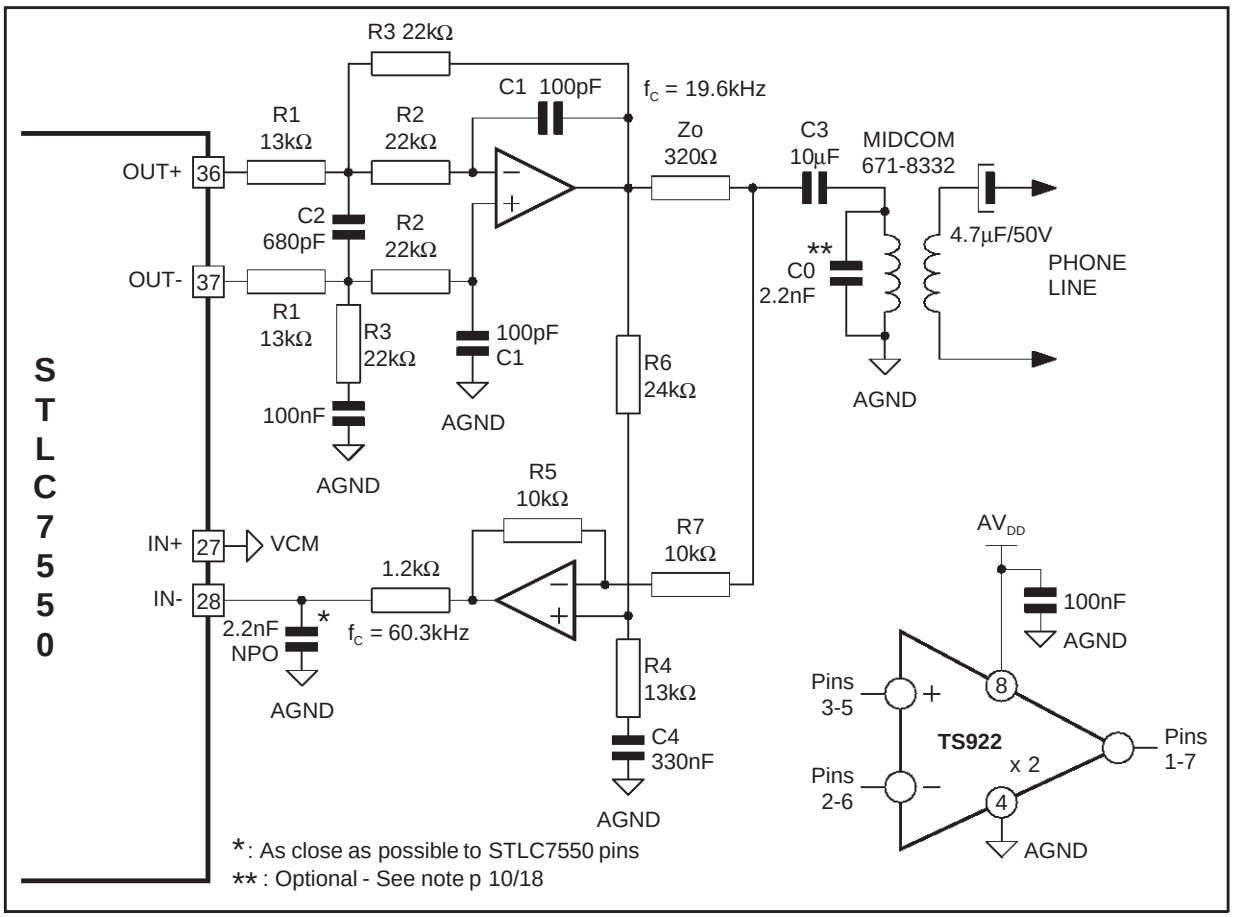
Application :

m = 1,
AL = 0dBm = $2.2V_{PP}$,
R_S + Rp · m2 = 305Ω, Z_O = 320Ω, L_R = 0.512,
A_S = $1.25V_{PP}$,
$G_R = AS/(m \cdot AL \cdot LR) = 1.109 = +0.9dB$

Choosing R5 = 10kΩ gives R7 = 10kΩ and GR = 1.

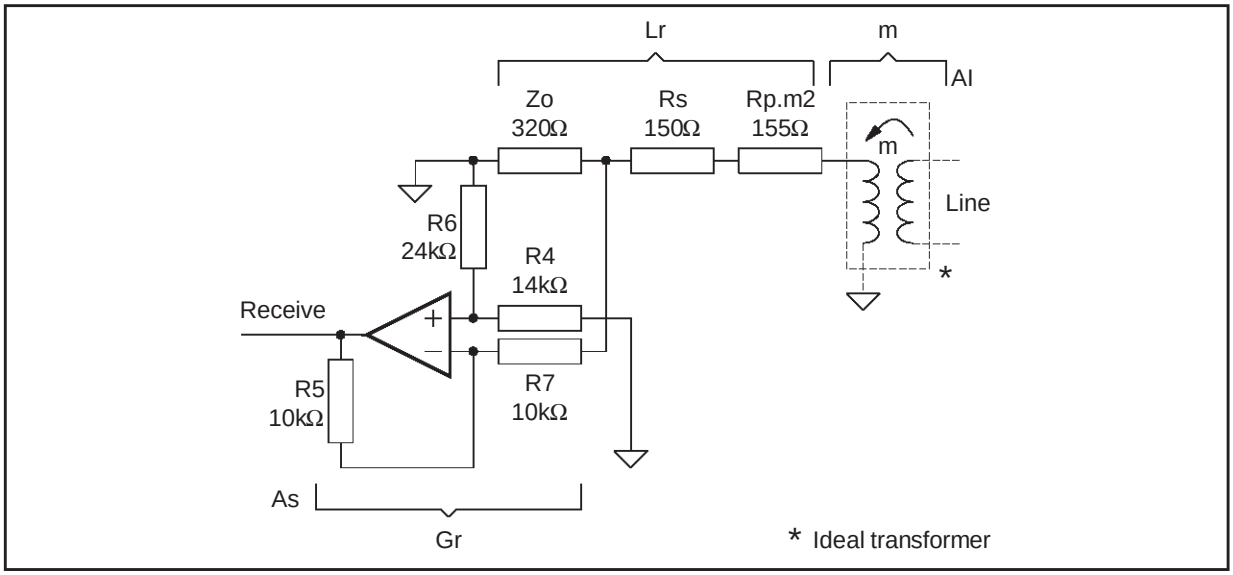
Note : The maximum line level during V.34 communication is around $1.2V_{PP}$. This gives a maximum signal level on codec output pin around $0.6V_{PP}$ $[1.2 \cdot m \cdot L_R + G_R]$ that gives a good dynamic with no distortion.

Figure 23 : Low Cost Duplexor



VI - LINE INTERFACE (continued)

Figure 24 : Receive Amplifier Simplified AC Schematic (View From Line, No Transmit Signal)



C. Transmit Rejection

For full duplex communication a Transmit signal rejection is made on the Receive amplifier by subtracting the $V_{transmit\ signal}$.
The loss is given by :

$$LOSS = \frac{V_{Receive}}{V_{Transmit(No\ signal\ received)}} \quad [7]$$

$$= 20 \cdot Log\left(\frac{Z_{EQ}}{Z_{EQ}+Z_O} \cdot \frac{R5}{R7} - \frac{R4}{R4+R6} \cdot \frac{R7+R5}{R7}\right)$$

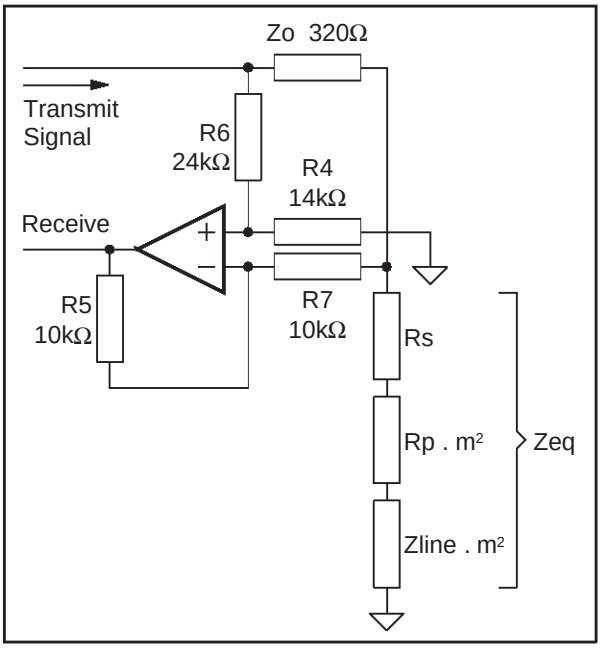
with Z_{EQ} the equivalent impedance of the phone line seen from the secondary.
Maximum loss is achieved when :

$$\frac{Z_{EQ}}{Z_{EQ}+Z_0} = \frac{R4}{R4+R6} \cdot \frac{R7+R5}{R5}$$

Application :
R 5 = 10kΩ, R6 = 24kΩ, R7 = 10kΩ,
R4 = 14kΩ, Z_{EQ} = 905Ω , Z_O = 320Ω

[7] = L_{OSS} = -54dB (Theoretical value, resistor values should be certified at 1% for good performances.)

Figure 25 : Transmit Rejection Simplified AC Schematic (View from Transmit Amplifier, No Signal Received from The Line)



VI - LINE INTERFACE (continued)

D. Transmit filter

A two-pole continuous time external filter must follow the output pin in order to remove quantization noise. The filter characteristics are :

Transfer function :

$$H = \frac{V_{OUT}}{V_{IN}} = G_T \cdot \frac{1}{1 + 2 \cdot x \cdot s + s^2} \text{ with } s = j\frac{\omega}{2\pi \cdot f_C}$$

DC gain : $G_T = -\frac{R3}{R1}$

Peak factor :

$$x = \frac{1}{2} \cdot \left[\sqrt{\frac{R2}{R3}} + \sqrt{\frac{R3}{R2}} + \frac{\sqrt{R2 \cdot R3}}{R1}\right] \sqrt{\frac{C1}{2 \cdot C2}}$$

Cutoff frequency : $f_C = \frac{1}{2\pi\sqrt{R_2 \cdot R_3 \cdot C_1 \cdot 2 \cdot C_2}}$

with $f_C > 2 \cdot f_S$ [8]

f_C must be at least twice the value of the sampling frequency.

The filter also amplifies (with a gain G_T) the Transmit signal to compensate the loss (L_T) due to the divider made of resistor Z_O and equivalent line impedance Z_{EQ}. The condition that makes the codec maximum output level A_C match with maximum phone line level A_L is :

$$A_C \cdot L_T \cdot G_T = m \cdot A_L$$

with $G_T \frac{R3}{R1}$ and $L_T = \frac{Z_{line} \cdot m^2}{Z_O + Z_{EQ}}$ [9]

For low-power application, op-amp supply is limited to 3V and can be a limitation. It is advised to use Rail to Rail op-amp dedicated to 3V application.

Op-amp should never saturate, i.e. op-amp output signal peak-to-peak level should lie within the supply range : $A_C \cdot G_T < 3V$ [10]

Application :

DTMF level is considered as the highest level to be transmitted. Levels used in this application are :

- High Group tone level is -9dBV +2/-2.5
- Low Group tone level is -11dBV +2.5/-2
- The level of the tone in the high group must be 1dB to 4dB higher than the level of the tone in the low group.

In consequence, maximum DTMF signal level is within 1.38 and 2.32 V_{PP}. Maximum phone line level is set to 2.2V (corresponding to a 0dBm single tone).

$A_L = 2.2V_{PP}$, m = 1,

[9] Zline = 600Ω, Z_{EQ} = 905Ω, Z0 = 320Ω, L_T = 0.490,

A_C = 2*1.25V (differential codec output), $A_C = 2.5V_{PP}$

[9] $G_T = A_L \cdot m / (A_C \cdot L_T) = 1.796 = +5.1dB$

Choosing R3 = 22kΩ, (STLC7550 minimum load is 10kΩ,) gives R1 = 13kΩ, G_T = 1.69 = +4.6dB

Note : The maximum line level during V.34 communication is around $1.2V_{PP}$. This gives a maximum signal level on codec output pin around $0.6V_{PP}$ $[1.2 \cdot m/(2 \cdot G_T \cdot L_T)]$ that gives a good dynamic with no distortion.

[10] $A_C \cdot G_T = 4.23V_{PP} > 3V$

When codec outputs are at maximum level (i.e. $1.25V_{PP}$) the op-amp is saturated. The gain value G_T is kept in order to have communication signal on codec input pin within the 0.6V range for best performances. Nevertheless DTMF will be transmitted at a lower level, i.e. at the highest level possible without saturation that is :

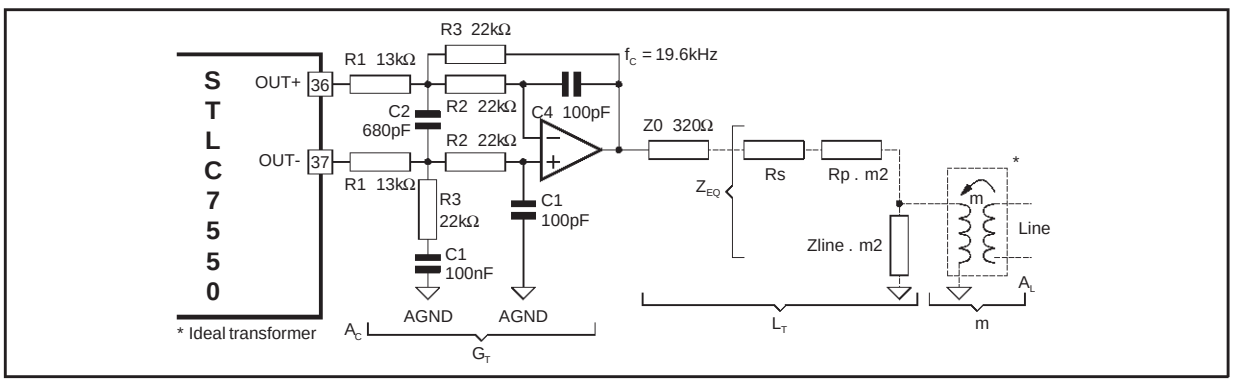
$$\text{DTMF\_LEVEL codec pin} = \frac{\text{op–amp max. output level (3V)}}{2 \cdot G_T}$$

In that case, DTMF signal on the phone line will be DTMF_LEVEL phone line = (op-amp maximum level (3V)) $\cdot L_T = 1.47V_{PP} > 1.38V_{PP}$.

Note that DTMF level on phone line is still within the expected range, but it becomes critical for a DAA designed with a L_T gain not close enough to 0.5. In the case of critical L_T gain, see next chapter for a DAA with a higher turns ratio (1:1.414 instead of 1:1).

Sampling frequency : 9.6kHz gives f_C # 19.2kHz choosing R2 = 22kΩ, C2 = 680pF and C1 = 100pF, [8] gives f_C = 19.6kHz.

Figure 26 : Transmit Filter AC Schematic



VI - LINE INTERFACE (continued)

VI.1.3 - Low Cost DAA using a 1.414:1 Transformer

For low-cost 3V DAA, the Transmit level can become critical because of the single Op-Amp (only 3V of dynamic, refer to the previous chapter VI.1.2). The DAA proposed on Figure 27 uses a transformer with a higher turns ratio that allows a higher Transmit level on the phone line. On this schematic, only component values and transformer reference have been changed. Refer to the previous chapter for a detailed description. (VI.1.2 Low Cost DAA using a 1:1 Transformer). The calculation of the components values is given hereafter.

A. Phone Line Impedance Matching

The MIDCOM 671-9366 transformer used gives the following performances :

- D.C resistance : Primary : 119Ω ± 10 %
  Secondary : 129Ω ± 10 %
- Turns radio : 0.707 : 1 ± 1 % (m = 1.414)
- Longitudinal balance : 46dB min.
- Insertion loss : 2.5dB max.

This 0.707:1 transformer is used as a 1.414:1 one by reverting its sides :

- the secondary (instead of primary) is connected to the phone line.
- the primary is connected to the hybrid.

The obtained transformer characteristics are :

- R_P = 129Ω
- R_S = 119Ω
- m = 0.707

Zline = 600Ω
[1] = $Z_O = (Zline-R_P) \cdot m^2 - R_S$ = 116Ω
We take Z_O = 118Ω

B. Receive Amplifier

m = 0.707
A_L = 0dBm = $2.2V_{PP}$,
$R_S + Rp \cdot m2$ = 184Ω, Z_O = 118Ω, L_R = 0.391
A_S = $1.25V_{PP}$
$G_R = A_S /(m \cdot A_L \cdot L_R)$ = 2.05 = +6.2dB
Choosing R5 = 20kΩ gives R7 = 10kΩ and G_R = 2.

C. Transmit Rejection

R5 = 20kΩ, R6 = 13kΩ, R7 = 10kΩ,
R4 = 15kΩ, Z_{EQ} = 484Ω, Z_O = 118Ω
[7] = Loss = -66dB (Theoretical value, resistor values should be certified at 1% for good performances.)

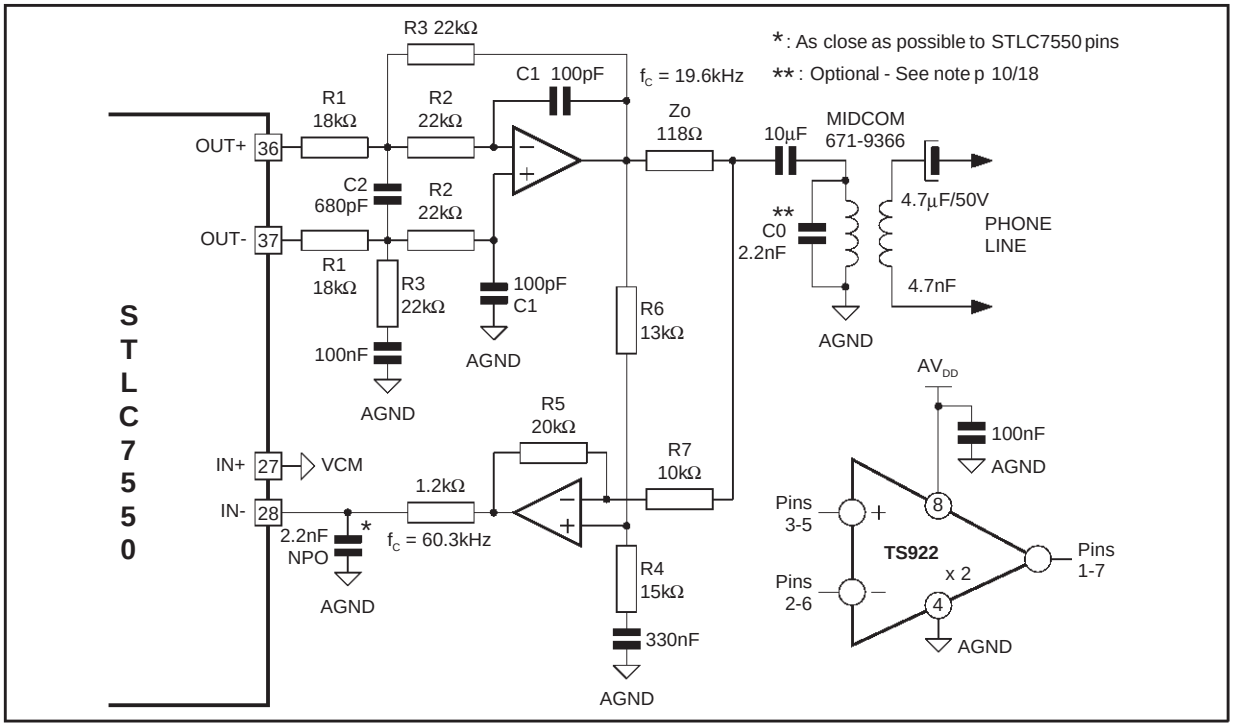
D. Transmit Filter

A_L = $2.2V_{PP}$, m = 0.707
[9] Zline = 600Ω, Z_{EQ} = 484Ω, Z0 = 118Ω, L_T = 0.498
A_C = 2*1.25V (differential codec output),
A_C = $2.5V_{PP}$

[9] $G_T = A_L \cdot m /(A_C \cdot L_T)$ = 1.249 = +1.9 dB
Choosing R3 = 22kΩ, (STLC7549 minimum load is 10kΩ,) gives R1 = 18kΩ, G_T = 1.22 = +1.7dB

[10] $A_C \cdot G_T$ = $3V_{PP}$ Op-Amp are not saturated

Figure 27



VI - LINE INTERFACE (continued)

VI.1.4 - Low Cost DAA for complex impedances

In the previous parts, the phone line impedance Zline has been set to a resistive load of 600Ω (main case). For certain countries, like Germany, Australia, Norway, Sweden, U.K., or in the new european standard TBR21, Zline is considered as a R,R,C network. This part gives an example based on a low cost DAA for TBR21 complex impedance:

$$Z_{TBR21} = 270\Omega + (750\Omega // 150nF)$$

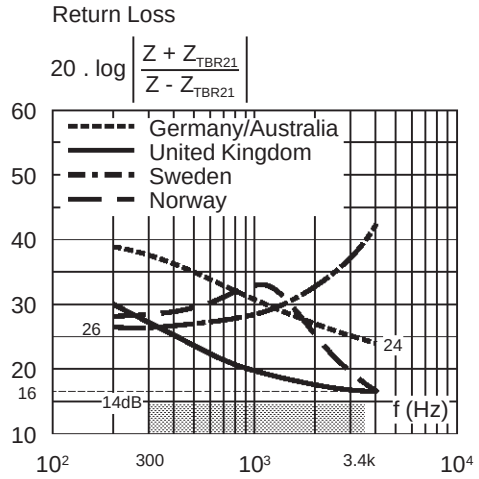
It can used as a universal R, R, C network that match with any complex impedance countries as it provides optimum return loss (Min. 16dB, see Figure 28).

Country $Z = R_{L1} + (R_{L2} // C_L)$	R_{L1} (Ω)	R_{L2} (Ω)	C_L (nF)	Min. Return Loss required (dB)
Germany	220	820	115	18
Australia	220	820	120	14
Norway	120	820	110	9
Sweden	275	850	150	18
United Kingdom	370	620	310	14

Refer to section VI.1.2 for a general description of the low cost DAA.

Switching from real to complex impedances requires to review the impedance matching and the Transmit rejection parts.

Figure 28



A. Phone Line Impedance Matching on a specific complex impedance

Figure 29 shows the equivalent model of a line interface, where Rp and Rs are the transformer resistances, and Zline the phone R,R,C complex impedance. R10, R9, C9 are shown on the DAA schematic given in Figure 30.

Impedances are matching when DAA input impedance (composed of R9,C9,R10,Rs and Rp) is equivalent to line impedance Zline.

It gives :

$R9 = RL2 . m^2$, $C9 = CL/m^2$

$R10 + Rs + Rp.m^2 = RL1.m^2$

Note that the transformer equivalent resistance ($Rs+Rp.m^2$) must be lower or equal to $RL1.m^2$.

Application

This example is targeted for TBR21 impedance:
$R_{L1} = 270\Omega$, $R_{L2} = 750\Omega$, $C_L = 150nF$.

The transformer MIDCOM 671-8332 used in previous schematics present an equivalent resistor ($Rs + Rp . m^2$) too high. It is replaced by a MIDCOM 671-8248 that gives the following performances :

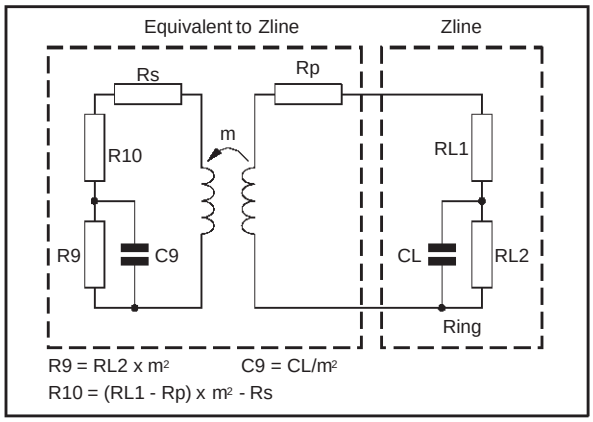
$Rs = 67.5\Omega$, $Rp = 67.5\Omega$, $m=1$

$Rs + Rp . m2 = 135 < RL1$

Then $R9 = 750\Omega$, $R10 = 130\Omega$,
$C9 = 147nF$ (100nF +47nF).

It gives a return loss around 30dB in the whole bandwidth.

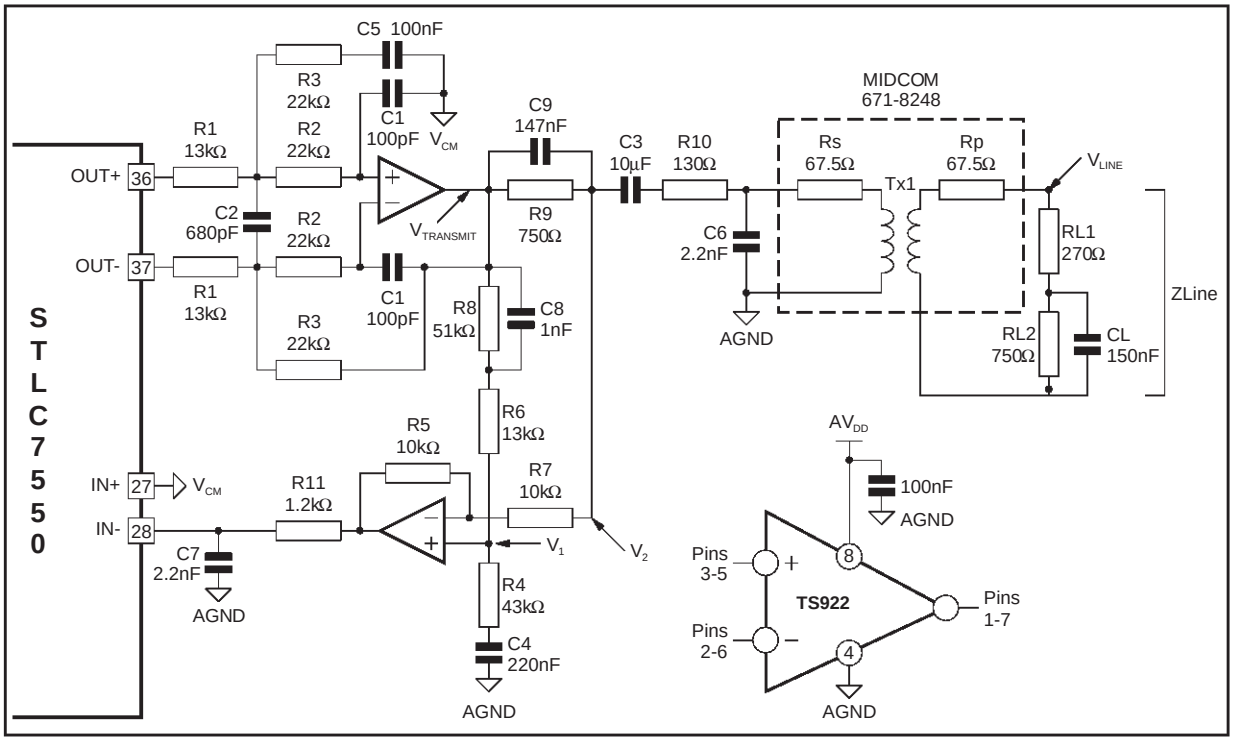
Figure 29



VI - LINE INTERFACE (continued)

VI.1.4 - Low Cost DAA for complex impedances (continued)

Figure 30



B. Transmit Rejection

Transmit rejection performance is directly linked to the line impedance.

With complex impedance lines, Transmit rejection needs to be featured with a complex network (composed of R6,R8,C8 and R4) in order to follow the line impedance move within the whole bandwidth.

R4 is set to a convenient value (R4 = 43kΩ). Note that capacitor C4 becomes critical for a good rejection at low frequencies. It is so interesting to choose R4 high enough to obtain a good R4,C4 cut-off frequency with a low cost C4.

Detailed calculation are given below for any complex impedance value.

In this example, R5 is chosen equal to R7 (R5 = R7 = 10kΩ, refer to the chapter "B. Receive amplifier", page 15). Transmit rejection is achieved when V1 = 1/2 · V2 in the whole bandwidth.

- at high frequencies, R9, RL2 and R8 have no influence (shunted by capacitors C9, CL and C8). Taking R9 = RL2 = R8 = 0, it gives V2 = Vtransmit and then V1 = 1/2 Vtransmit. Then R6 = R4 = 43kΩ.
- at low frequencies, C9, CL and C8 have no influence. Transmit rejection can be calculated considering only resistors.

$$\frac{V2}{V_{Transmit}} = \frac{R10 + Rs + (Rp + RL1 + RL2) \cdot m^2}{R9 + R10 + Rs + (Rp + RL1 + RL2) \cdot m^2}$$

$$= \frac{RL1 + RL2/2}{RL1 + RL2} = 0.632$$

$$V1 = \frac{1}{2} \cdot V2 = 0.316$$

$$R8 + R6 = \frac{1 - 0.316}{0.316} \cdot R4 = 93k\Omega$$

R8 = 93kΩ, R6 = 51kΩ

Values should be certified at 1% for good performances.

$$C8 = \frac{RL1 \cdot RL2}{(RL1 + RL2/2) \cdot R8} \cdot CL = 923pF$$

We take C8 = 1nF.

Note : capacitor C9 and related resistors constitute a low-pass filter for phone line incoming signals. We have to check that its cut-off frequency is outside the bandwidth :

$$fc9 = \frac{R9 + Req}{2\pi \cdot R9 \cdot Req \cdot C9}$$

with Req = R10 + Rs + m^2 . Rp

fc9 = 5.3kHz, then the low-pass filter has no effect in the bandwidth.

VI - LINE INTERFACE (continued)

Experimental measures gives an electrical receive echo in the same range (+3dB higher) than for 600Ω lines (refer to Figure 46, page 27).

Detailed Calculation *(see Figure 31)*

Transmit rejection is achieved when

$$V1 = \frac{R5}{R7 + R5} \cdot V2 \quad [1]$$

$$\frac{V2}{V_{Transmit}} = Al \cdot \frac{1 + j\frac{\omega}{\omega l1}}{1 + j\frac{\omega}{\omega l2}}$$

$$\text{with } Al = \frac{RL1 + RL2/2}{RL1 + RL2}$$

$$\omega l1 = \frac{RL1 + RL2/2}{RL1 \cdot RL2 \cdot CL}, \ \omega l2 = \frac{RL1 + RL2}{RL1 \cdot RL2 \cdot CL}$$

$$\omega l1 < \omega l2$$

$$\frac{V1}{V_{Transmit}} = Ar \cdot \frac{1 + j\frac{\omega}{\omega r1}}{1 + j\frac{\omega}{\omega r2}}$$

$$\text{with } Ar = \frac{R4}{R4 + R8 + R6}$$

$$\omega r1 = \frac{1}{R8 \cdot C8}, \ \omega r2 = \frac{R4 + R6 + R8}{R8 \cdot (R4 + R6) \cdot C8}$$

$$\omega r1 < \omega r2$$

Solving equation [1] , gives

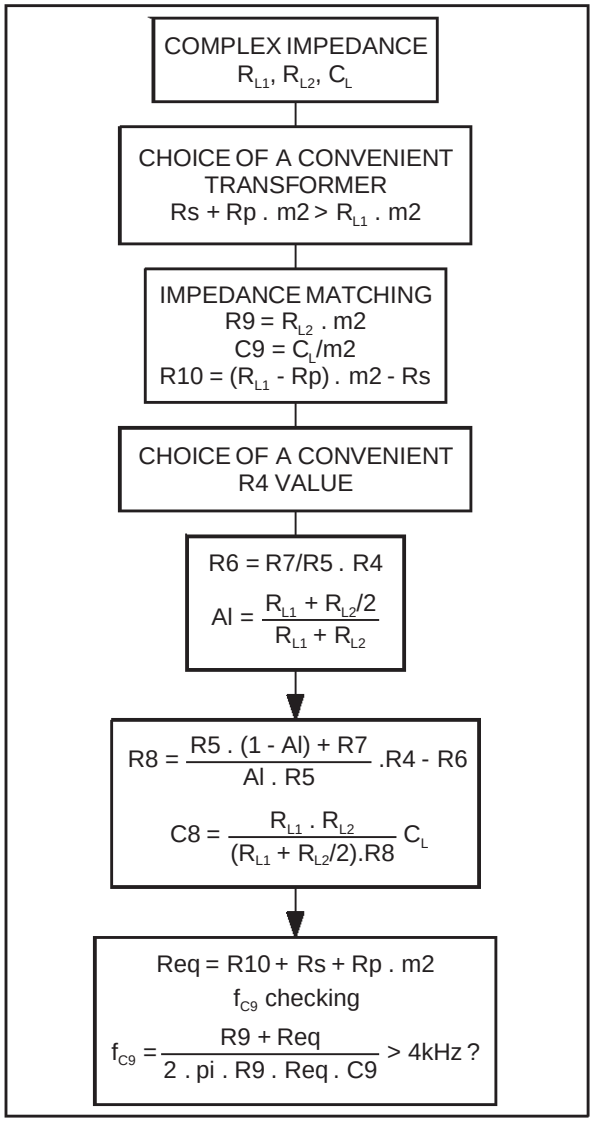
$$Ar = \frac{R5}{R5 + R7} \cdot Al \quad \text{with } \omega r1 = \omega l1 \text{ and } \omega r2 = \omega l2$$

It gives the following component values

$$R6 + R8 = \frac{R5 \cdot (1 - Al) + R7}{Al \cdot R5} \cdot R4, \ R6 = \frac{R7}{R5} \cdot R4$$

$$C8 = \frac{RL1 \cdot RL2}{(RL1 + RL2/2) \cdot R8} \cdot CL$$

Figure 31



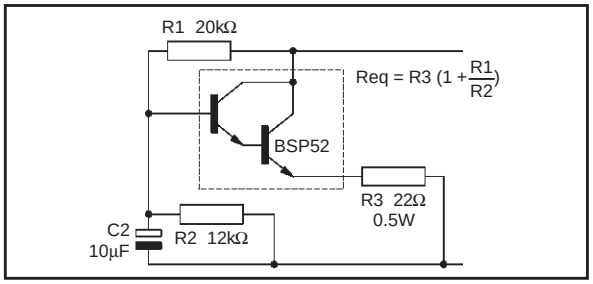
VI - LINE INTERFACE (continued)

VI.2 - Current Driver

The current driver block provides the DC current required to maintain the line in a off-hook condition. It must provide a high AC impedance to avoid attenuating the phone signals. This is achieved by using a darlington device or 2 NPN transistors that looks resistive for DC current and gives a high AC impedance across Tip and Ring within the voice band.
DC current is fixed by the equivalent resistor R_{EQ}, depending on the phone line characteristics of the country to which the modem is dedicated (Minimum current required, maximum current and line voltage).

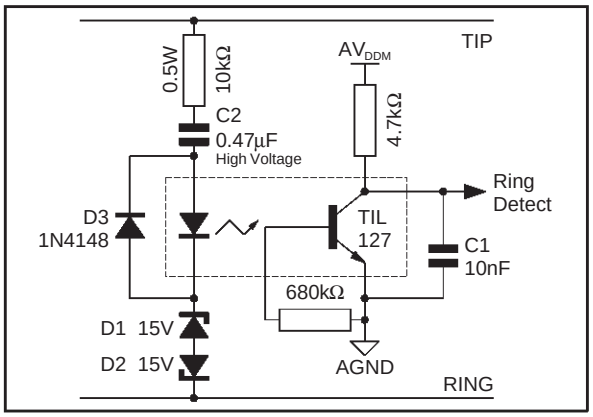
Application : $R_{EQ} = 58\Omega$

Figure 32 : Current Driver Block



VI.2.1 - Ring Detect (see Figure 33)

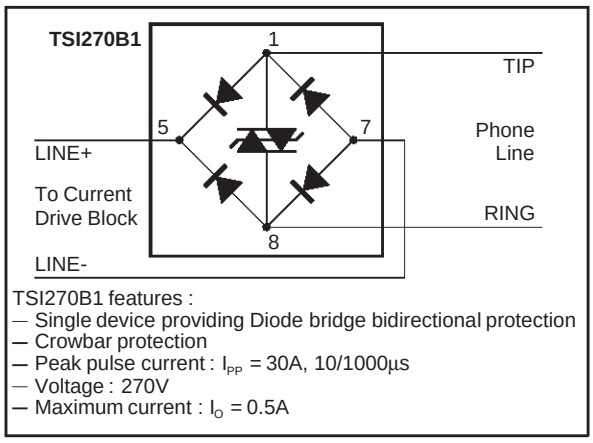
Figure 33 : Ring Detect



VI.2.2 - Protection Devices

The bridge protects modem against Tip and Ring inverting. The protection block is varistors that protect modem against spikes (e.g. lightning). The two protection devices are included in a unique component TSI270B1. The connections are shown on Figure 34.

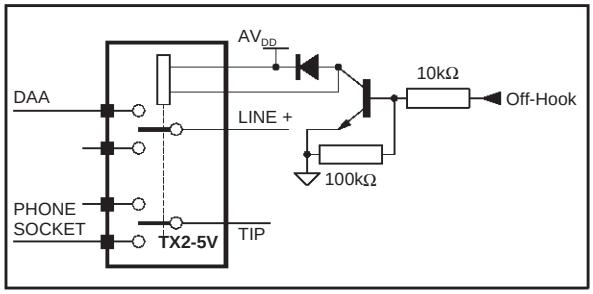
Figure 34 : Modem Protection



VI.2.3 - Hook switch

The hook switch connects the PSTN to the DAA or to the phone socket.
To answer an incoming call, the system needs to make the connection on the PSTN after a ringing unit. The diode is used to bypass current peak at the hook switch pins during switching.

Figure 35 : Hook Switch



VII - APPLICATION

Figure 36 : Low Power Host Processing Modem Application using STLC7550.

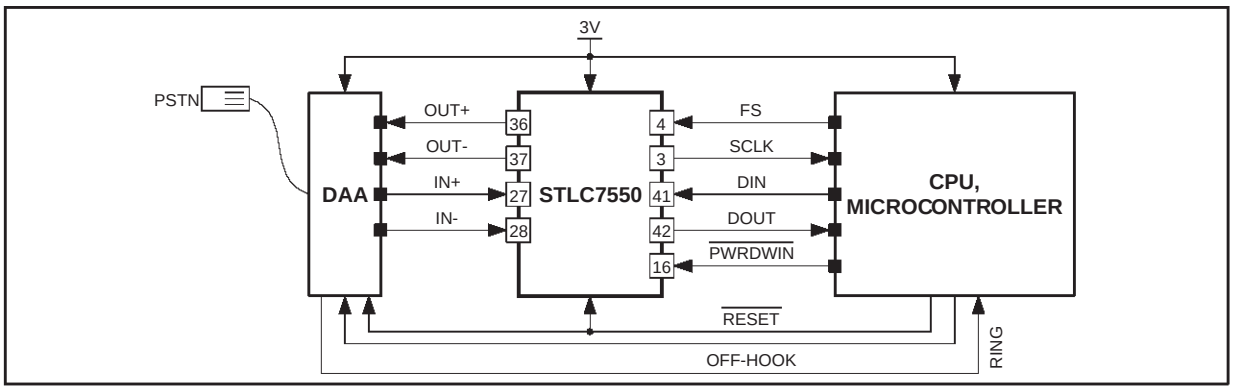
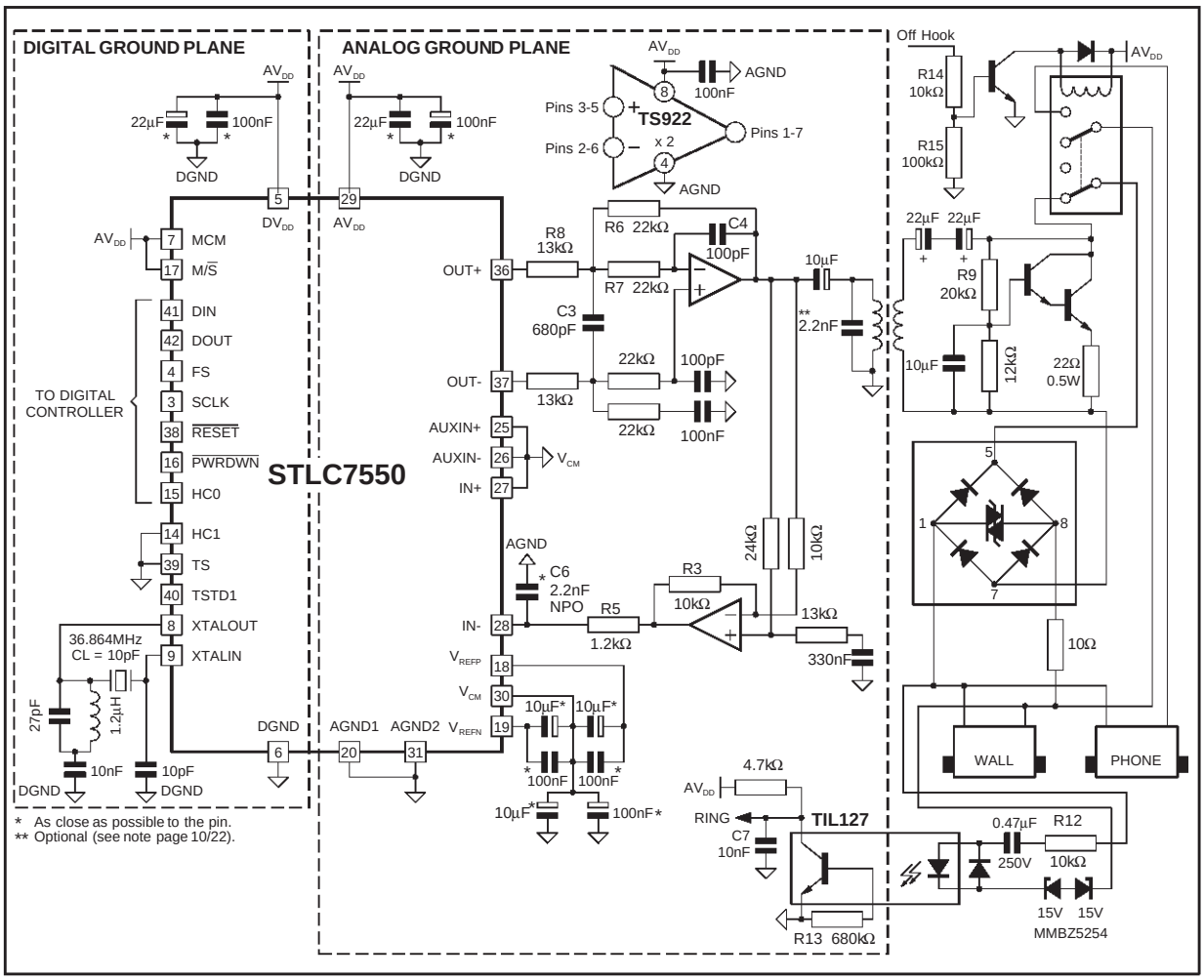


Figure 37 : Appendix : Suggested Implementation



VIII - PERFORMANCES

The measurements have been performed with a RODHE & SCHWARZ Audio Analyzer 2Hz-300kHz UPD. The sampling frequency is 9.6kHz and oversampling ratio is 160.

VIII.1 - ADC Converter

The SNDR measured is 83dB for a signal level equal to -3dBr (see Figure 38).
Figure 39 gives the SNDR for the analog to digital/digital to analog loop back. We can see that the SNDR is 78dB at -6dBr and this value is 80dB at -3dBr.
In this configuration the noise power of the ADC and the DAC are added conducting to a +3dB noise power increase. So it means that both ADC and DAC present a SNDR to 83dB for a -3dBr signal level.

Dynamic Range : DR

The measurement result is 87.5dB for a signal level equal to -20dBFs (0.0884V_{RMS}) (see Figure 40).

The DR Figure is dependant on the oversampling ratio and the supply voltage : see below table.

		V_{DD}	
		3V	**5V**
Over	**64**	80dB	78dB
	160	87.5dB	85dB

Total Harmonic Distortion

The THD measured with a -6dBFs signal level is 93dB (see Figure 41).

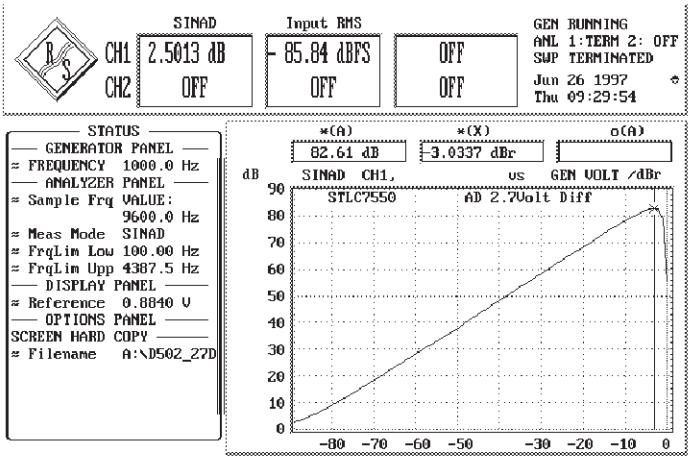
Offset

ADC offset is specified within the range ±300LSB. It is recommended to perform offset cancellation at the DSP side.

VIII.2 - DAC Converter

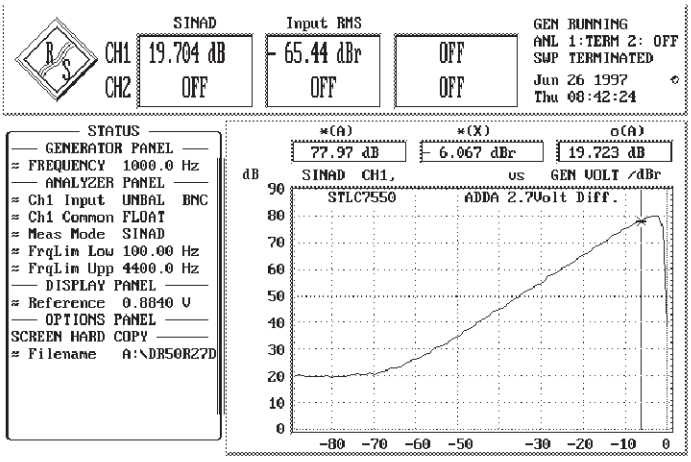
Figure 42 gives the measurement result of the dynamic range. The signal level is -20dBr. Dynamic range extrapolated to full range is 87dB.
The total harmonic distortion (harmonic frequencies in the band 100Hz-4080Hz) is equal to -94dB (see Figure 43).

Figure 38 : Signal to Noise Ratio : ADC



AN930-38.PCX

Figure 39 : Signal to Noise Ratio : ADC + DAC



AN930-39.PCX

VIII - PERFORMANCES (continued)

Figure 40 : Dynamic Range. Supply = 3V, Oversampling Ratio = 160.

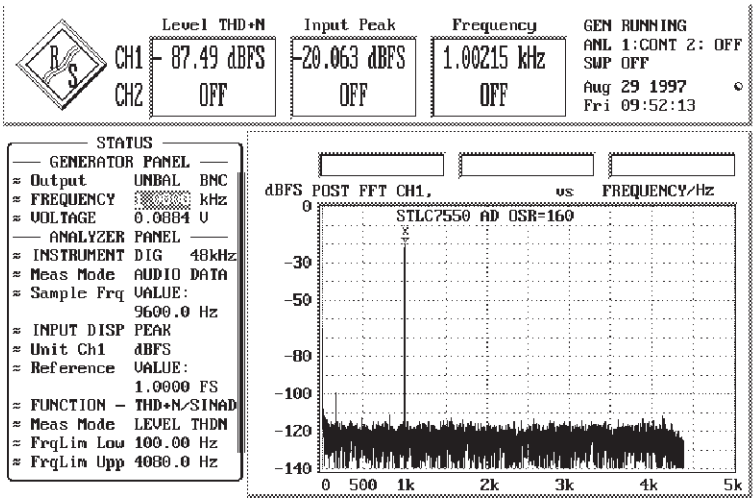


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Figure 41 : Total Harmonic Distortion

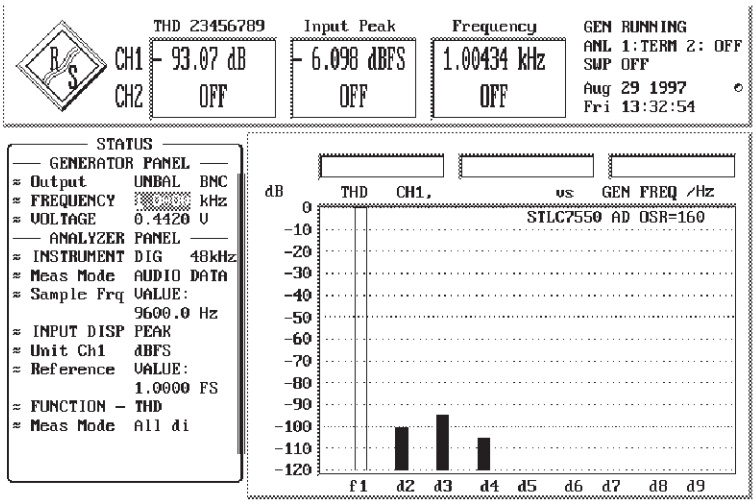

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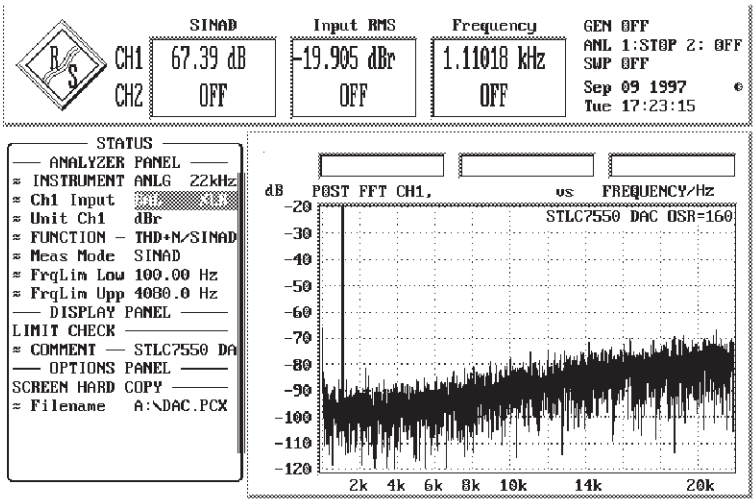
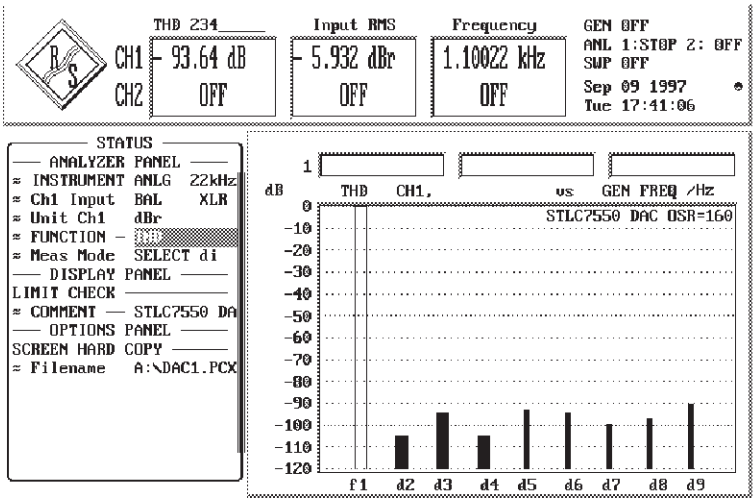
Figure 42 : DAC (DR = 87dB, level = -20dBr)



AN930-42.PCX

VIII - PERFORMANCES (continued)

Figure 43 : DAC (THD = -93dB, level = -6dBr)



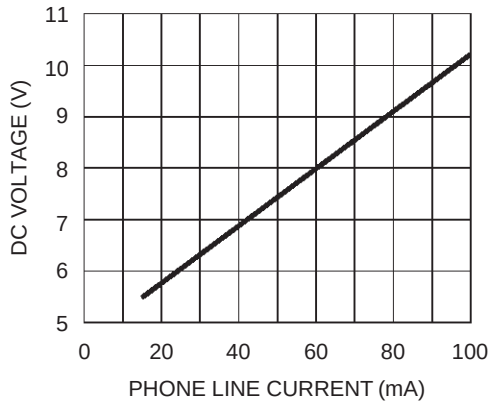
AN930-43.PCX

VIII.3 - DAA Characteristics

DC Mask

Figure 44 gives the TIP and ring voltage versus the line current. The slope and the absolute voltage are managed with the resistor R1, R2 and R3 (see Figure 32) in order to fulfill the different countries regulation.

Figure 44



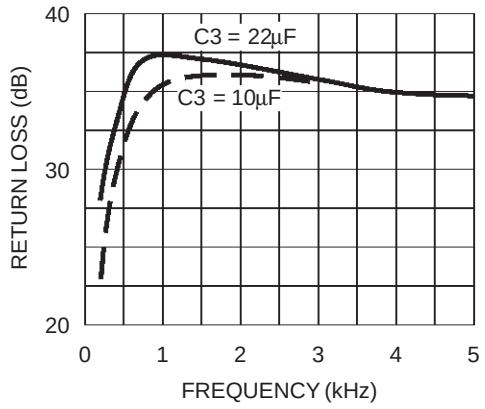
AN930-44.EPS

Return Loss

Figure 45 gives the 600Ω impedance matching in single ended configuration. The low frequency response is significantly dependant on the C3 capacitor value (see Figure 23).

The return loss figure is stable over a 15 to 120mA line current range.

Figure 45



AN930-45.EPS

VIII - PERFORMANCES (continued)

Electrical Receive Echo

(single ended duplexer mode)

Figure 46 gives signal levels at different successive points of the transmit channel. The signal level at the transmit STLC7550 outputs is -6dBr (0dBr = 2.5V_{PP}).

The external duplexer transmit gain (+4.6dB) compensates part of the transformer stage losses and lead to a global attenuation from the STLC7550 and the line of about -2dB.

The electrical echo is measured at the IN+/- inputs for a 600Ω resistive line impedance. The two plots corresponding to different C4 (see Figure 22) capacitor values show the low frequency rejection difference.

Figure 46 : Transmit Single Ended Mode