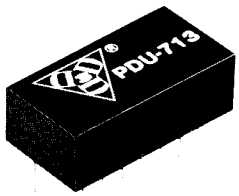
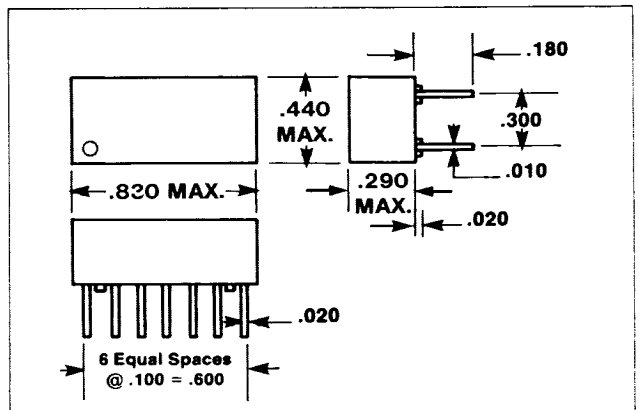
Programmable Delay Units

SERIES: PDU-713

T²L Interfaced (3 BIT)

data delay devices, inc.



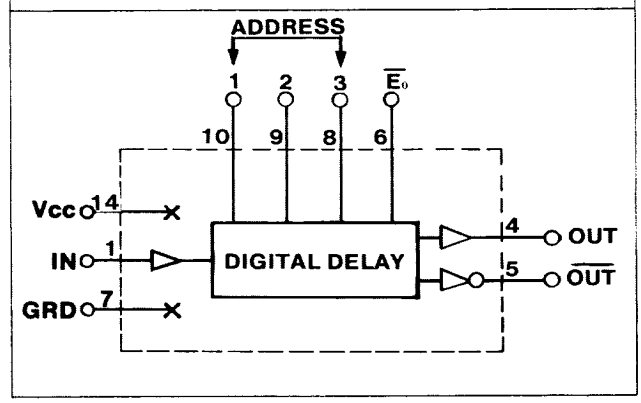


Features:

- Digitally programmable in 8 delay steps.
- Fits standard 14 pins DIP socket.
- Input & outputs fully TTL interfaced & buffered.
- Two (2) separate outputs; inverting & non-inverting.
- Precise and stable delays.
- 10 T²L fan-out capability

Specifications:

- **Input signal requirement:** TTL logic.
- **Output fan-out:** TTL Schottky loads.
- **Delay variation:** Monotonic in one direction.
- **Total programmed delay tolerance:** 5% or 1 NS whichever is greater.
- **Inherent delay (T_{DO}):** 14 NS on pin 4, 11 NS on pin 5 } typical
- **Propagation delay:**
  Address to output (T_{SUA}) = 12 NS typ.
  Enable to output (T_{SUE}) = 12 NS typ.
- **Operating temperature:** 0° to 70°C.
- **Temperature coefficient:** 100 PPM/°C.
- **Supply voltage Vcc:** 5 VDC ± 5%.
- **Power dissipation:** 740 MW max.



TRUTH TABLE

Enable	Address (Bit No.) 3	2	1	Delay Out
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	1	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1	ϕ	ϕ	ϕ	0

1 = High
0 = Low
ϕ = Don't care
T_0 = Reference or inherent delay of circuit.
T_1 to T_7 = Multiplier of incremental delay.

Part Number	Incremental Delay Per Step	Total Delay* Change
PDU-713-.5	.5 NS ± .3 NS	3.5 NS
PDU-713-1	1 NS ± .4 NS	7 NS
PDU-713-2	2 NS ± .4 NS	14 NS
PDU-713-3	3 NS ± .5 NS	21 NS
PDU-713-5	5 NS ± .6 NS	35 NS
PDU-713-10	10 NS ± 1.0 NS	70 NS
PDU-713-15	15 NS ± 1.3 NS	105 NS
PDU-713-20	20 NS ± 1.5 NS	140 NS
PDU-713-40	40 NS ± 2.0 NS	280 NS
PDU-713-50	50 NS ± 2.5 NS	350 NS

*This delay value does not include T_0 delay.

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