

HB56A49 Series

4,194,304-Word x 9-Bit High Density Dynamic RAM Module

DESCRIPTION

The HB56A49 is a 4M x 9 dynamic RAM module, mounted 9 pieces of 4 Mbit DRAM (HM514100AS, HM514100JP) sealed in an SOJ package. An outline of the HB56A49 is the 30-pin single in-line package. Therefore, the HB56A49 makes high density mounting possible without surface mount technology. The HB56A49 provides common data inputs and outputs, and also provides separate I/O parity bit for parity check. Decoupling capacitors are mounted beneath each SOJ.

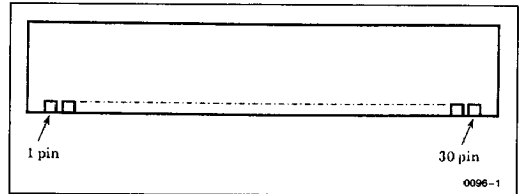
FEATURES

- 30-pin Single In-line Package
Lead Pitch 2.54mm
- Single 5V ($\pm 10\%$) Supply
- High Speed
Access Time 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
Active Mode 5445 mW/4059 mW/4455 mW/
3960 mW (max)
Standby Mode 99 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle (16 ms)
- 3 Variations of Refresh
RAS Only Refresh
CAS Before RAS Refresh
- Hidden Refresh

PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₁₀	Address Input
A ₀ -A ₉	Refresh Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$, $\overline{\text{PCAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Enable
DQ ₀ -DQ ₇	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V _{CC}	Power Supply (+ 5V)
V _{SS}	Ground
NC	No Connection

PIN OUT



Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	16	DQ ₄
2	$\overline{\text{CAS}}$	17	A ₈
3	DQ ₀	18	A ₉
4	A ₀	19	A ₁₀
5	A ₁	20	DQ ₅
6	DQ ₁	21	$\overline{\text{WE}}$
7	A ₂	22	V _{SS}
8	A ₃	23	DQ ₆
9	V _{SS}	24	NC
10	DQ ₂	25	DQ ₇
11	A ₄	26	PQ
12	A ₅	27	$\overline{\text{RAS}}$
13	DQ ₃	28	$\overline{\text{PCAS}}$
14	A ₆	29	PD
15	A ₇	30	V _{CC}

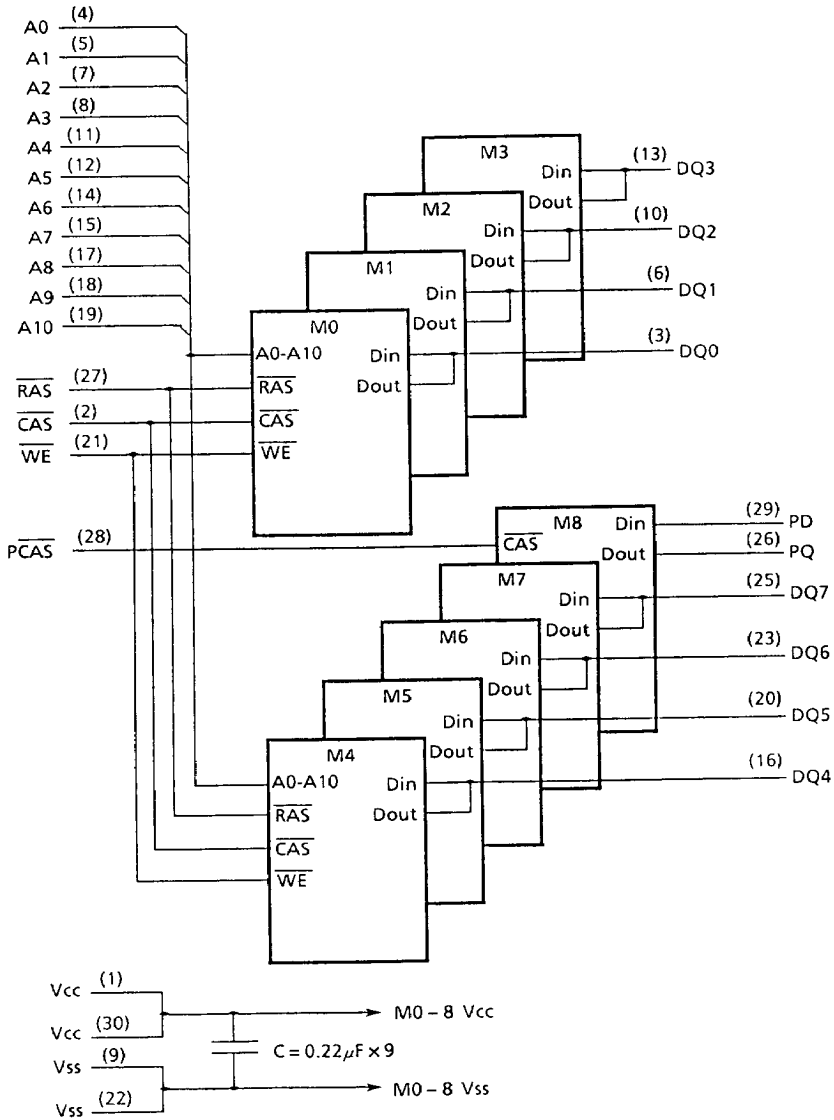
ORDERING INFORMATION

Access Time	Package					
	30-pin ¹ SIP Socket Type	30-pin ¹ SIP Socket Type	30-pin SIP Lead Type	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIP Low Profile Lead Type
	0.945 Inch Height	0.805 Inch Height	0.989 Inch Height	0.810 Inch Height	0.591 Inch Height	0.500 Inch Height
60 ns	—	HB56A49BR/GBR-6A	—	HB56A49AR-6A	—	HB56A49ATR-6A
70 ns	—	HB56A49BR/GBR-7A	—	HB56A49AR-7A	—	HB56A49ATR-7A
80 ns	HB56A49B/GB-8	HB56A49BR/GBR-8A	HB56A49A-8	HB56A49AR-8A	HB56A49AT-8	HB56A49ATR-8A
100 ns	HB56A49B/GB-10	HB56A49BR/GBR-10A	HB56A49A-10	HB56A49AR-10A	HB56A49AT-10	HB56A49ATR-10A

Note: 1. Following the specification of the contact pad.
 HB56A49B-XX, HB56A49BR-XX: solder
 HB56A49GB-XX, HB56A49GBR-XX: gold



■ BLOCK DIAGRAM



Note: M0-M8[HB56A49XX-XXA]: HM514100AS
 M0-M8[HB56A49XX-8/10]: HM514100JP

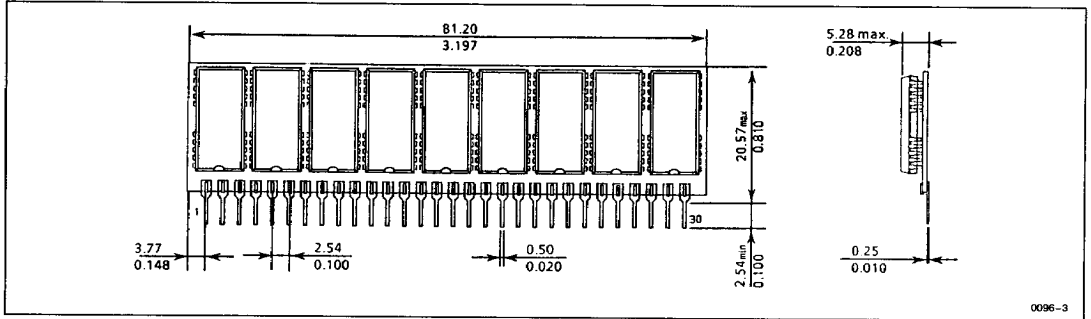
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■ PHYSICAL OUTLINE

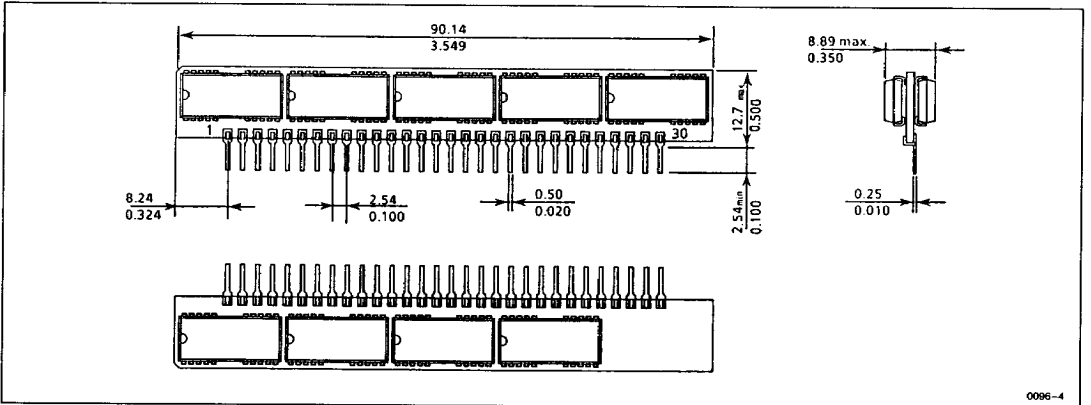
Unit: mm
inch

• HB56A49AR Series



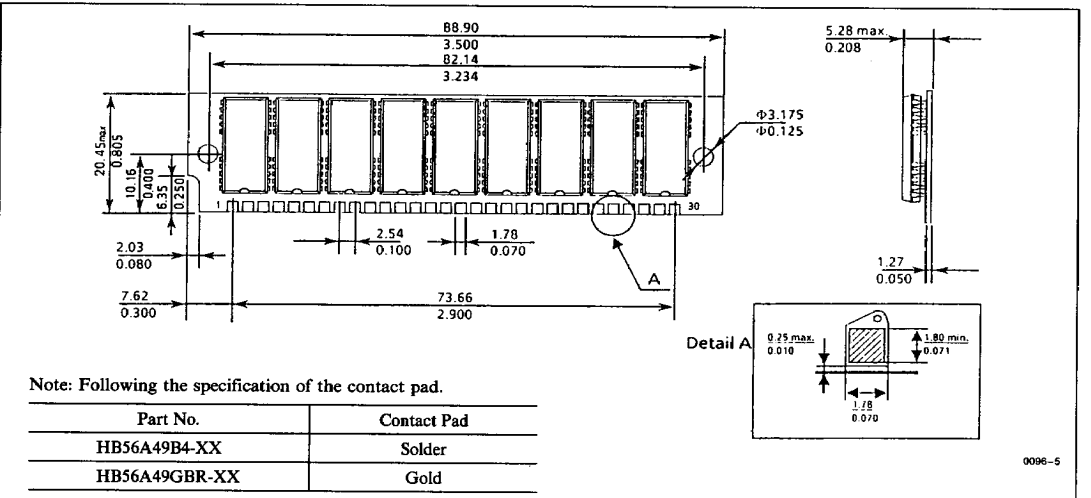
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• HB56A49ATR Series



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• HB56A49BR/GBR Series



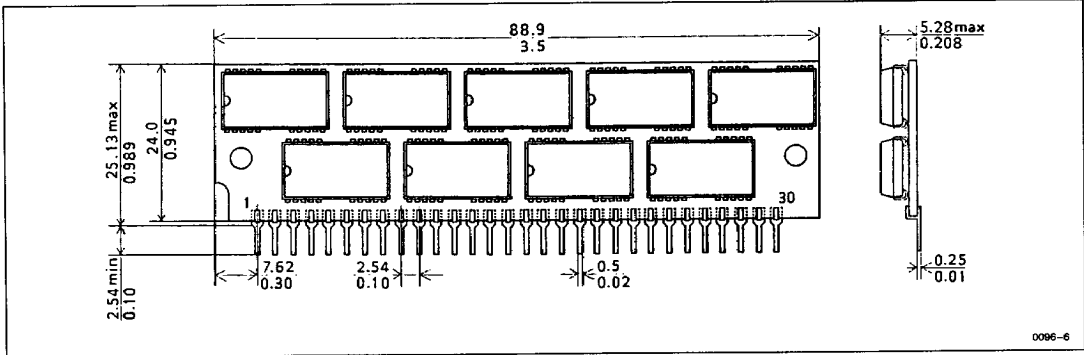
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Part No.	Contact Pad
HB56A49B4-XX	Solder
HB56A49GBR-XX	Gold



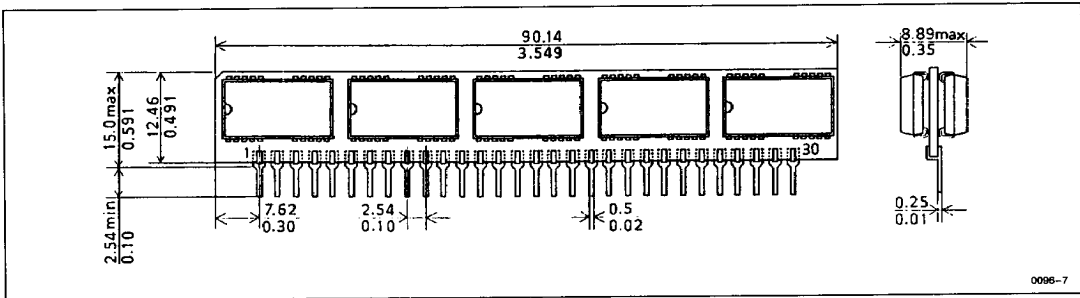
Unit: mm
inch

• HB56A49A Series



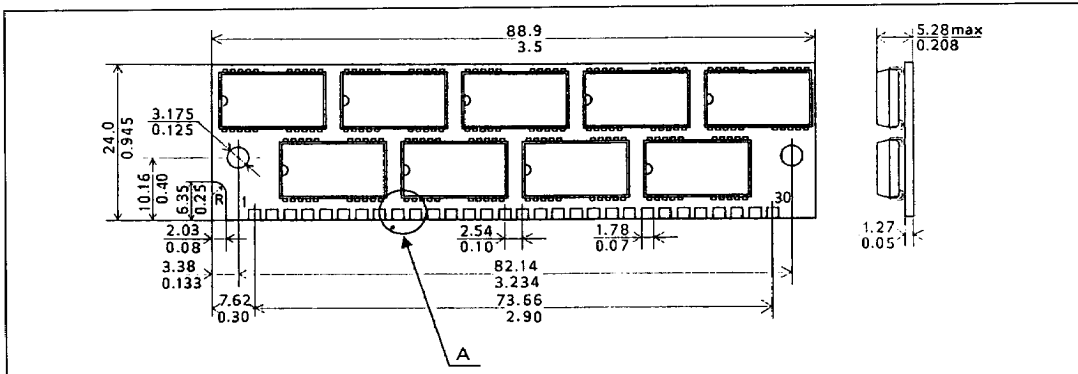
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• HB56A49AT Series



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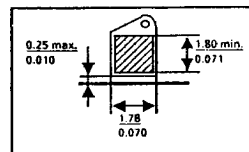
• HB56A49B/GB Series



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Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A49B-XX	Solder
HB56A49GB-XX	Gold



Detail A

0096-9



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	- 1.0 to + 7.0	V
Supply Voltage Relative to V _{SS}	V _{CC}	- 1.0 to + 7.0	V
Short Circuit Output Current	I _{out}	50	mA
Power Dissipation	P _T	9	W
Operating Temperature	T _{opr}	0 to + 70	°C
Storage Temperature	T _{stg}	- 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V _{SS}	0	0	0	V	
	V _{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V _{IH}	2.4	—	5.5	V	1
Input Low Voltage	V _{IL}	- 0.5	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR								Unit	Test Condition	Note
		-6A		-7A		-8/-8A		-10/-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I _{CC1}	—	990	—	900	—	810	—	720	mA	t _{RC} = Min	1, 2
Standby Current	I _{CC2}	—	18	—	18	—	18	—	18	mA	TTL Interface R _{AS} , C _{AS} = V _{IH} D _{out} = High-Z	
		—	9	—	9	—	9	—	9	mA	CMOS Interface R _{AS} , C _{AS} ≥ V _{CC} - 0.2V D _{out} = High-Z	
R _{AS} Only Refresh Current	I _{CC3}	—	990	—	900	—	810	—	720	mA	t _{RC} = Min	2
Standby Current	I _{CC5}	—	45	—	45	—	45	—	45	mA	R _{AS} = V _{IH} C _{AS} = V _{IL} D _{out} = Enable	1
C _{AS} Before R _{AS} Refresh Current	I _{CC6}	—	990	—	900	—	810	—	720	mA	t _{RC} = Min	
Page Mode Current	I _{CC7}	—	990	—	900	—	810	—	720	mA	t _{PC} = Min	1, 3
Input Leakage Current	I _{L1}	- 10	10	- 10	10	- 10	10	- 10	10	μA	0V ≤ V _{IN} ≤ 7V	
Output Leakage Current	I _{L0}	- 10	10	- 10	10	- 10	10	- 10	10	μA	0V ≤ V _{out} ≤ 7V D _{out} = Disable	
Output High Voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	I _{out} = - 5 mA	
Output Low Voltage	V _{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I _{out} = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Address can be changed less than three times while R_{AS} = V_{IL}.
 3. Address can be changed once or less while C_{AS} = V_{IH}.



• Capacitance (T_A = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	HB56A49				Unit	Note
		BR/GBR/AR/ATR		A/AT/B/GB			
		Typ	Max	Typ	Max		
Input Capacitance (Address)	C _{I1}	—	60	—	70	pF	1
Input Capacitance (Clock)	C _{I2}	—	75	—	88	pF	1
Input Capacitance (PCAS)	C _{I3}	—	12	—	20	pF	1
Input/Output Capacitance (DQ ₀₋₇)	C _{L/O}	—	17	-	30	pF	1, 2
Input Capacitance (PD)	C _{I4}	—	10	—	20	pF	1
Output Capacitance (PQ)	C _O	—	12	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. CAS = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)^{1, 12, 15}

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR											Unit	Note	
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min			Max
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	150	—	180	—	150	—	180	—	ns	
RAS Precharge Time	t _{RP}	40	—	50	—	60	—	70	—	60	—	70	—	ns	
RAS Pulse Width	t _{RAS}	60	10000	70	10000	80	10000	100	10000	80	10000	100	10000	ns	
CAS Pulse Width	t _{CAS}	15	10000	20	10000	20	10000	25	10000	20	10000	25	10000	ns	
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	15	—	10	—	15	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
RAS to CAS Delay Time	t _{RCD}	20	50	20	50	20	60	25	75	20	60	25	75	ns	8
RAS to Column Address Delay Time	t _{RAD}	15	35	15	35	15	40	20	55	15	40	20	55	ns	9
RAS Hold Time	t _{RSH}	15	—	20	—	20	—	25	—	20	—	25	—	ns	
CAS Hold Time	t _{CSH}	60	—	70	—	80	—	100	—	80	—	100	—	ns	
CAS to RAS Precharge Time	t _{CRP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t _{REF}	—	16	—	16	—	16	—	16	—	16	—	16	ms	17

Read Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR											Unit	Note	
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min			Max
Access Time from RAS	t _{RAC}	—	60	—	70	—	80	—	100	—	80	—	100	ns	2, 3, 16
Access Time from CAS	t _{CAC}	—	15	—	20	—	20	—	25	—	25	—	25	ns	3, 4, 14
Access Time from Address	t _{AA}	—	30	—	35	—	40	—	45	—	40	—	45	ns	3, 5, 14, 16
Read Command Setup Time	t _{RCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	



Read Cycle (continued)

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Command Hold Time to CAS	t _{RCH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to RAS	t _{RRH}	0	—	0	—	0	—	0	—	10	—	10	—	ns	
Column Address to RAS Lead Time	t _{RAL}	30	—	35	—	40	—	45	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t _{OFF}	0	15	0	20	0	20	0	25	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	10	—	20	—	15	—	20	—	ns	
Write Command to RAS Lead Time	t _{RWL}	15	—	20	—	20	—	25	—	25	—	25	—	ns	
Write Command to CAS Lead Time	t _{CWL}	15	—	20	—	20	—	25	—	25	—	25	—	ns	
Data-in Setup Time	t _{DS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CAS Setup Time (CAS Before RAS Refresh Cycle)	t _{CSR}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh Cycle)	t _{CHR}	10	—	10	—	10	—	10	—	20	—	20	—	ns	
RAS Precharge to CAS Hold Time	t _{RPC}	10	—	10	—	10	—	10	—	10	—	10	—	ns	



Fast Page Mode Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	55	—	55	—	ns	
Fast Page Mode CAS Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Fast Page Mode RAS Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from CAS Precharge	t_{ACP}	—	35	—	40	—	45	—	50	—	50	—	50	ns	14, 16
RAS Hold Time from CAS Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	50	—	50	—	ns	

Test Mode Cycle

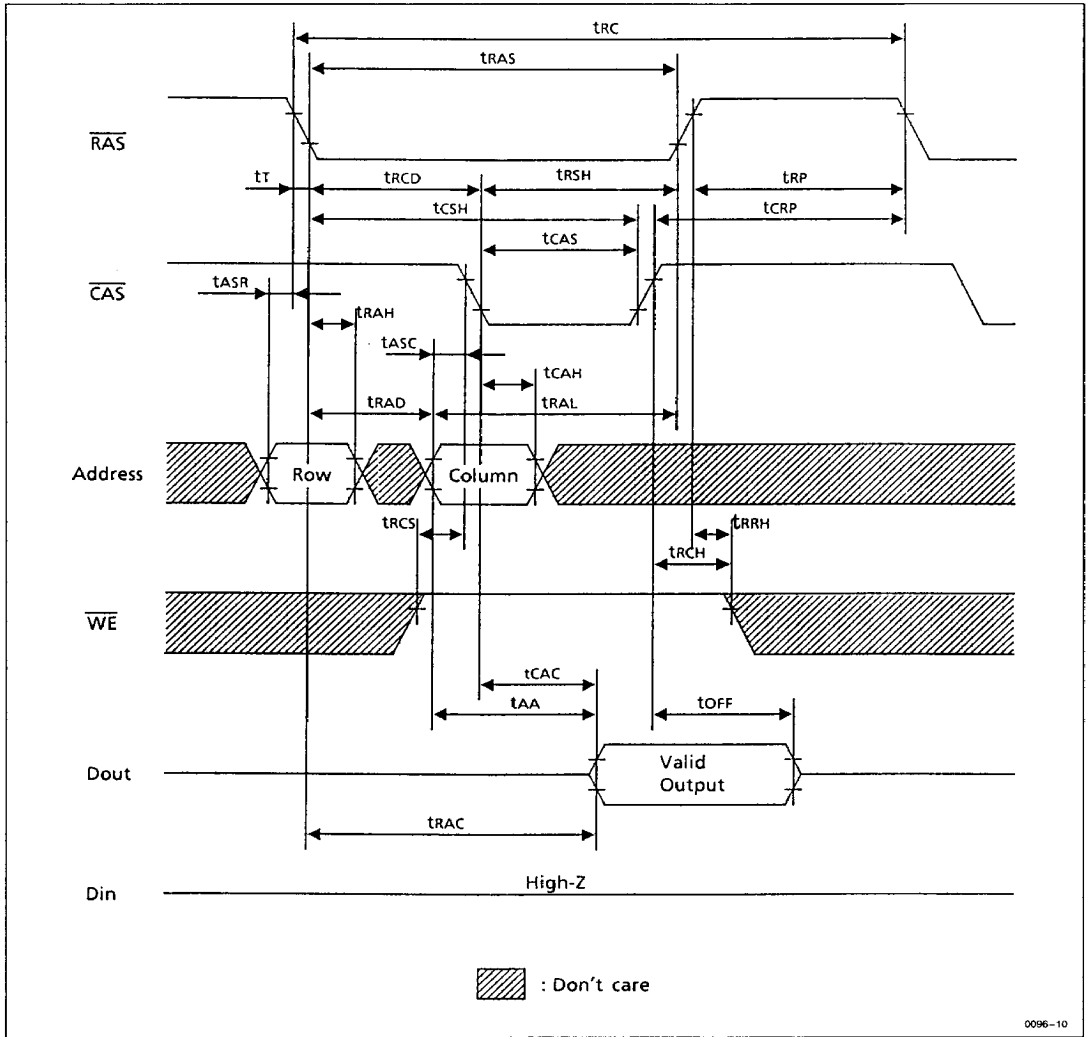
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		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode \overline{WE} Setup Time	t_{WS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Test Mode \overline{WE} Hold Time	t_{WH}	10	—	10	—	10	—	10	—	20	—	20	—	ns	

- Notes:
- AC measurements assume $t_T = 5$ ns.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 - Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$, $t_{RAD} \leq t_{RAD}(\text{max})$.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$, $t_{RAD} \geq t_{RAD}(\text{max})$.
 - $t_{OFF}(\text{max})$ is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 - $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 - Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 - Early write cycle only ($t_{WCS} \geq t_{WCS}(\text{min})$).
 - These parameters are referenced to CAS leading edge in an early write cycle.
 - An initial pause of 100 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS clock such as RAS only refresh).
 - t_{RASC} is determined by RAS pulse width in fast page mode cycles.
 - Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP} .
 - Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits . . . RA10, CA10 and CA0. This test mode operation can be performed by WE and CAS before RAS (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in} . In order to end this test mode operation, perform a RAS only refresh cycle or a CAS before RAS refresh cycle.
 - In a test mode read cycle, the value of t_{RAC} , t_{AA} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
 - t_{REF} is determined by 1,024 refresh cycles.

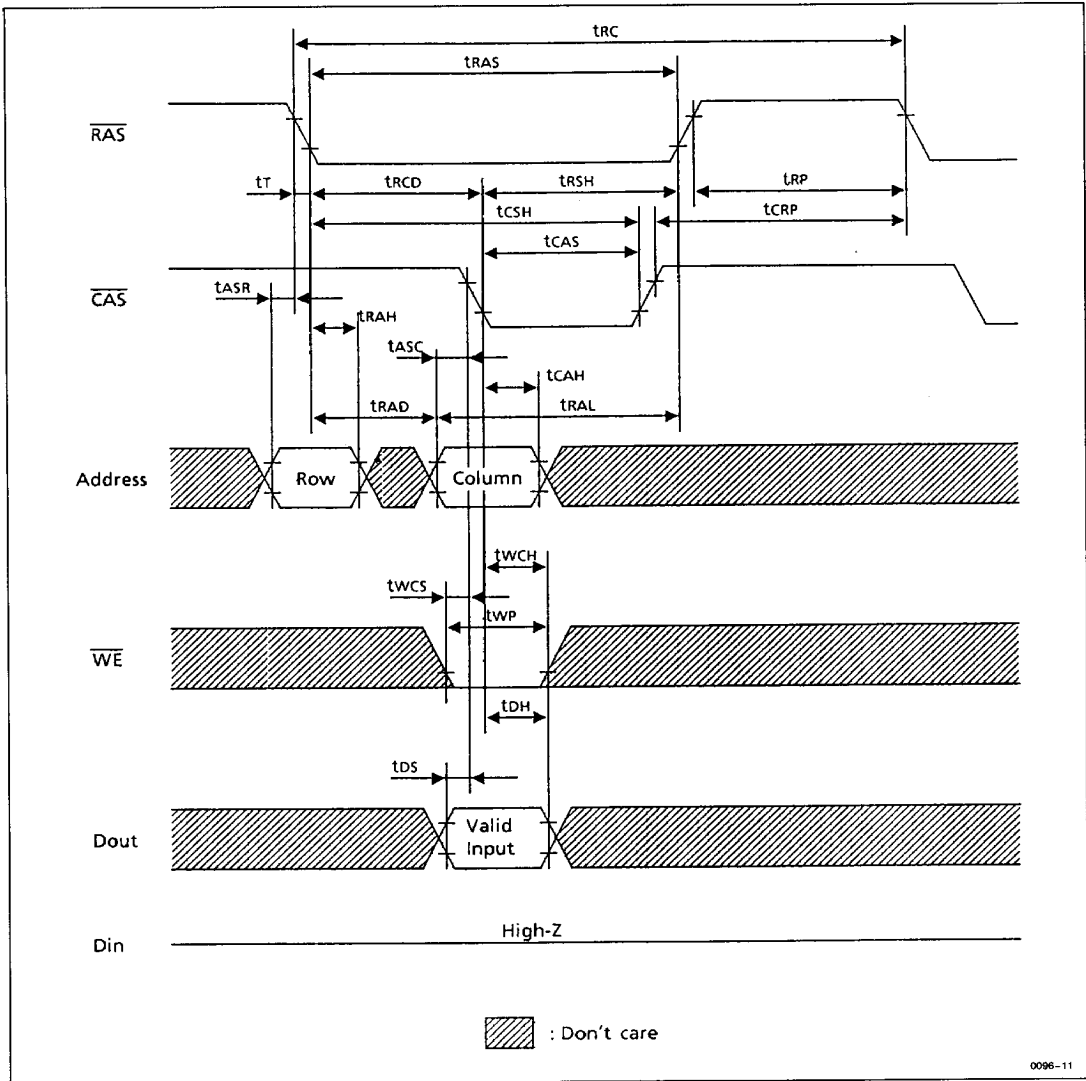


■ TIMING WAVEFORM

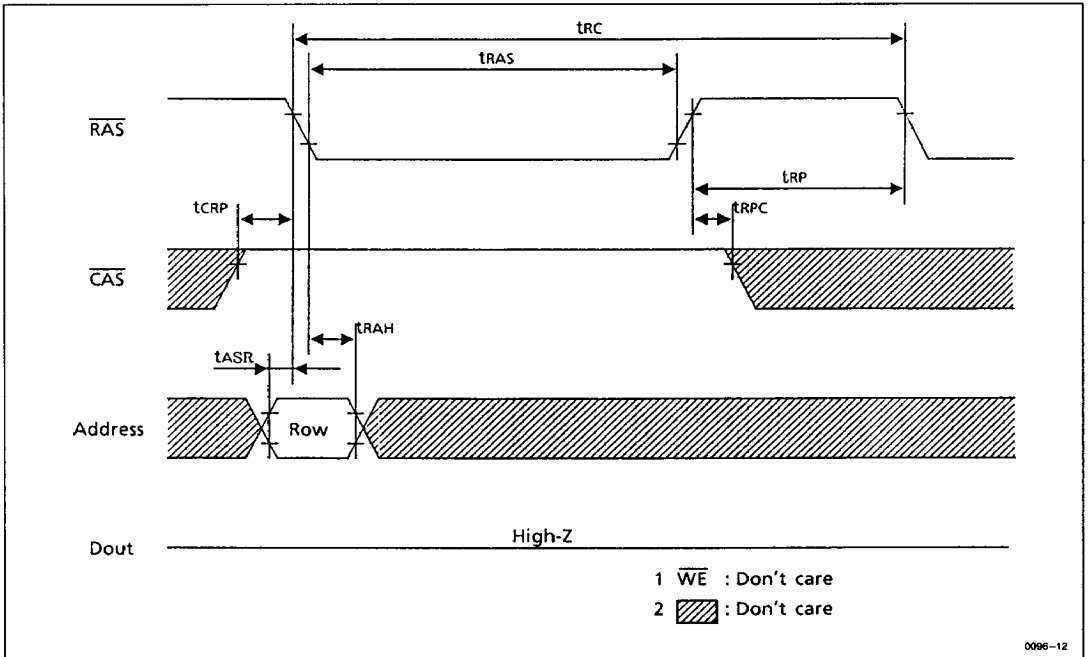
• Read Cycle



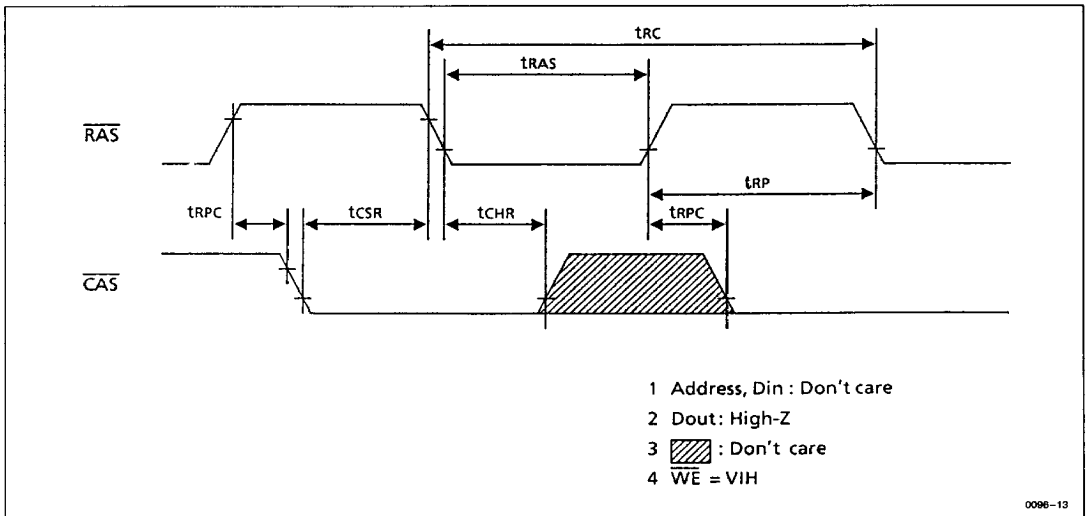
• Early Write Cycle



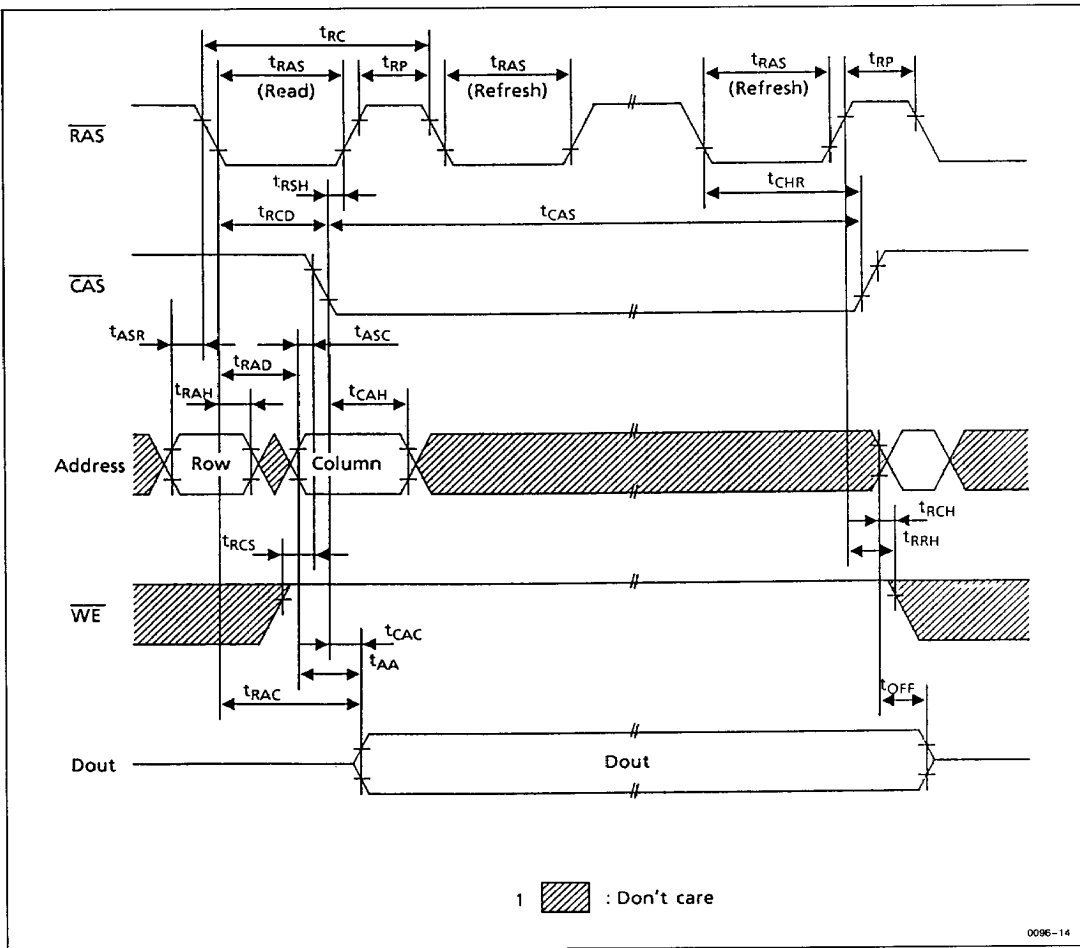
• $\overline{\text{RAS}}$ Only Refresh Cycle




• $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



• Hidden Refresh Cycle

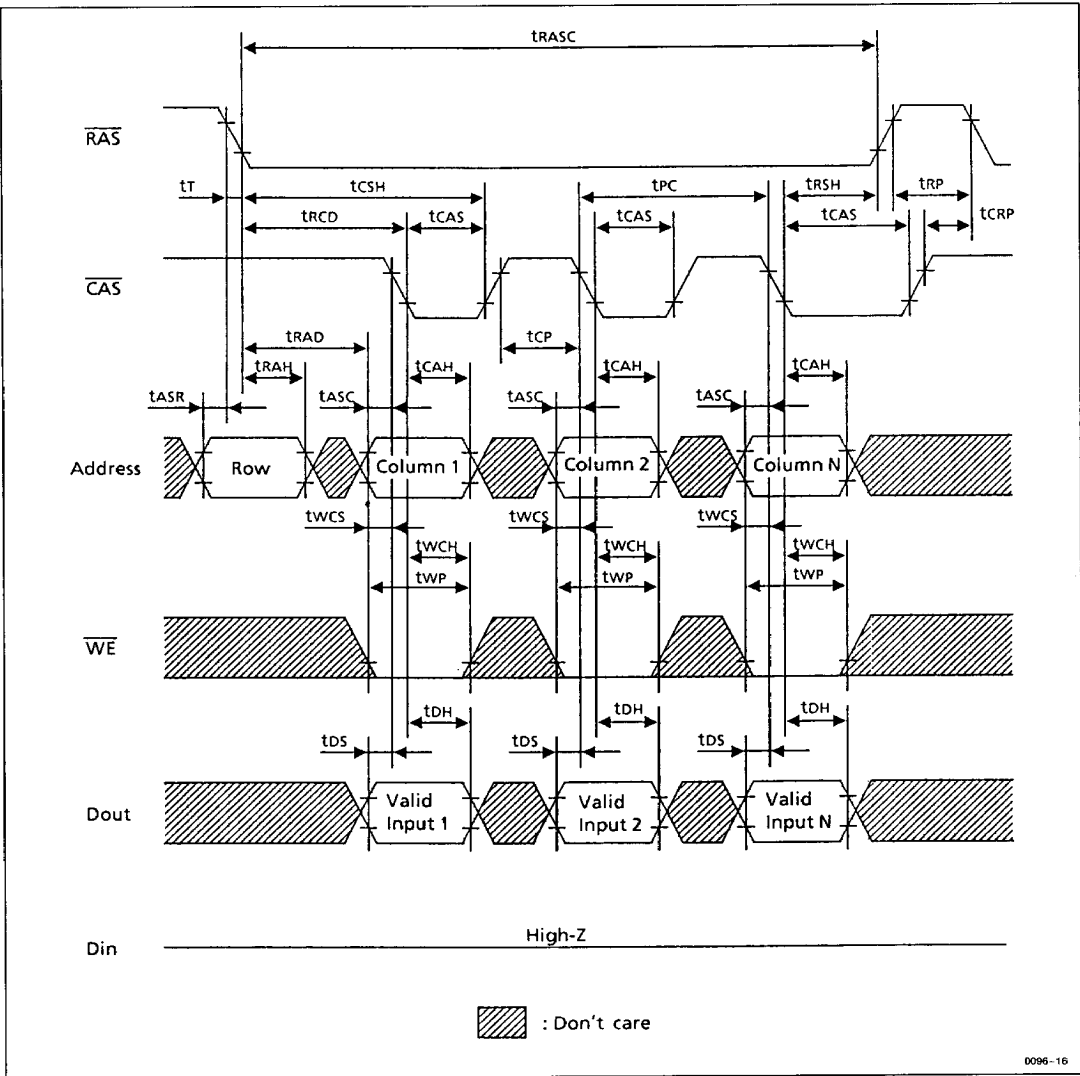


1  : Don't care

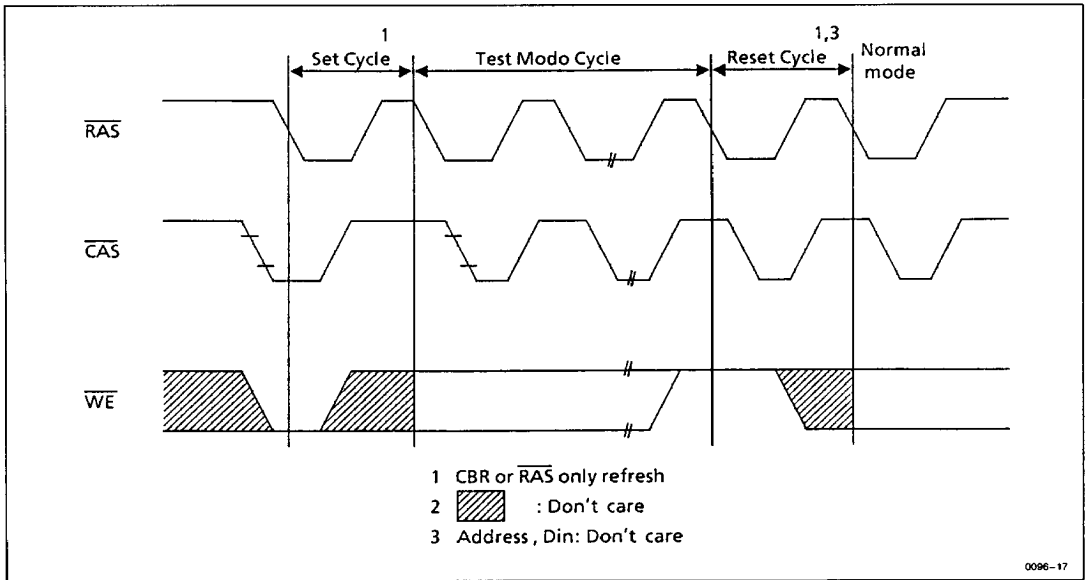
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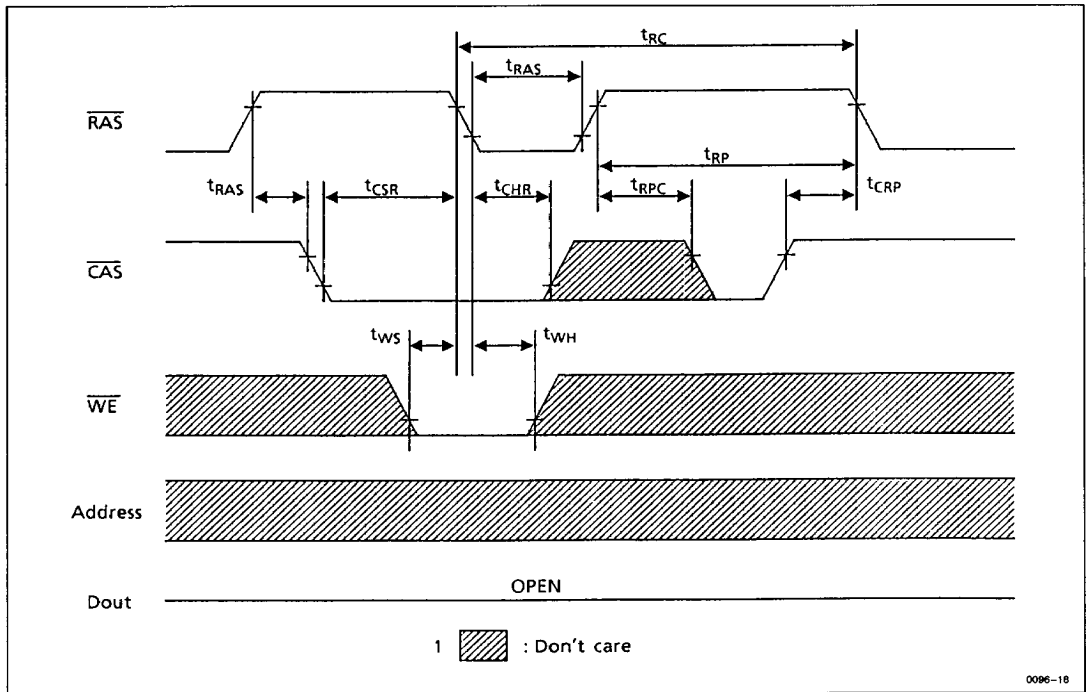
• Fast Page Mode Early Write Cycle



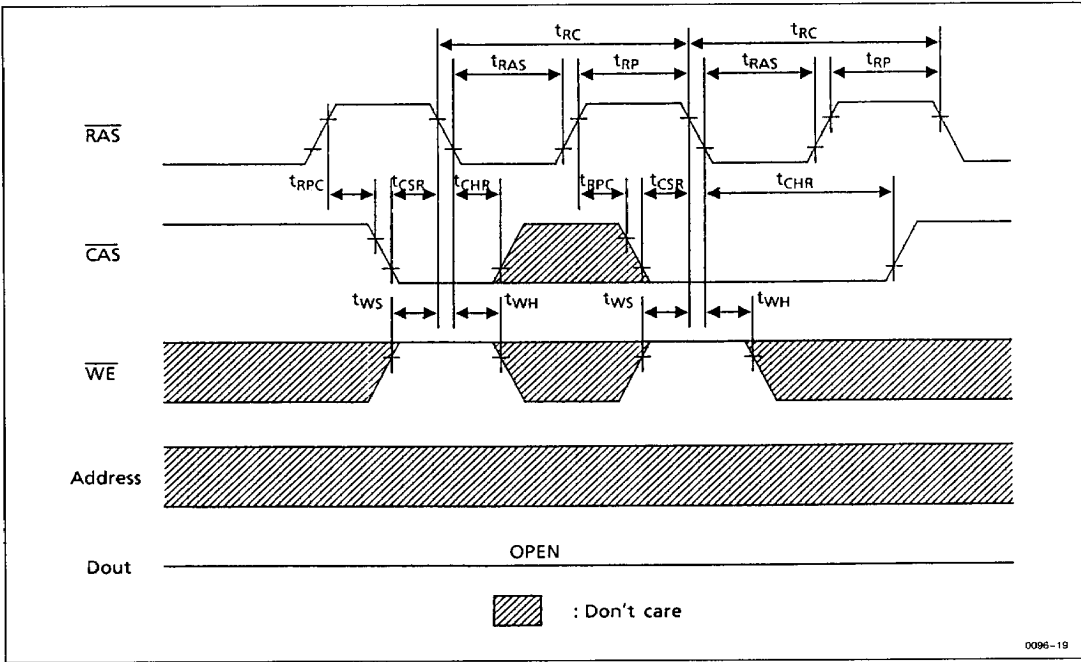
• TEST MODE CYCLE



• Test Mode Set Cycle



• Test Mode Reset Cycle
CAS Before RAS Refresh Cycle



RAS Only Refresh Cycle

