C9821

Direct Rambus® Plus Clock Generator

Product Features

- High Speed Clock support - provides a 267 to 400MHz differential clock source for Direct Rambus® memory systems for an 1.6 GbPS data transfer rate
- Synchronization Flexibility - provides signals to synchronize the clock domains of the Rambus® Channel with an external system or processor clock, provided by C9801, C9812, C9830, C9840, C9850, C9851, and the C9853.
- Power Management Support permits channel clocks to be enabled and disabled as required
- Supports Independent Channel Clocking
- 24 pin 150 mil SSOP Package
- Supports Intel Architecture platforms

Product Description

The C9821 is a Rambus® compliant DRCG clock synchronizer. It contains a Phase Locked Loop that provides complimentary Rambus® memory clocks. Included in its functionality is the control logic to phase and frequency synchronizing the device's output clocks with the system reference clock. Power management logic is also provided for Mobile application and green PC functionality. Also included are separate power pins for each internal functional block so as to minimize interaction of these sections with each other and thus maximize the device performance.

Block Diagram

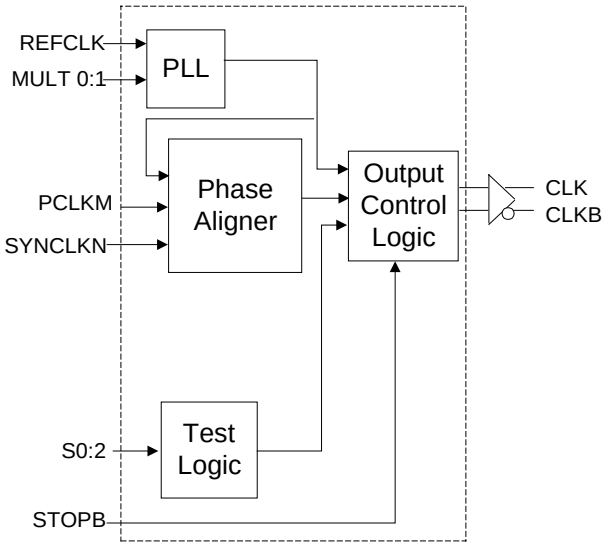


Figure: 1

Pin Configuration

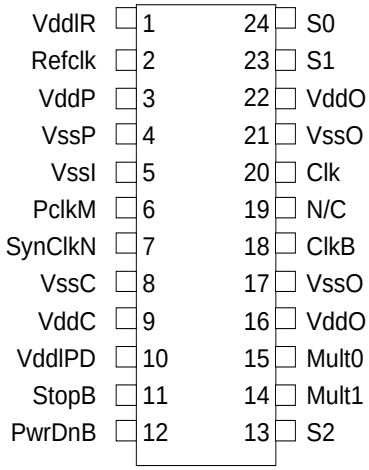


Figure: 2

Pin Description

Pin No.	Pin Name	I/O	Description
2	**REFCLK**	I	Reference clock input. Normally supplied by a system clock source generator.
6	**PCLKM**	I	Phase detector input: The phase difference between this signal and SYNCLKN is used to synchronize the Rambus®channel Clock with the system clock. The memory controller provides both the PCLKM and SYNCLKN. If the gear ratio is not used, connect this pin to ground.
7	**SYNCLKN**	I	Phase detector input: The phase difference between this signal and PCLKM is used to synchronize the Rambus® Channel Clock with the system clock. THE MEMORY CONTROLLER PROVIDES PCLKM AND SYNCLKN. If the gear ratio is not used, connect this pin to ground.
11	**STOPB**	I	Clock Stop. When this input is driven to low state, the differential Rambus® channel clocks are disabled.
12	**PWRDNB**	I	Power Down. When this input is driven to a logic low level, the differential Rambus® channel clocks are disabled and the system clock generator is placed in a power-down mode.
15, 14	**MULT (0:1)**	I	PLL Multiplier Select: These inputs select the PLL prescaler and feedback dividers to determine the multiply ratio for the PLL from the input REFLCK.
18, 20	**CLKB, CLK**	O	Differential Rambus ® channel clock outputs.
24, 23 13	**S0, S1, S2**	I	These input pins control the operating mode of the device.
19	**NC**	-	No Connect. DO NOT CONNECT ANY VOLTAGE LEVELS TO THIS PIN.
1	**VDDIR**	RefV	Base voltage reference level for the device's input reference clock.
10	**VDDIPD**	RefV	Base voltage reference for the PCLKM, SYNCLKN, and STOPB.
9	**VDDC**	P	Power supply connection for the devices phase aligner circuitry. Connected to 3.3V supply.
3	**VDDP**	P	Power supply for Analog PLL circuitry. Connected to 3.3V supply.
16, 22	**VDDO**	P	Power supply clock output buffers. Connected to 3.3V supply. Care should be taken when routing these power supply connections so as to not have their power supply current is adequately bypassed (as close to the device as possible) and their switching noise (surges) does not couple into the other device power supplies.
8	**VSSC**	P	Power supply ground return connection for the devices phase aligner circuitry. Connected to system ground.
5	**VSSI**	P	Reference supply ground for control input signals.
4	**VSSP**	P	Power supply ground return connection for Analog PLL circuitry. Should be connected to system ground potential through a well bypassed path.
17, 21	**VSSO**	P	System Ground for clock output buffers. Care should be taken when routing these power return connections so as to not have their power return current shared with other power return paths of the device.

A bypass capacitor (0.1µF) should be placed as close as possible to each Vdd pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be canceled by the lead inductance's of the traces.

System Clock Configuration

Figure 3 shows the clocking configuration for an example Direct Rambus subsystem. The configuration shows the interconnection of the system clock source, the C9821, and the clock signals of a memory controller ASIC. The ASIC contains the RAC, the Rambus Memory Controller protocol engine (RMC), and logic to support synchronizing the Channel clock with the controller clock (This diagram represents the differential clocks as a single Busclk wire).

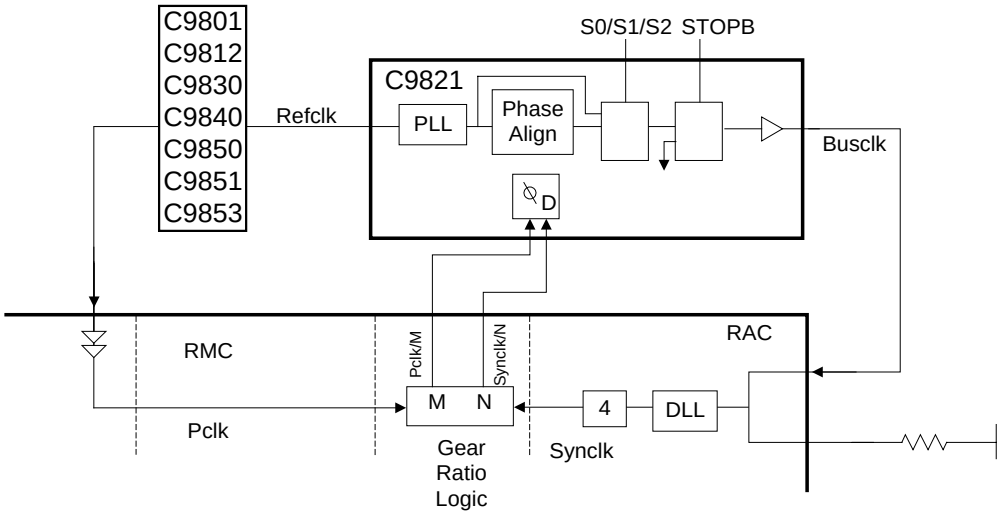


Figure: 3 DDLL System Architecture

This configuration achieves frequency-lock between the controller and Rambus Channel clocks (Pclk and Synclk). these clock signals are matched and phase-aligned at the RMC/RAC boundary in order to allow data transfers to occur across this boundary without additional latency.

The main clock source drives the system clock (Pclk) to the ASIC, and also drives the reference clock (Refclk) to the C9821. Refclk is not the same frequency as Pclk. A PLL inside the C9821 multiplies Refclk to generate the desired frequency for Busclk. Busclk is driven on the Rambus Channel through a terminated transmission line. At the mid-point of the Channel, the RAC senses Busclk using its own DLL for clock alignment, followed by a fixed divide-by-4 circuit that generates SynClk.

Pclk is the clock used in the Rambus memory controller (RMC) in the ASIC. SynClk is the clock used at the ASIC interface of the RAC. The C9821 together with the Gear Ratio Logic enables the controller to exchange data directly from the Pclk domain to the SynClk domain without incurring additional latency for synchronization. In general, Pclk and SynClk can run at different frequencies, so the Gear Ratio Logic must select the appropriate M and N dividers such that the frequencies of Pclk/M and SynClkN are equal. In one example, Pclk = 133 MHz and SynClk = 100 MHz, and M = 4 while N = 3, giving Pclk/M = SynClk/N = 33 MHz.

The ASIC drives the output clocks, Pclk and SynClk/N from the Gear Ratio Logic to the C9821 Phase Detector inputs. The routing of the Pclk/M and SynClk/N signal traces must be matched in impedance and propagation delay on the ASIC as well as on the board. These signals are not part of the Rambus Channel and board designers must match their routing.

System Clock Configuration (Cont.)

After comparing the phases of Pclk/M and SynClk/N, the C9821 Phase Detector drives a phase aligner that adjusts the phase of the C9821 output clock, busclk. Since the other elements in the distributed loop have a fixed delay, adjusting Busclk adjusts the phase of SynClk and thus the phase of SynClk/N.

In this manner, the distributed loop adjusts the phase of SynClk/N to match that of Pclk/M, eliminating the phase error at the input of the C9821. When the clocks are aligned, data can be exchanged directly from the Pclk domain to the SynClk domain.

The Gear Ratio Logic supports four clock ratios (1.0, 1.33, 1.5), where the ratio is defined as the ratio of Pclk/SynClk. Since Busclk - 4*synClk, this ratio also is equal to 4*Pclk/busclk.

In addition, the device is able to receive input signals that are generated from different voltage power supplies. The controller output voltage supply is connected to the pin VDDIPD of the C9821, and is used as the reference for the two-phase detector input signal, PclkM and SynClkN. The output voltage supply is also used as the reference for the output enable/disable signal, StopB.

The reference clock comes from the main clock source chip. The main clock source output voltage supply is connected to the pin VDDIR of C9821, and is used as the reference for the Refclk input signal.

Table of Frequencies and Gear Ratios

Gear Ratio Timing Diagram

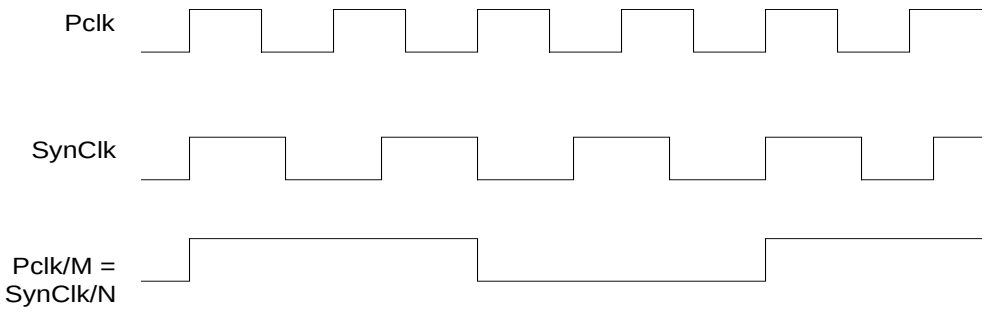


Figure: 4

Table of Frequencies and Gear Ratios (Cont.)

Pclk	Refclk	Busclk	Synclk	A	B	M	N	Ratio	F@PD
67	33	267	67	8	1	2	2	1.0	33
100	50	300	75	6	1	8	6	1.33	12.5
100	50	400	100	8	1	2	2	1.0	25
133	67	400	100	6	1	8	6	1.33	16.7
133	67	356	89	16	3	6	4	1.5	22
150	75	400	100	16	3	6	4	1.5	25

Table 1A. Frequencies, Dividers, and Gear Ratios

A: Feedback divider in the DRCG PLL.
B: Refclk divider in the DRCG PLL
M: Pclk divider in the gear ratio logic.
N: synclk divider in the gear ratio logic.

Table 1A above shows several supported Pclk and Busclk frequencies, the corresponding A and B dividers required in the DRCG PLL, and the corresponding M and N dividers in the gear ratio logic. The column Ratio gives the Gear Ratio as defined by Pclk/Synclk (same as M/N). The column F@PD gives the divided down frequency (in MHz) at the Phase Detector, where F@PD = Pclk/M = Synclk/N.

Table 1B below show examples of CLK/CLKB frequencies for different DRCG input frequencies.

Mult0	Mult1	DRCG input Frequency	CLK and CLKB output frequency
0	0	89 MHz	400 MHz
0	1	50 MHz	300 MHz
1	0	50 MHz	267 MHz
1	1	50 MHz	400 MHz
0	0	66 MHz	300 MHz
0	1	66 MHz	400 MHz
1	0	66 MHz	356 MHz
1	1	33 MHz	267 MHz

Table 1B: CLK and CLKB example frequencies

Selection Logic

Mult0	Mult1	A	B
0	0	9	2
0	1	6	1
1	0	16	3
1	1	8	1

Table 2: PLL Divider Selection

Selection Logic (Cont.)

Table 2 shows the logic for selecting the PLL prescaler and feedback dividers to determine the multiply ratio for the PLL from the input Refclk. Divider A sets the feedback and Divider B sets the prescaler, so the PLL output is set by: PLLclk = Refclk*A/B.

Mode	StopB	Clk	ClkB
Normal	1	PAclk	PAclkB
Clk Stop	0	$V_{X,STOP}$	$V_{X,STOP}$

Table 3: Clk Stop Mode Selection

Table 3 shows the logic for enabling the clock outputs, using the StopB input signal. When StopB is high, the DRCG is in its normal mode, and Clk and ClkB are complementary outputs following the Phase Aligner output (PAclk). When StopB is low, the DRCG is in the Clk Stop mode, the output drivers are both disabled (set to Hi-Z), and the Clk and ClkB outputs both drive DC voltages ($V_{X,STOP}$) as given in Table 11. The level of $V_{X,STOP}$ is set by internal resistor dividers.

Mode	S0	S1	S2	Bypclk (Int.)	Clk	ClkB
Normal	0	0	0	Gnd	PAclk	PAclkB
Bypass	1	0	0	PLLclk	PLLclk	PLLclkB
Test	1	1	0	Refclk	Refclk	RefclkB
Vendor Test A	0	0	1	-	-	-
Vendor Test B	1	0	1	-	-	-
Reserved	1	1	1	-	-	-
Output Test (OE)	0	1	X	-	Hi-Z	Hi-Z

Table 4: Bypass and Test Mode Selection

Power Management Functions

Mode	PwrDnB	Clk	ClkB
Normal	1	PAclk	PAclkB
PowerDown	0	Gnd	Gnd

Table 5: Powerdown Mode Selection

Table 5 shows the logic for selecting the Powerdown mode, using the PwrDnB input signal. PwrDnB is active low (enabled when 0). When PwrDnB is disabled, the DRCG is in its normal mode. When PwrDnB is enabled, the DRCG is put into a powered-off state, and the Clk and ClkB outputs are both low (ground).

Power Management Functions (Cont.)

The device is able to turn off the Rambus Channel clock to minimize power for mobile and other power-sensitive applications. In the “clock off” mode, the device remains on while the output is disabled, allowing fast transitions between the clock-off and clock-on states. This mode could be used in conjunction with the Nap mode of the RDRAMs and Rambus ASIC Cell (RAC). When output clocks are in a power down mode they are driven to and held at a logic low level by the device.

In the “power down” mode, the device is completely powered down for minimum power dissipation. This mode is used in conjunction with the power down modes of the RDRAMs and RAC.

The device has three operating states: Normal, Clock off and Powerdown. In normal mode, the clock source is on, and the output is enabled. In Clock off mode, the clock source is on, but the output is disabled (StopB asserted). In powerdown mode, the device is powered down with the control signal PwrDnB equal to 0. The control signals Mult0, Mult1, S0, S1, and S2 must be stable before power is applied to the device, and can only be changed in power-down mode (PwrDnB=0).

Power Management Modes

State	PwrDnB	StopB
Normal	1	1
Clock Off	1	0
Powerdown	0	X

Table 6: Control Signals for Clock Source States

Upon applying power to the device, the device can enter any state, depending on the settings of the control signals, PwrDnB and StopB. the clock source output need not be glitch-free during state transitions.

State Transitions

The clock source has three fundamental operating states. Figure 5 shows the state diagram with each transition labeled A through J. Note that the clock source output need NOT be glitch-free during state transitions.

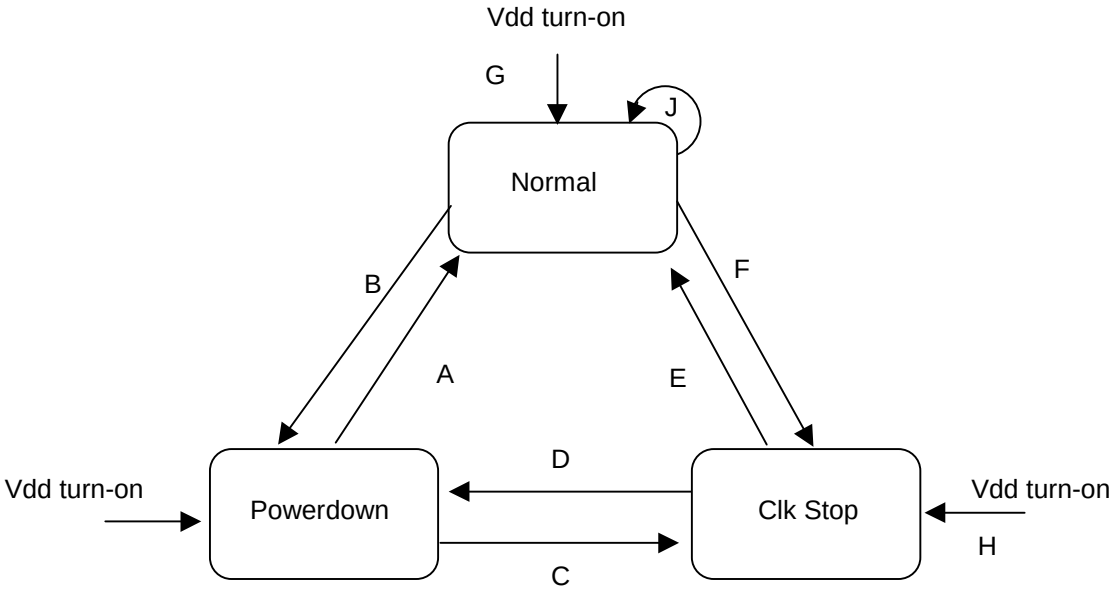


Figure 5: Clock Source State Diagram

Upon powering up the device, the device can enter any state, depending on the settings of the control signals PwrDnB and StopB.

In Powerdown mode, the clock source is powered down with the control signal, PwrDnB, equal to 0. The control signals S0, S1, and S2 must be stable before power is applied to the device, and can only be changed in Powerdown mode (PwrDnB=0). The reference inputs, VddIR and VddIPd, may remain on or may be grounded during the Powerdown mode.

The control signals Mult0, Mult1 can be used in two ways. If they are changed during Powerdown mode, then the Powerdown transition timings determine the settling time of the DRCG. However, the Mult0 and Mult1 control signals can also be changed during Normal mode. When the Mult control signals are “hot swapped” in this manner, the Mult transition timings determine the settling time of the DRCG.

In Clk Stop mode, the clock source is on, but the output is disabled (StopB de-asserted). The VddIPD reference input may remain on or may be grounded during the Clk Stop mode. The VddIR reference input must remain on during the Clk Stop mode.

State Transitions and Timing Diagrams

Powerdown Exit and Entry

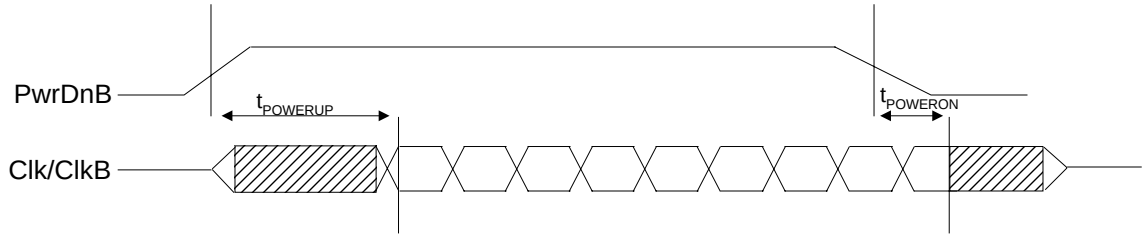


Figure: 6

Output Enable Control

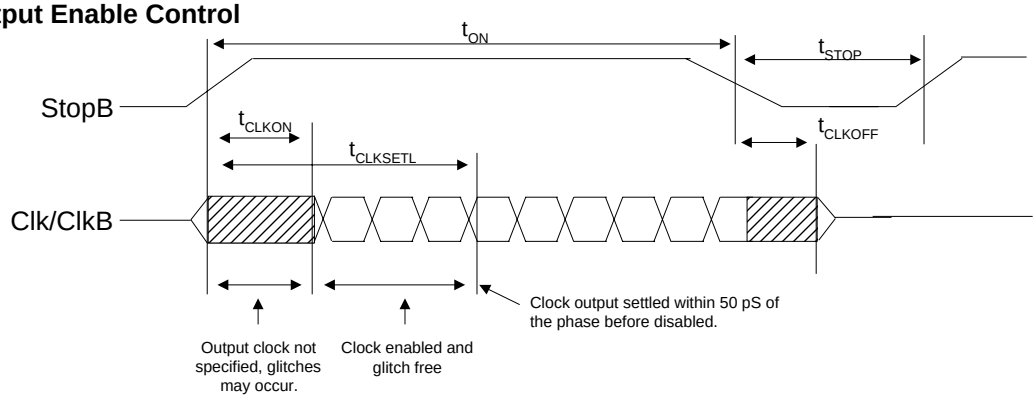


Figure: 7

Mult Transition Timing Diagram

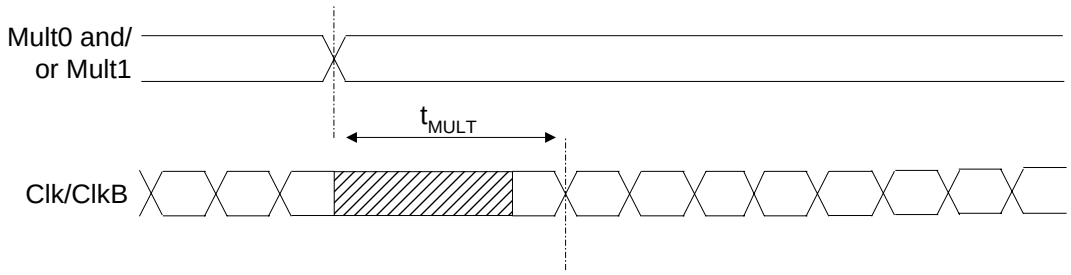


Figure: 8

Transition Specifications

Transition	From	To	Transition Latency (target spec)		Description
			Symbol	Max	
A	Powerdown	Normal	tPOWERUP	3 ms	Time from PwrDnB ↑ to Clk/ClkB output settled (excluding tDISTLOCK).
C	Powerdown	Clk Stop	tPOWERUP	3 ms	Time from PwrDnB ↑ to when the internal PLL and clock has turned on and settled.
G	Vdd on	Normal	tPOWERUP	3 ms	Time from Vdd is applied and settled to Clk/ClkB output settled (excluding tDISTLOCK).
H	Vdd on	Clk Stop	tPOWERUP	3 ms	Time from Vdd is applied and settled to the internal PLL and clock has turned on and settled.
J	Normal	Normal	tMULT	1 ms	Time from Mult0 or Mult1 change to Clk/ClkB output re-settled (excluding tDISTLOCK).
E	Clk Stop	Normal	tCLKON	10 ns	Time from StopB ↑ to when Clk/ClkB provides glitch-free clock edges.
E	Clk Stop	Normal	tCLKSETL	20 cycles	Time from stopB ↑ to Clk/ClkB output settled to within 50 ps of the phase before StopB was disabled.
F	Normal	Clk Stop	tCLKOFF	5 ns	Time from StopB ↓ to Clk/BlkB output disabled.
B,D	Normal or Clk Stop	Powerdown	tPOWERDN	1ms	Time from PwerDnB ↓ to the device in Powerdown.

Table 7: State Transition Latency Specifications

Transition Specifications (Cont.)

Figure 7 shows that the Clk Stop to Normal transition goes through three phases. During tCLKON, the clock output is not specified and can have glitches. For tCLKON < t<tCLKSETL, the clock output is enabled and must be glitch-free. For t>tCLKSETL, the clock output phase must be settled to within 50 ps of the phase before the clock output was disabled. At this time, the clock output must also meet the voltage and timing specifications in Table 11. The outputs are in a high impedance state during the Clk Stop mode (see Table 7). The above specification apply when the output has been held in the ClkStop state for less than tSTOP of Table 8.

Symbol	Min	Max	Units	Description
tSTOP		100	µS	Max time in Clk Stop (StopB=0) before re-entering Normal mode (StopB=1).
tON	100		nS	Min time in Normal mode (StopB=1) before re-entering Clk Stop (StopB=0)

Table 8: StopB Control Timing

After the DRCG PLL has settled, the distributed loop containing the phase aligner must also settle. This settling time depends on components in the distributed loop which are outside of the clock source. Therefore, this settling time is not a component specification.

The maximum lock time for the distributed loop is specified in Table 9 below. Note that the total time for the output clock to settle from the Powerdown state to the Normal state is the sum of tPOWERUP plus tDISTLOCK. Similarly, if the Mult0 and Mult1 control signals are changed during the Normal state, the total time for the output clock to re-settle is the sum of tMULT plus tDISTLOCK.

Symbol	Min	Max	Units	Description
tDISTLOCK		5	mS	Time from when Clk/ClkB output is settled to when the phase error between SynClkN and PclkM falls with the t_{ERR-PD} spec in Table 11.

Table 9: Distributed Loop Lock Time Specification

Maximum Ratings

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0ºC to + 125ºC
Ambient Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	3.135	-	3.465	V	
Input (scalable CMOS) Signal Low Voltage	V_{IL}	-	-	0.3	Vdd	
Input (scalable CMOS) Signal High Voltage	V_{IH}	0.7	-	-	Vdd	
Refclk Input Low Voltage	$V_{IL,R}$	-	-	0.3	VddlR	
Refclk Input High Voltage	$V_{IH,R}$	0.7	-	-	VddlR	
Input Low Voltage	$V_{IL,PD}$	-	-	0.3	VddlPD	
Input High Voltage	$V_{IH,PD}$	0.7	-	-	VddlPD	
Input Supply Reference	$V_{DDI,R,}$	1.235	-	3.465	V	
Input Supply Reference for PD inputs	$V_{DDI,PD}$	1.235		2.625	V	
Channel Impedance	Z_{CH}		28		ohms	
Tri-State leakage Current	Ioz			50	uA	
Current in Powerdown state (PwrDnB=0)	Ipowerdown			200	uA	
Current in Clk Stop state (stopB = 0)	Iclkstop			50	mA	
Current in Normal state (stopB = 1)	Inormal			100	mA	
Reference Current in Powerdown state (PwrDnB=0)	Iref,pwdn			50	µA	
Reference Current in Normal or ClkStop state (PwrDnB=1)	Iref,norm			2	mA	
=3.3V ± 5%, TA = 0ºC to +70ºC						

Note 1. DC bias = 0.9V, and V_{AC} < 100mV

Table 10: Electrical Characteristics

Device Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle over 10,000 cycles	DC	40%	50%	60%	t cycle	
Clock cycle time	t_{CYCLE}	2.5	-	3.75	nS	
Jitter over 1-6 clock cycles at 400 MHz[a]		-		100	pS	
Jitter over 1-6 clock cycles at 356 MHz[a]	tj	-		140	pS	
Jitter over 1-6 clock cycles at 300 MHz[a]		-		140	pS	
Jitter over 1-6 clock cycles at 267 MHz[a]		-		160	pS	
Phase Aligner phase step size (at Clk/ClkB)	t_{STEP}	2			pS	
Phase Detector phase error for distributed loop Measured at PcklM-SynclkN (rising edges) (does not include clock Jitter)	$t_{ERR,PD}$	-100	-	100	pS	
PLL output phase error when tracking SSC	$t_{ERR,SSC}$	-100	-	100	pS	
Output voltage during Clk Stop (StopB=0)	$V_{X,STOP}$	1.1	-	2.0	V	
Output crossing-point voltage	V_X	1.3	-	1.8	V	
Output voltage swing[b]	V_{COS}	0.4	-	0.6	V	
Output high voltage	V_{OH}	-	-	2.0	V	
Output low voltage	V_{OL}	1.0	-	-	V	
Output dynamic resistance (at pins)[c]	R_{OUT}	12	-	50	Ω	
Output current during Hi-Z (S0=1, S1=1)	I_{OZ}	-	-	50	µA	
Output current during Clk Stop (StopB=0)	$I_{OZ,STOP}$	-		500	µA	
Cycle-to-cycle duty cycle error at 400 MHz		-	-	50	pS	
Cycle-to-cycle duty cycle error at 300 MHz	$t_{DC,ERR}$	-	-	70	pS	
Cycle-to-cycle duty cycle error at 267 MHz		-	-	80	pS	
Output rise and fall times (measured at 20% - 80% of output voltage)	t_{CR}, t_{CF}	160	-	400	pS	
Difference between rise and fall times on the same pin of a single device (20% - 80%)	t_{CR}, t_{CF}	-		100	pS	
=3.3V ± 5%, TA = 0ºC to +70ºC						

a. Output short-term jitter spec is peak to peak.
b. $V_{COS} = V_{OH} - V_{OL}$
c. $R_{OUT} = \Delta V_O / \Delta I_O$. This is defined at the output pins, not at the measurement point.

Table 11: Device Characteristics

AC Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Units
Refclk Input Cycle Time	$t_{CYCLE,IN}$	10	-	40	nS
Faster speed bin for Refclk input cycle time[a]		6[a]	-	40	nS
Input Cycle-to-cycle jitter[b]	$t_{J,IN}$	-	-	250	pS
Input Duty Cycle over 10,000 cycles	D_{CIN}[c]	40%	-	60%	t_{CYCLE}
Input Frequency of Modulation	$f_{MIN,IN}$[c]	30	-	33	kHz
Modulation index for triangular modulation	$P_{M,IN}$[c]	-	-	0.6	%
Modulation index for non-triangular modulation		-	-	0.5[d]	%
Phase Detector Input Cycle time at PclkM and SynclkN	$t_{CYCLE, PD}$	30	-	100	nS
Initial Phase Error at Phase Detector Inputs (required range of phase aligner)	$t_{ERR,INIT}$	-0.5	-	0.5	$t_{CYCLE,PD}$
Phase Detector Input Duty Cycle over 10,000 Cycles	$D_{CIN,PD}$	25%	-	75%	$t_{CYCLE,PD}$
Input Slew Rate (measured at 20% - 80% of input voltage) for PclkM, SynclkN, and Refclk	$t_{I,SR}$	1	-	4	V/nS
Input Capacitance at PclkM, SynclkN, and Refclk[e]	$C_{IN,PD}$	-	-	7	pF
Input Capacitance Matching at PclkM and SynclkN[e]	$\Delta C_{IN,PD}$	-	-	0.5	pF
Input Capacitance at Scalable CMOS Pins (excluding PclkM, SynclkN, and Refclk)[e]	$C_{IN,CMOS}$	-	-	10	pF

a. Faster speed bin for future systems (not a requirement now), and applicable for $V_{DDI,R}$>1.7V only
b. Refclk jitter measured at $V_{DDI,R}$(nom)/2
c. If input modulation is used, input modulation is allowed but not required.
d. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream tracking skew, which cannot exceed the skew generated by the specified 0.6% triangular modulation. Typically, the amount of allowed non-triangular modulation is about 0.5%.
e. Capacitance measured at Freq = 1 MHz, DC bias = 0.9V, and V_{AC}<100mV

Table 12: AC Operating Conditions

Test Circuit

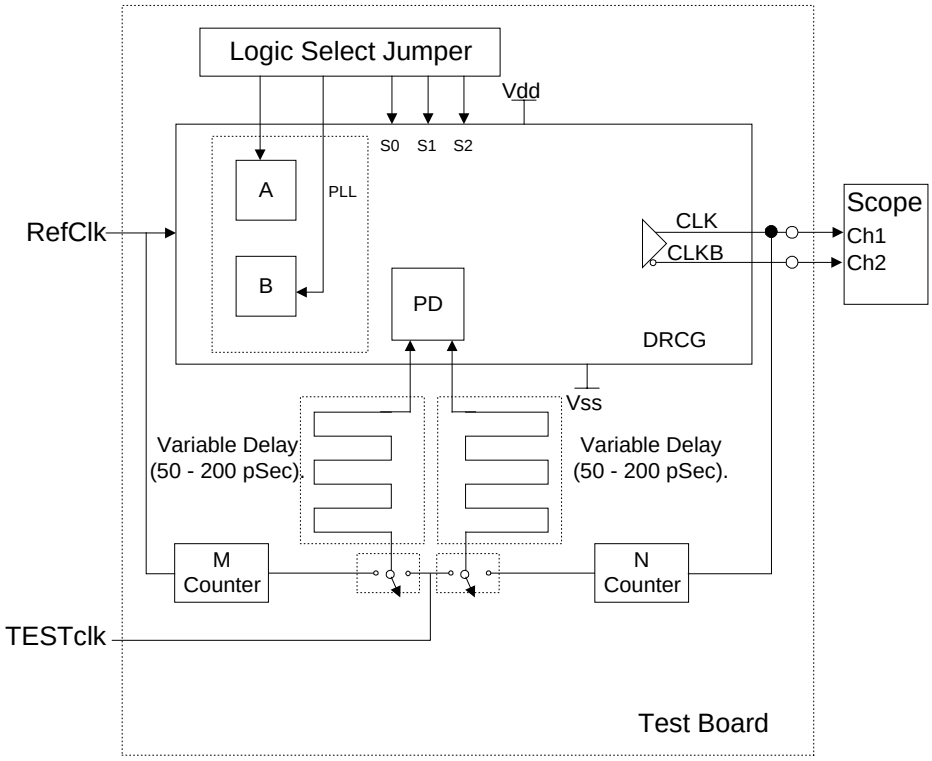


Figure 9: Characterization Test Fixture

Output Buffer Termination

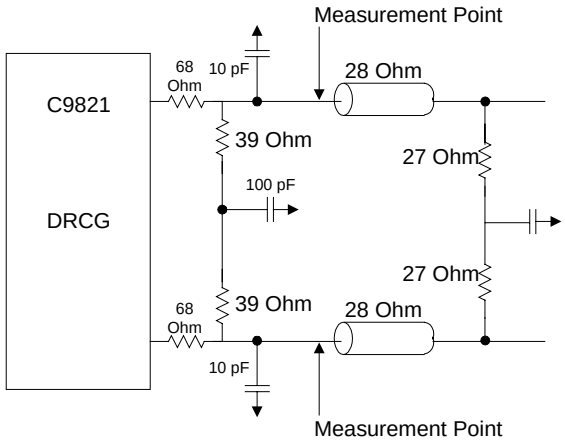
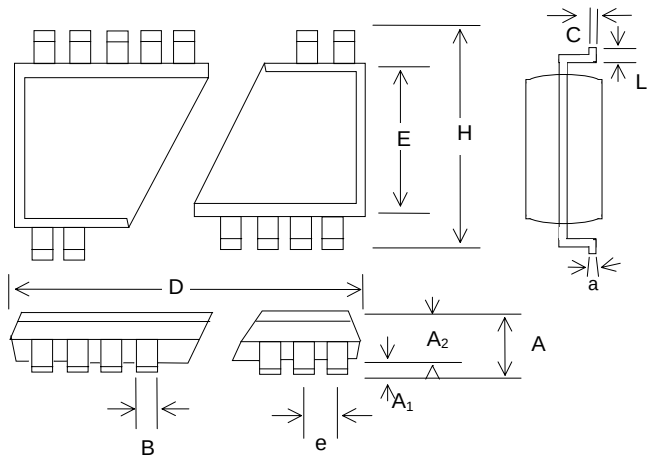


Figure 10: Output Termination

Package Drawing and Dimensions



24 Pin QSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	0.064	0.069	1.35	1.63	1.75
A_1	0.004	0.006	0.010	0.102	0.152	0.254
A2	0.055	-	0.059	1.40	-	1.50
B	0.008	-	0.012	0.203	-	0.305
C	0.007	-	0.010	0.178	-	0.254
D	0.337	0.341	0.344	8.56	8.66	8.74
E	0.150	0.154	0.157	3.81	3.91	3.99
e	0.025 BSC			0.635 BSC		
H	0.228	0.235	0.244	5.79	5.97	6.20
L	0.016	0.025	0.050	0.406	0.635	1.27
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
C9821GQ	24 PIN QSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Date Code
C9821GQ
Lot #

C9821GQ

- Package
  Q = QSOP (150 Mil. SSOP)
- Revision
- Device Number

Notice

Document Title: C9821 Direct Rambus® Plus Clock Generator **Document Number:** 38-07092				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107128	06/14/01	IKA	Convert from IMI to Cypress