

FEATURES

- 2-channel, 256-position devices
- OTP (one-time programmable) set-and-forget resistance setting, low cost alternative to EEMEM
- Unlimited adjustments prior to OTP activation
- OTP overwrite allows dynamic adjustments with user-defined preset
- End-to-end resistance: 2.5 k Ω , 10 k Ω , 50 k Ω , 100 k Ω
- Compact MSOP-10 (3 mm \times 4.9 mm) package
- Fast settling time: $t_s = 5 \mu s$ typ in power-up
- Full read/write of wiper register
- Power-on preset to midscale
- Extra package address decode pins AD0 and AD1 (AD5173)
- Single supply: 2.7 V to 5.5 V
- Low temperature coefficient: 35 ppm/ $^{\circ}C$
- Low power: $I_{DD} = 6 \mu A$ max
- Wide operating temperature: $-40^{\circ}C$ to $+125^{\circ}C$
- Evaluation board and software are available
- Software replaces μC in factory programming applications

APPLICATIONS

- Systems calibration
- Electronics level setting
- Mechanical Trimmers[®] replacement in new designs
- Permanent factory PCB setting
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- RF amplifier biasing
- Automotive electronics adjustment
- Gain control and offset adjustment

GENERAL OVERVIEW

The AD5172/AD5173 are dual-channel, 256-position, one-time programmable (OTP) digital potentiometers¹ that employ fuse link technology to achieve memory retention of resistance setting. OTP is a cost-effective alternative to EEMEM for users who do not need to program the digital potentiometer setting in memory more than once. This device performs the same electronic adjustment function as mechanical potentiometers or variable resistors with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

The AD5172/AD5173 are programmed using a 2-wire, I²C-compatible digital interface. Unlimited adjustments are allowed before permanently setting the resistance value. During OTP activation, a permanent blow-fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

Rev. B

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FUNCTIONAL BLOCK DIAGRAMS

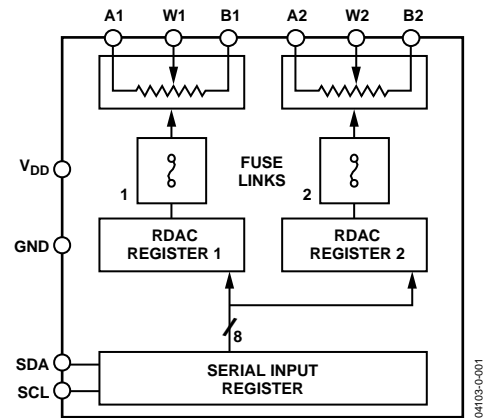


Figure 1. AD5172

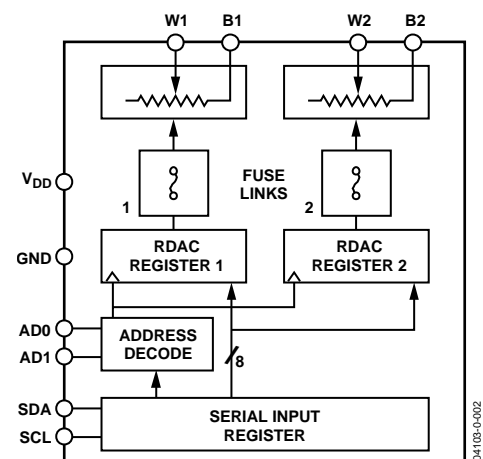


Figure 2. AD5173

Unlike traditional OTP digital potentiometers, the AD5172/AD5173 have a unique temporary OTP overwrite feature that allows for new adjustments even after a fuse has been blown. However, the OTP setting is restored during subsequent power-up conditions. This feature allows users to treat these digital potentiometers as volatile potentiometers with a programmable preset.

For applications that program the AD5172/AD5173 at the factory, Analog Devices offers device programming software running on Windows[®] NT[®], 2000, and XP[®] operating systems. This software effectively replaces any external I²C controllers, thus enhancing the time-to-market of the user's systems.

¹ The terms digital potentiometer, VR, and RDAC are used interchangeably.

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REVISION HISTORY

11/04—Changed from Rev. A to Rev. B

Updated Format.....	Universal
Changes to Specifications	3
Changes to One-Time Programming (OTP) Section.....	13
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11/03—Changed from Rev. 0 to Rev. A

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ELECTRICAL CHARACTERISTICS—2.5 k Ω VERSION

$V_{DD} = 5\text{ V} \pm 10\%$ or $3\text{ V} \pm 10\%$; $V_A = +V_{DD}$; $V_B = 0\text{ V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$; unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity ²	R-DNL	R_{WB} , $V_A = \text{No Connect}$	-2	± 0.1	+2	LSB
Resistor Integral Nonlinearity ²	R-INL	R_{WB} , $V_A = \text{No Connect}$	-6	± 0.75	+6	LSB
Nominal Resistor Tolerance ³	ΔR_{AB}	$T_A = 25^\circ\text{C}$	-20		+55	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, Wiper = No Connect		35		ppm/ $^\circ\text{C}$
RWB (Wiper Resistance)	R_{WB}	Code = 0x00, $V_{DD} = 5\text{ V}$		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications Apply to all VRs)						
Differential Nonlinearity ⁴	DNL		-1.5	± 0.1	+1.5	LSB
Integral Nonlinearity ⁴	INL		-2	± 0.6	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/ $^\circ\text{C}$
Full-Scale Error	V_{WFSE}	Code = 0xFF	-10	-2.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	2	10	LSB
RESISTOR TERMINALS						
Voltage Range ⁵	V_A , V_B , V_W		GND		V_{DD}	V
Capacitance ⁶ A, B	C_A , C_B	$f = 1\text{ MHz}$, Measured to GND, Code = 0x80		45		pF
Capacitance W	C_W	$f = 1\text{ MHz}$, Measured to GND, Code = 0x80		60		pF
Shutdown Supply Current ⁷	I_{A_SD}	$V_{DD} = 5.5\text{ V}$		0.01	1	μA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	$V_{DD} = 5\text{ V}$	2.4			V
Input Logic Low	V_{IL}	$V_{DD} = 5\text{ V}$			0.8	V
Input Logic High	V_{IH}	$V_{DD} = 3\text{ V}$	2.1			V
Input Logic Low	V_{IL}	$V_{DD} = 3\text{ V}$			0.6	V
Input Current	I_{IL}	$V_{IN} = 0\text{ V}$ or 5 V			± 1	μA
Input Capacitance ⁶	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD_RANGE}		2.7		5.5	V
OTP Supply Voltage	V_{DD_OTP}	$T_A = 25^\circ\text{C}$	5.25		5.5	V
Supply Current	I_{DD}	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$		3.5	6	μA
OTP Supply Current	I_{DD_OTP}	$V_{DD_OTP} = 5.5\text{ V}$, $T_A = 25^\circ\text{C}$	100			mA
Power Dissipation ⁸	P_{DISS}	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$, $V_{DD} = 5\text{ V}$			30	μW
Power Supply Sensitivity	PSS	$V_{DD} = 5\text{ V} \pm 10\%$, Code = Midscale		± 0.02	± 0.08	%/%
DYNAMIC CHARACTERISTICS⁹						
Bandwidth -3 dB	BW_2.5K	Code = 0x80		4.8		MHz
Total Harmonic Distortion	THD _W	$V_A = 1\text{ V rms}$, $V_B = 0\text{ V}$, $f = 1\text{ kHz}$		0.1		%
V_W Settling Time	t_S	$V_A = 5\text{ V}$, $V_B = 0\text{ V}$, $\pm 1\text{ LSB Error Band}$		1		μs
Resistor Noise Voltage Density	e_{N_WB}	$R_{WB} = 1.25\text{ k}\Omega$, $R_S = 0$		3.2		nV/ $\sqrt{\text{Hz}}$

¹ Typical specifications represent average readings at 25°C and $V_{DD} = 5\text{ V}$.

² Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

³ $V_{AB} = V_{DD}$, Wiper (V_W) = no connect.

⁴ INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and $V_B = 0\text{ V}$. DNL specification limits of $\pm 1\text{ LSB}$ maximum are guaranteed monotonic operating conditions.

⁵ Resistor terminals A, B, W have no limitations on polarity with respect to each other.

⁶ Guaranteed by design and not subject to production test.

⁷ Measured at the A terminal. The A terminal is open circuited in shutdown mode.

⁸ P_{DISS} is calculated from $(I_{DD} \times V_{DD})$. CMOS logic level inputs result in minimum power dissipation.

⁹ All dynamic characteristics use $V_{DD} = 5\text{ V}$.

ELECTRICAL CHARACTERISTICS—10 k Ω , 50 k Ω , 100 k Ω VERSIONS

$V_{DD} = 5\text{ V} \pm 10\%$ or $3\text{ V} \pm 10\%$; $V_A = V_{DD}$; $V_B = 0\text{ V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$; unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity ²	R-DNL	$R_{WB}, V_A = \text{No Connect}$	-1	± 0.1	+1	LSB
Resistor Integral Nonlinearity ²	R-INL	$R_{WB}, V_A = \text{No Connect}$	-2.5	± 0.25	+2.5	LSB
Nominal Resistor Tolerance ³	ΔR_{AB}	$T_A = 25^\circ\text{C}$	-20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, Wiper = No Connect		35		ppm/ $^\circ\text{C}$
R_{WB} (Wiper Resistance)	R_{WB}	Code = 0x00, $V_{DD} = 5\text{ V}$		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications Apply to all VRs)						
Differential Nonlinearity ⁴	DNL		-1	± 0.1	+1	LSB
Integral Nonlinearity ⁴	INL		-1	± 0.3	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/ $^\circ\text{C}$
Full-Scale Error	V_{WFSE}	Code = 0xFF	-2.5	-1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2.5	LSB
RESISTOR TERMINALS						
Voltage Range ⁵	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance ⁶ A, B	C_A, C_B	$f = 1\text{ MHz}$, Measured to GND, Code = 0x80		45		pF
Capacitance ⁶ W	C_W	$f = 1\text{ MHz}$, Measured to GND, Code = 0x80		60		pF
Shutdown Supply Current ⁷	I_{A_SD}	$V_{DD} = 5.5\text{ V}$		0.01	1	μA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	$V_{DD} = 5\text{ V}$	2.4			V
Input Logic Low	V_{IL}	$V_{DD} = 5\text{ V}$			0.8	V
Input Logic High	V_{IH}	$V_{DD} = 3\text{ V}$	2.1			V
Input Logic Low	V_{IL}	$V_{DD} = 3\text{ V}$			0.6	V
Input Current	I_{IL}	$V_{IN} = 0\text{ V}$ or 5 V			± 1	μA
Input Capacitance ⁶	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD_RANGE}		2.7		5.5	V
OTP Supply Voltage ⁸	V_{DD_OTP}		5.25		5.5	V
Supply Current	I_{DD}	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$		3.5	6	μA
OTP Supply Current ⁹	I_{DD_OTP}	$V_{DD_OTP} = 5.5\text{ V}$, $T_A = 25^\circ\text{C}$	100			mA
Power Dissipation ¹⁰	P_{DISS}	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$, $V_{DD} = 5\text{ V}$			30	μW
Power Supply Sensitivity	PSS	$V_{DD} = +5\text{ V} \pm 10\%$, Code = Midscale		± 0.02	± 0.08	%/%
DYNAMIC CHARACTERISTICS¹¹						
Bandwidth -3 dB	BW	$R_{AB} = 10\text{ k}\Omega$, Code = 0x80		600		kHz
		$R_{AB} = 50\text{ k}\Omega$, Code = 0x80		100		kHz
		$R_{AB} = 100\text{ k}\Omega$, Code = 0x80		40		kHz
Total Harmonic Distortion	THD _W	$V_A = 1\text{ V rms}$, $V_B = 0\text{ V}$, $f = 1\text{ kHz}$, $R_{AB} = 10\text{ k}\Omega$		0.1		%
V_W Settling Time (10 k Ω /50 k Ω /100 k Ω)	t_S	$V_A = 5\text{ V}$, $V_B = 0\text{ V}$, $\pm 1\text{ LSB Error Band}$		2		μs
Resistor Noise Voltage Density	e_{N_WB}	$R_{WB} = 5\text{ k}\Omega$, $R_S = 0$		9		nV/ $\sqrt{\text{Hz}}$

¹ Typical specifications represent average readings at 25°C and $V_{DD} = 5\text{ V}$.

² Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

³ $V_{AB} = V_{DD}$, Wiper (V_W) = no connect.

⁴ INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and $V_B = 0\text{ V}$. DNL specification limits of $\pm 1\text{ LSB}$ maximum are guaranteed monotonic operating conditions.

⁵ Resistor terminals A, B, W have no limitations on polarity with respect to each other.

⁶ Guaranteed by design and not subject to production test.

⁷ Measured at the A terminal. The A terminal is open circuited in shutdown mode.

⁸ Different from operating power supply, power supply OTP is used one time only.

⁹ Different from operating current, supply current for OTP lasts approximately 400 ms for one time only.

¹⁰ P_{DISS} is calculated from $(I_{DD} \times V_{DD})$. CMOS logic level inputs result in minimum power dissipation.

¹¹ All dynamic characteristics use $V_{DD} = 5\text{ V}$.

TIMING CHARACTERISTICS—2.5 k Ω , 10 k Ω , 50 k Ω , 100 k Ω VERSIONS

$V_{DD} = 5\text{ V} \pm 10\%$ or $3\text{ V} \pm 10\%$; $V_A = V_{DD}$; $V_B = 0\text{ V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$; unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C INTERFACE TIMING CHARACTERISTICS¹ (Specifications Apply to All Parts)						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between Stop and Start	t_1		1.3			μs
$t_{HD,STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated.	0.6			μs
t_{LOW} Low Period of SCL Clock	t_3		1.3			μs
t_{HIGH} High Period of SCL Clock	t_4		0.6			μs
$t_{SU,STA}$ Setup Time for Repeated Start Condition	t_5		0.6			μs
$t_{HD,DAT}$ Data Hold Time ²	t_6				0.9	μs
$t_{SU,DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU,STO}$ Setup Time for Stop Condition	t_{10}		0.6			μs

¹ See the timing diagrams (Figure 51 to Figure 55) for locations of measured values.

² The maximum $t_{HD,DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V _{DD} to GND	-0.3 V to +7 V
V _A , V _B , V _W to GND	V _{DD}
Terminal Current, A _X -B _X , A _X -W _X , B _X -W _X ¹	
Pulsed	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature (T _{JMAX})	150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 s)	300°C
Thermal Resistance ² θ _{JA} : MSOP-10	230°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

¹ Maximum terminal current is bound by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

² Package power dissipation = (T_{Jmax} - T_A)/θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

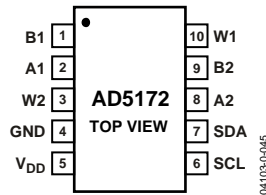


Figure 3. AD5172 Pin Configuration

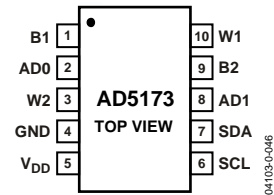


Figure 4. AD5173 Pin Configuration

Table 5. AD5172 Pin Function Descriptions

Pin	Mnemonic	Description
1	B1	B1 Terminal.
2	A1	A1 Terminal.
3	W2	W2 Terminal.
4	GND	Digital Ground.
5	V _{DD}	Positive Power Supply.
6	SCL	Serial Clock Input. Positive-edge triggered.
7	SDA	Serial Data Input/Output.
8	A2	A2 Terminal.
9	B2	B2 Terminal.
10	W1	W1 Terminal.

Table 6. AD5173 Pin Function Descriptions

Pin	Mnemonic	Description
1	B1	B1 Terminal.
2	AD0	Programmable Address Bit 0 for Multiple Package Decoding.
3	W2	W2 Terminal.
4	GND	Digital Ground.
5	V _{DD}	Positive Power Supply.
6	SCL	Serial Clock Input. Positive-edge triggered.
7	SDA	Serial Data Input/Output.
8	AD1	Programmable Address Bit 1 for Multiple Package Decoding.
9	B2	B2 Terminal.
10	W1	W1 Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

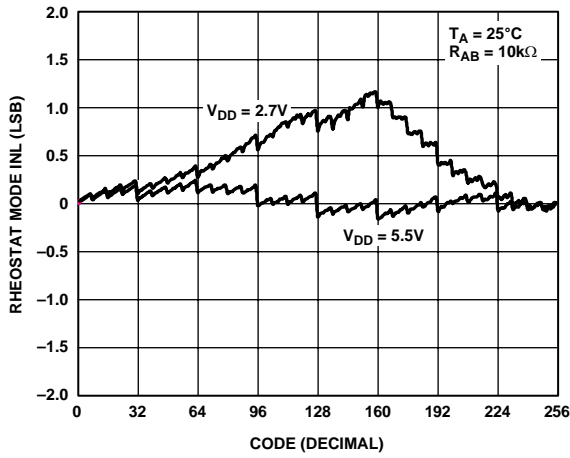


Figure 5. R-INL vs. Code vs. Supply Voltages

04103-0-003

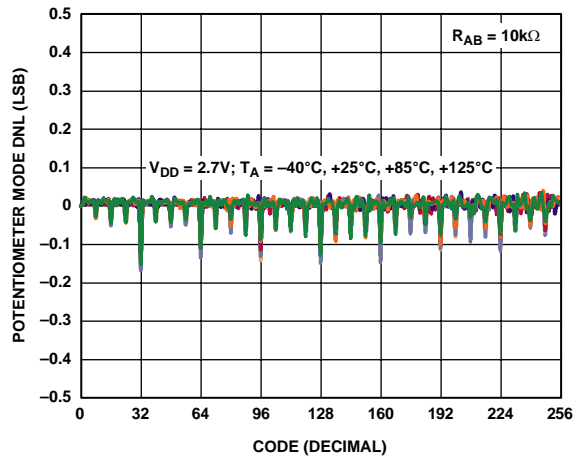


Figure 8. DNL vs. Code vs. Temperature

04103-0-006

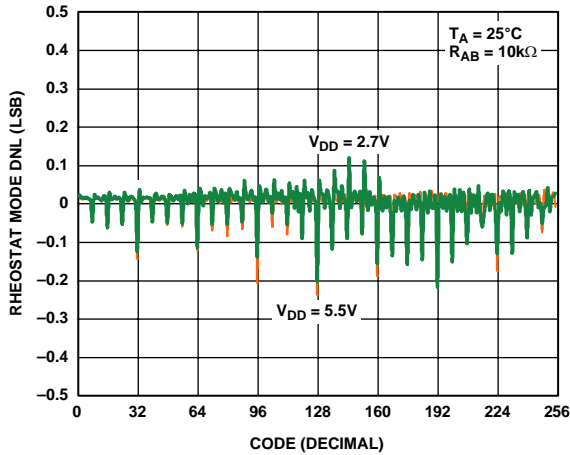


Figure 6. R-DNL vs. Code vs. Supply Voltages

04103-0-004

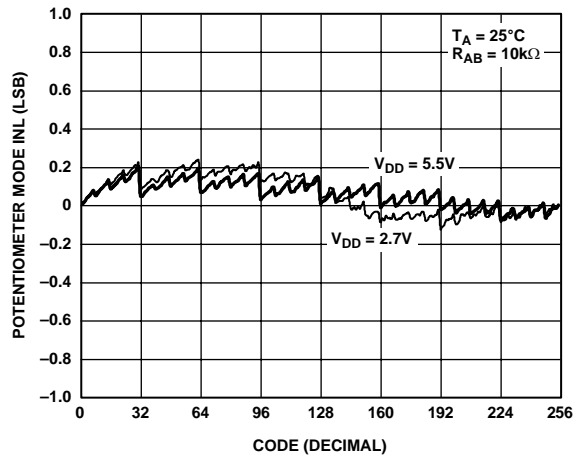


Figure 9. INL vs. Code vs. Supply Voltages

04103-0-007

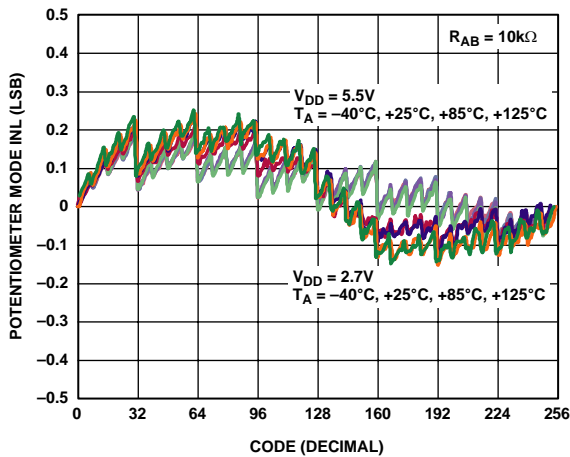


Figure 7. INL vs. Code vs. Temperature

04103-0-005

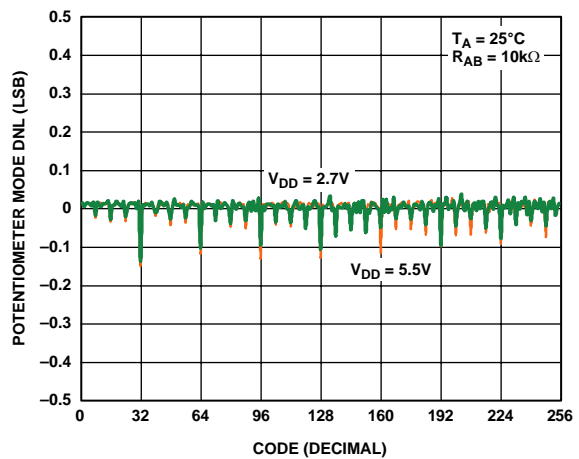


Figure 10. DNL vs. Code vs. Supply Voltages

04103-0-008

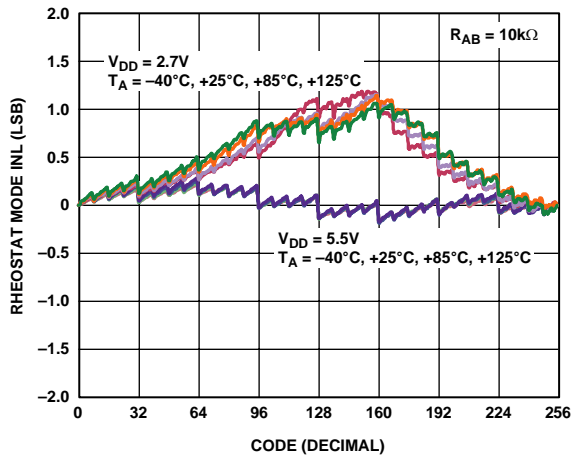


Figure 11. R-INL vs. Code vs. Temperature

04103-0-009

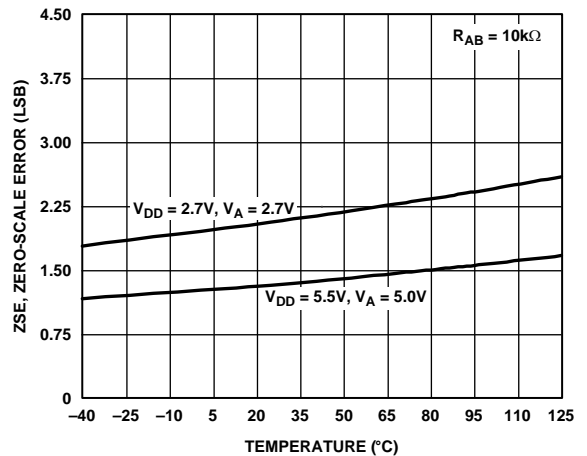


Figure 14. Zero-Scale Error vs. Temperature

04103-0-012

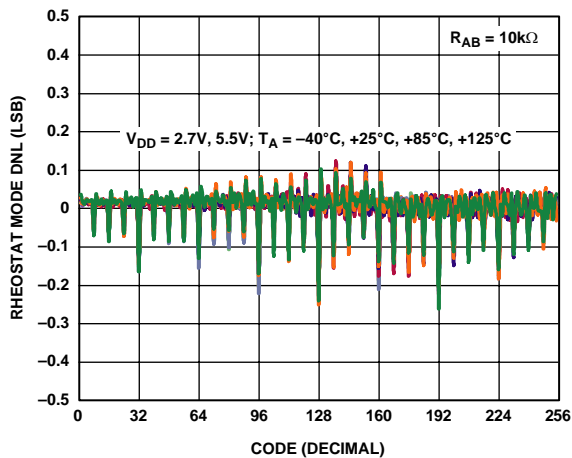


Figure 12. R-DNL vs. Code vs. Temperature

04103-0-010

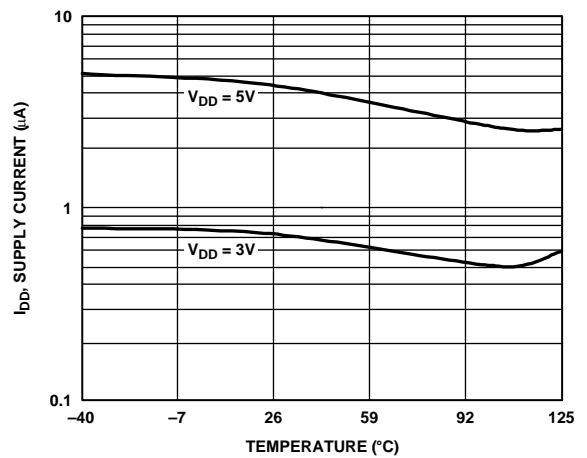


Figure 15. Supply Current vs. Temperature

04103-0-013

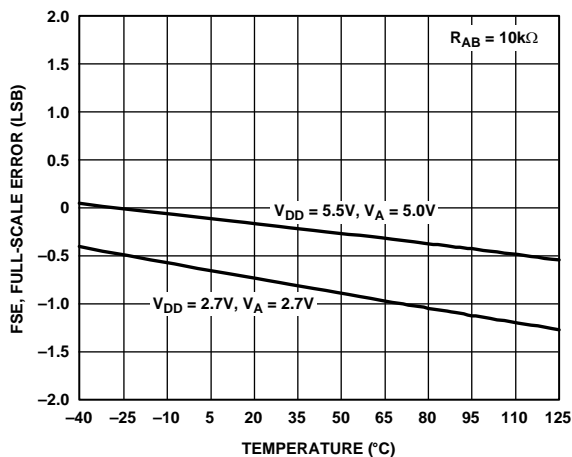


Figure 13. Full-Scale Error vs. Temperature

04103-0-011

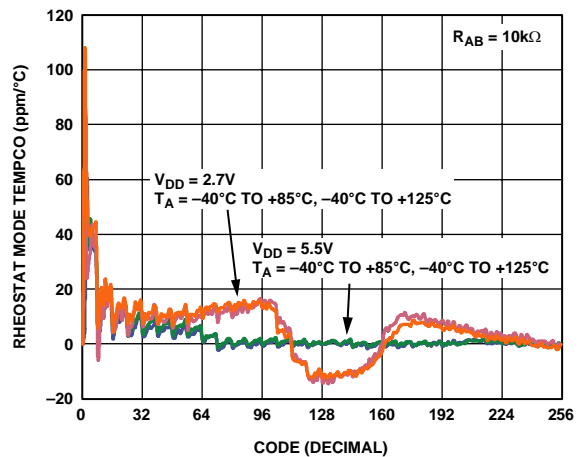


Figure 16. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

04103-0-014

AD5172/AD5173

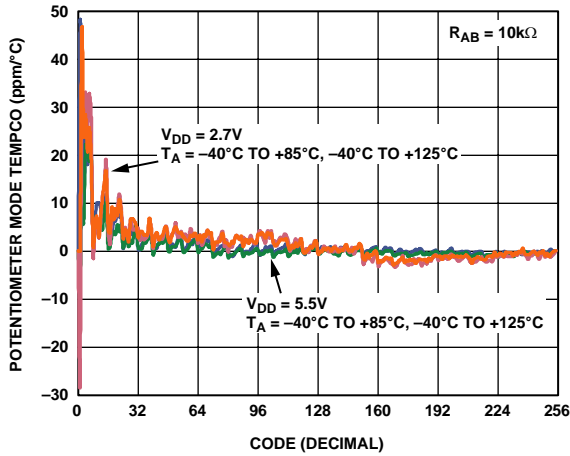


Figure 17. AD5172 Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

04103-0-047

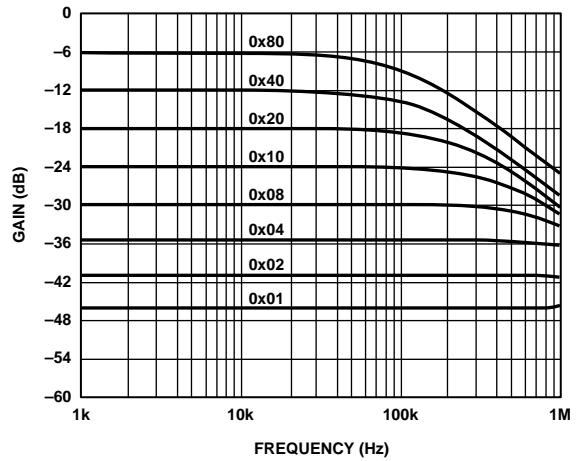


Figure 20. Gain vs. Frequency vs. Code, $R_{AB} = 50 \text{ k}\Omega$

04103-0-050

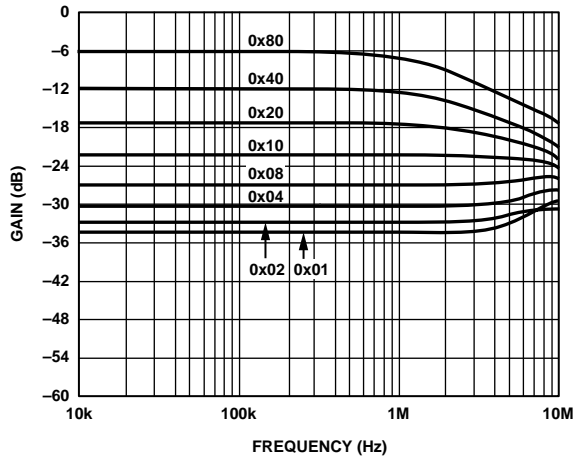


Figure 18. Gain vs. Frequency vs. Code, $R_{AB} = 2.5 \text{ k}\Omega$

04103-0-048

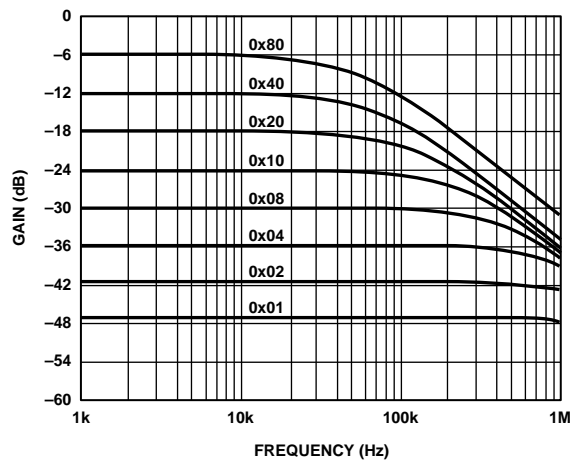


Figure 21. Gain vs. Frequency vs. Code, $R_{AB} = 100 \text{ k}\Omega$

04103-0-051

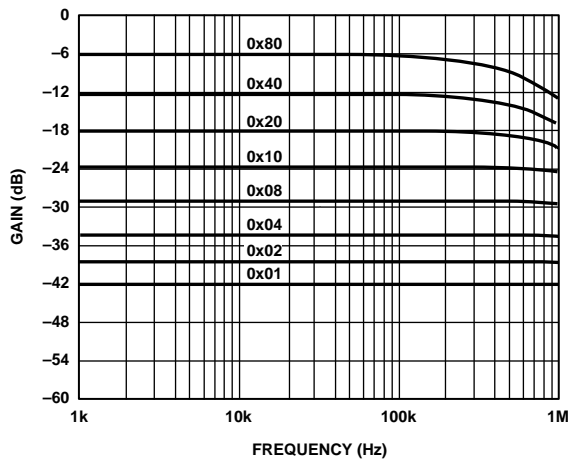


Figure 19. Gain vs. Frequency vs. Code, $R_{AB} = 10 \text{ k}\Omega$

04103-0-049

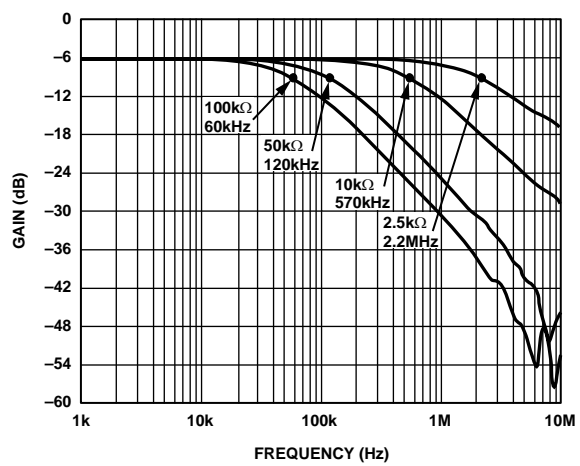


Figure 22. -3 dB Bandwidth @ Code = 0x80

04103-0-052

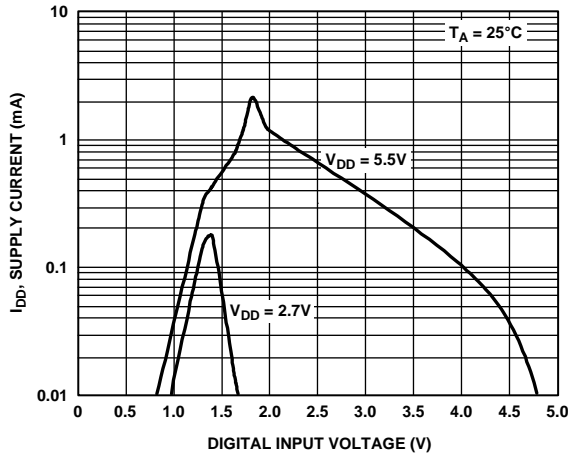


Figure 23. I_{DD} vs. Input Voltage

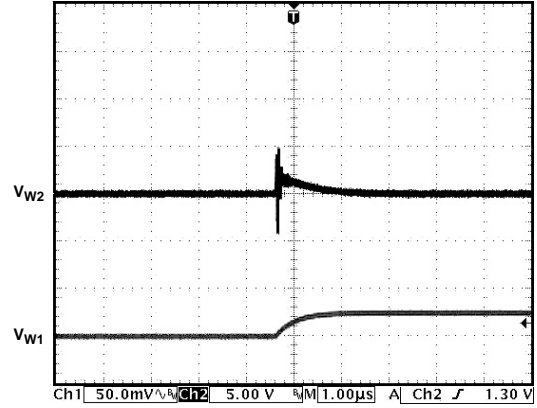


Figure 26. Analog Crosstalk

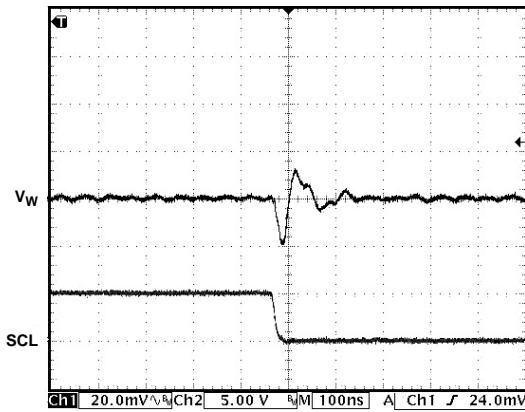


Figure 24. Digital Feedthrough

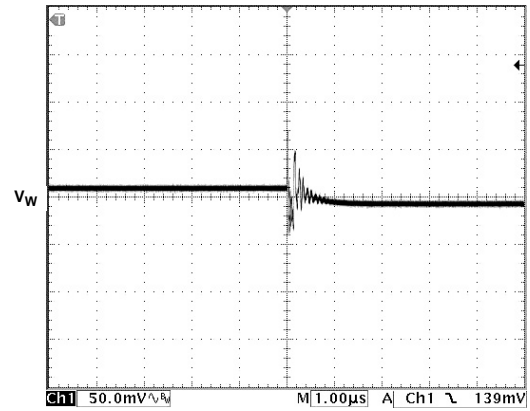


Figure 27. Midscale Glitch, Code 0x80 to 0x7F

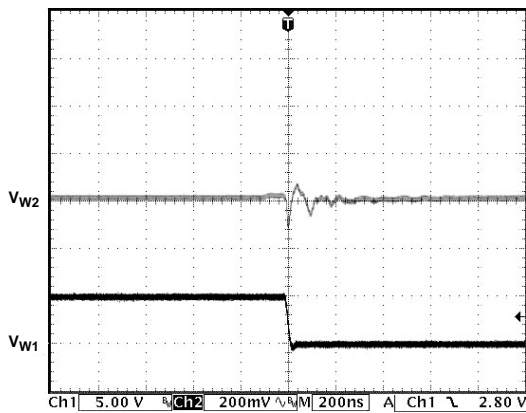


Figure 25. Digital Crosstalk

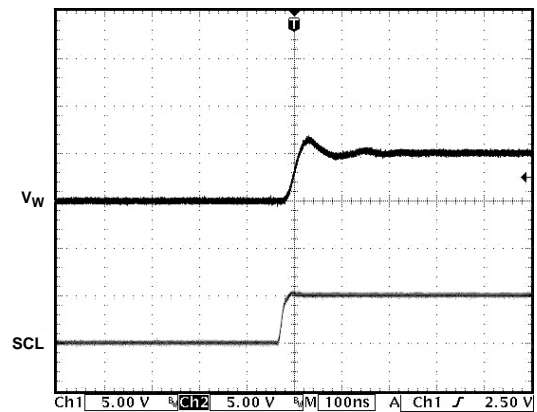


Figure 28. Large Signal Settling Time

TEST CIRCUITS

Figure 29 to Figure 36 illustrate the test circuits that define the test conditions used in the product specification tables.

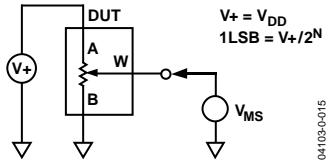


Figure 29. Potentiometer Divider Nonlinearity Error (INL, DNL)

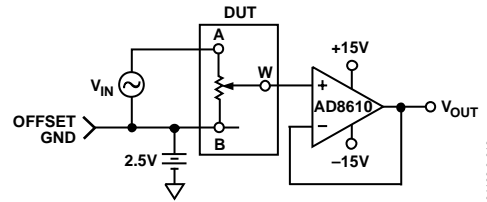


Figure 33. Test Circuit for Gain vs. Frequency

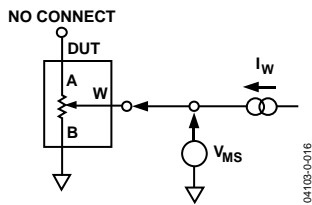


Figure 30. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

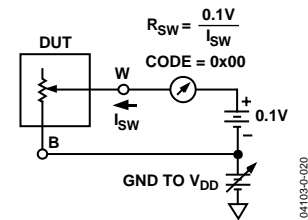


Figure 34. Incremental On Resistance

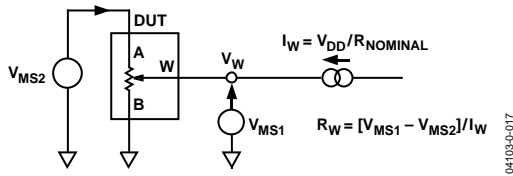


Figure 31. Wiper Resistance

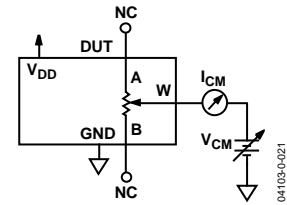


Figure 35. Common-Mode Leakage Current

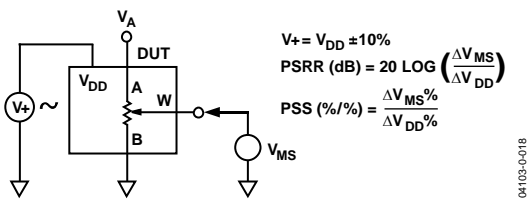


Figure 32. Power Supply Sensitivity (PSS, PSSR)

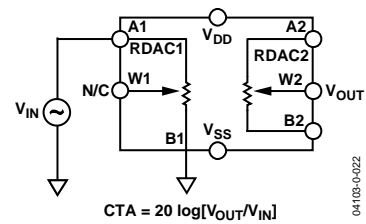


Figure 36. Analog Crosstalk

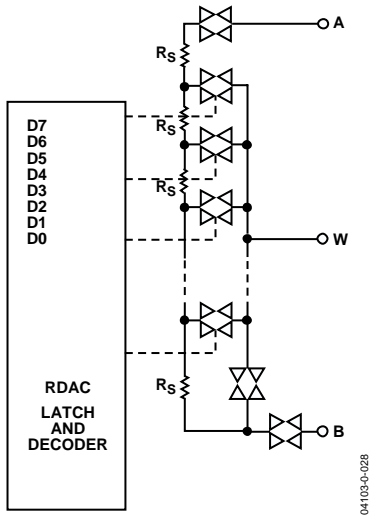


Figure 39. AD5172/AD5173 Equivalent RDAC Circuit

The general equation that determines the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + 2 \times R_W \quad (1)$$

where D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register, R_{AB} is the end-to-end resistance, and R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if $R_{AB} = 10 \text{ k}\Omega$ and the A terminal is open-circuited, the output resistance R_{WB} is set for the RDAC latch codes, as shown in Table 7.

Table 7. Codes and Corresponding R_{WB} Resistance

D (Dec.)	R_{WB} (Ω)	Output State
255	9,961	Full-Scale ($R_{AB} - 1 \text{ LSB} + R_W$)
128	5,060	Midscale
1	139	1 LSB
0	100	Zero-Scale (Wiper Contact Resistance)

Note that in the zero-scale condition, a finite wiper resistance of 100Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA . Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance, R_{WA} . When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{128} \times R_{AB} + 2 \times R_W \quad (2)$$

For $R_{AB} = 10 \text{ k}\Omega$ and the B terminal open-circuited, the following output resistance R_{WA} is set for the RDAC latch codes, as shown in Table 8.

Table 8. Codes and Corresponding R_{WA} Resistance

D (Dec)	R_{WA} (Ω)	Output State
255	139	Full-Scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero-Scale

Typical device-to-device matching is process-lot dependent and may vary by up to $\pm 30\%$. Because the resistance element is processed using thin film technology, the change in R_{AB} with temperature has a very low $35 \text{ ppm}/^\circ\text{C}$ temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A-B, W-A, and W-B can be at either polarity.

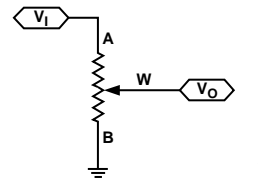


Figure 40. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V . Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values. Thus, the temperature drift reduces to $15 \text{ ppm}/^\circ\text{C}$.

ESD PROTECTION

All digital inputs—SDA, SCL, AD0, and AD1—are protected with a series input resistor and parallel Zener ESD structures, as shown in Figure 41 and Figure 42.

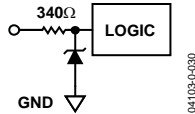


Figure 41. ESD Protection of Digital Pins

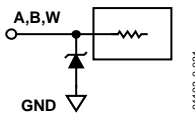


Figure 42. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5172/AD5173 V_{DD} to GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or GND are clamped by the internal forward-biased diodes (see Figure 43).

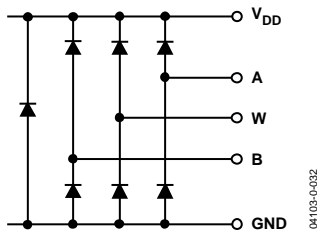


Figure 43. Maximum Terminal Voltages Set by V_{DD} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 43), it is important to power V_{DD} /GND before applying any voltage to terminals A, B, and W. Otherwise, the diode is forward biased such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is GND, V_{DD} , the digital inputs, and then VA/VB/VW. The relative order of powering VA, VB, VW, and the digital inputs is not important as long as they are powered after V_{DD} /GND.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the one-time programming and normal operating voltage supplies are applied to the same V_{DD} terminal of the device. The AD5172/AD5173 employ fuse link technology that requires 5.25 V to 5.5V to blow the internal fuses to achieve a given setting, but normal V_{DD} can be 2.7 V to 5.5V. Such dual-voltage requirements require isolation between the supplies if V_{DD} is lower than the required V_{DD_OTP} . The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 5.25 V to 5.5 V and must be able to provide a 100 mA transient current for 400 ms for successful one-time programming. Once the permanent setting programming is complete, the V_{DD_OTP} supply must be removed. The device then operates at V_{DD} and consumes only microamps of current. Figure 44 shows the simplest implementation to meet the dual voltage requirement with a jumper. This approach saves one voltage supply, but draws additional current and requires manual configuration.

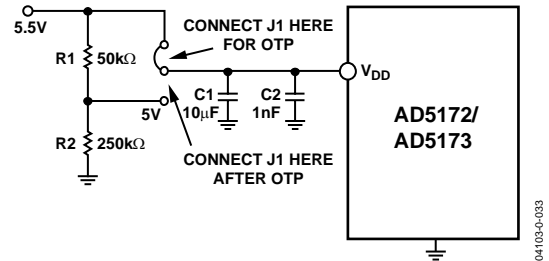


Figure 44. Power Supply Requirement

An alternate approach in 3.5 V to 5.25 V systems adds a signal diode between the system supply and the OTP supply for isolation, as shown in Figure 45.

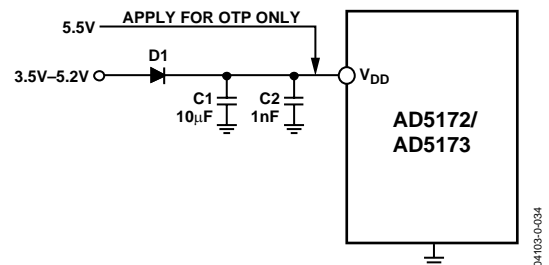


Figure 45. Isolate 5.5 V OTP Supply from 3.5 V to 5.25 V Normal Operating Supply. The V_{DD_OTP} supply must be removed once OTP is completed.

AD5172/AD5173

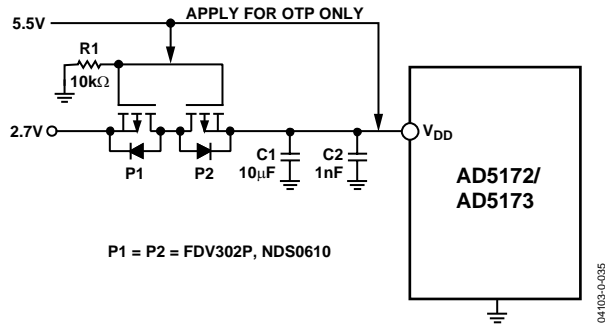


Figure 46. Isolate 5.5 V OTP Supply from 2.7 V Normal Operating Supply. The V_{DD_OTP} must be removed once OTP is completed.

For users who operate their systems at 2.7 V, use of the bidirectional low threshold P-Ch MOSFETs is recommended for the supply's isolation. As shown in Figure 46, this assumes that the 2.7 V system voltage is applied first, and that the P1 and P2 gates are pulled to ground, thus turning on P1 and subsequently P2. As a result, V_{DD} of the AD5172/AD5173 approaches 2.7 V. When the AD5172/AD5173 setting is found, the factory tester applies the V_{DD_OTP} to both the V_{DD} and the MOSFETs gates thus turning P1 and P2 off. The OTP command should be executed at this time to program the AD5172/AD5173 while the 2.7 V source is protected. Once the OTP is completed, the tester withdraws the V_{DD_OTP} and the AD5172/AD5173's setting is fixed permanently.

The AD5172/AD5173 achieve the OTP function by blowing internal fuses. Users should always apply the 5.25 V to 5.5 V one-time program voltage requirement at the first fuse programming attempt. Failure to comply with this requirement may lead to the change of fuse structures, rendering programming inoperable.

Poor PCB layout introduces parasitics that can affect fuse programming. Therefore, it is recommended to add a 1 μ F to 10 μ F tantalum capacitor in parallel with a 1 nF ceramic capacitor as close as possible to the V_{DD} pin. The type and value chosen for both capacitors are important. This combination of capacitor values provides both a fast response and larger supply current handling with minimum supply droop during transients. As a result, these capacitors increase the OTP programming success by not inhibiting the proper energy needed to blow the internal fuses. Additionally, C1 minimizes transient disturbance and low frequency ripple, while C2 reduces high frequency noise during normal operation.

LAYOUT CONSIDERATIONS

In PCB layout, it is a good practice to employ compact, minimum lead-length design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

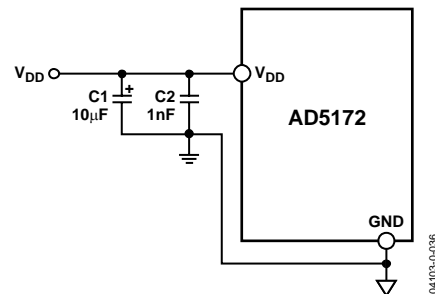


Figure 47. Power Supply Bypassing

EVALUATION SOFTWARE/HARDWARE

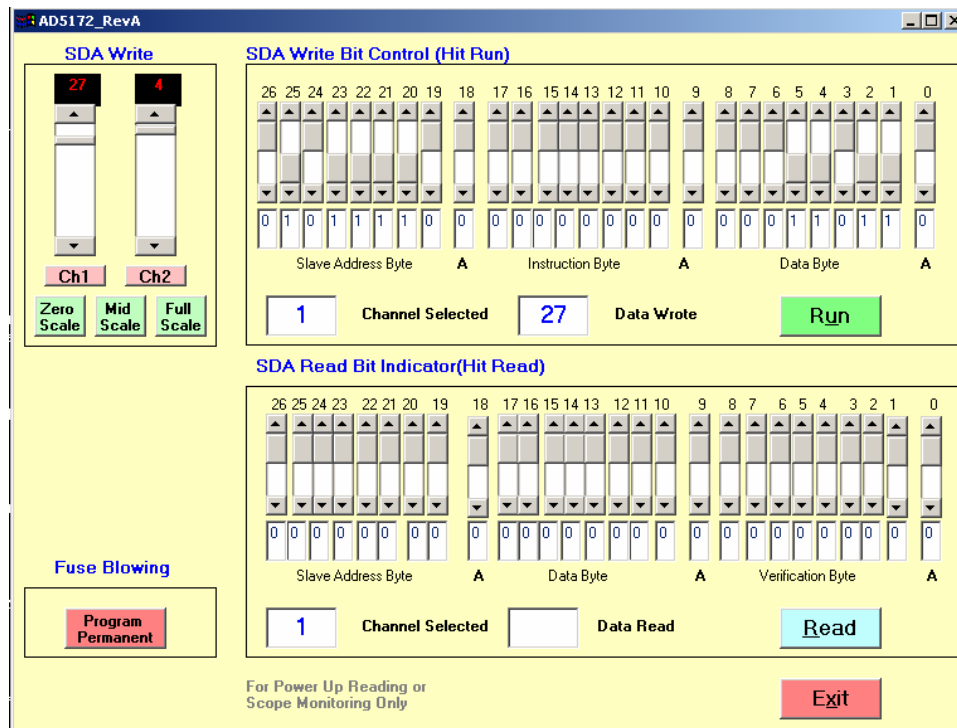


Figure 48. AD5172/AD5173 Computer Software Interface

There are two ways of controlling the AD5172/AD5173. Users can either program the devices with computer software or with external I²C controllers.

SOFTWARE PROGRAMMING

Taking advantage of the one-time programming feature, users may consider programming the device in the factory before shipping it to endusers. ADI offers a device programming software that can be implemented as an executable on PCs running Windows 95 or later. As a result, external controllers are not required, which significantly reduces development time. The program is easy to use and set up, and users do not need to have programming skills. Figure 48 shows the user interface. The software can be downloaded from www.analog.com.

Before one-time programming is set, the AD5172/AD5173 start at midscale after power-up. To increment or decrement the resistance, the user may simply move the scrollbars on the left. To write any specific value, the user should use the bit pattern in the upper screen and click Run. The format of writing data to the device is shown in Table 9. Once the desired setting is selected, click Program Permanent to blow the internal fuse links.

To read the validation bits and data out from the device, click Read. The format of the read bits is shown in Table 10.

To apply the device programming software in the factory, users must modify a parallel port cable and configure Pins 2, 3, 15, and 25 for SDA_write, SCL, SDA_read, and DGND, respectively, for the control signals (Figure 49). Users should also lay out the PCB of the AD5172/AD5173 with SCL and SDA pads, as shown in Figure 50, such that pogo pins can be inserted for factory programming.

AD5172/AD5173

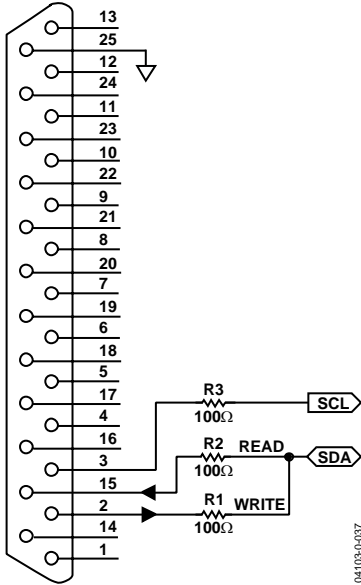


Figure 49. Parallel Port Connection. Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND.

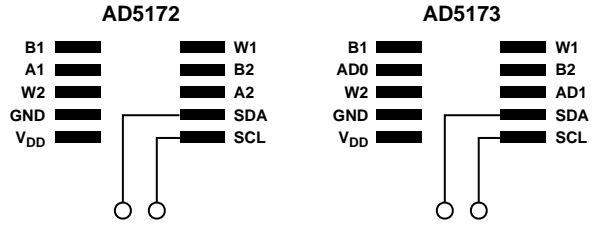


Figure 50. Recommended AD5172/AD5173 PCB Layout. The SCL and SDA pads allow pogo pins to be inserted so that signals can be communicated through the parallel port for programming (Figure 49).

I²C INTERFACE

Table 9. Write Mode

AD5172

S	0	1	0	1	1	1	1	\overline{W}	A	A0	SD	T	0	OW	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
Slave Address Byte									Instruction Byte							Data Byte												

AD5173

S	0	1	0	1	1	AD1	AD0	\overline{W}	A	A0	SD	T	0	OW	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
Slave Address Byte									Instruction Byte							Data Byte												

Table 10. Read Mode

AD5172

S	0	1	0	1	1	1	1	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	A	P
Slave Address Byte									Instruction Byte							Data Byte												

AD5173

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	A	P
Slave Address Byte									Instruction Byte							Data Byte												

The following is the legend for Table 9 and Table 10.

S = Start Condition

P = Stop Condition

A = Acknowledge

AD0, AD1 = Package Pin Programmable Address Bits

X = Don't Care

\overline{W} = Write

R = Read

A0 = RDAC Subaddress Select Bit

SD = Shutdown connects wiper to B terminal and open circuits the A terminal. It does not change contents of wiper register.

T = OTP Programming Bit. Logic 1 programs the wiper permanently.

OW = Overwrite the fuse setting and program the digital potentiometer to a different setting. Note that upon power-up, the digital potentiometer is preset to either midscale or fuse setting, depending on whether not the fuse link has been blown.

D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits.

E1, E0 = OTP Validation Bits.

0, 0 = Ready to Program.

1, 0 = Fatal Error. Some fuses not blown. Do not retry. Discard this unit.

1, 1 = Programmed Successfully. No further adjustments possible.

AD5172/AD5173

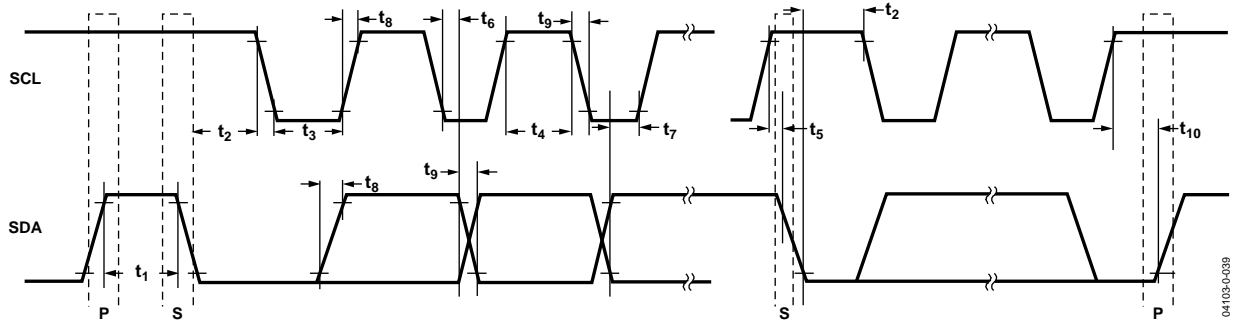


Figure 51. I²C Interface Detailed Timing Diagram

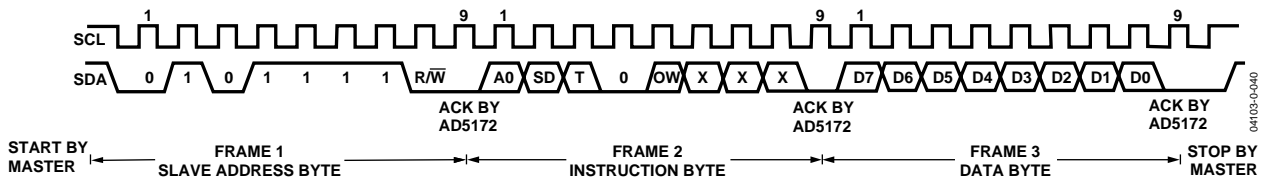


Figure 52. Writing to the RDAC Register—AD5172

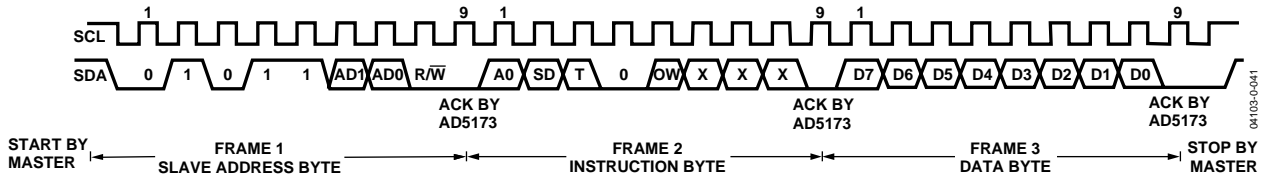


Figure 53. Writing to the RDAC Register—AD5173

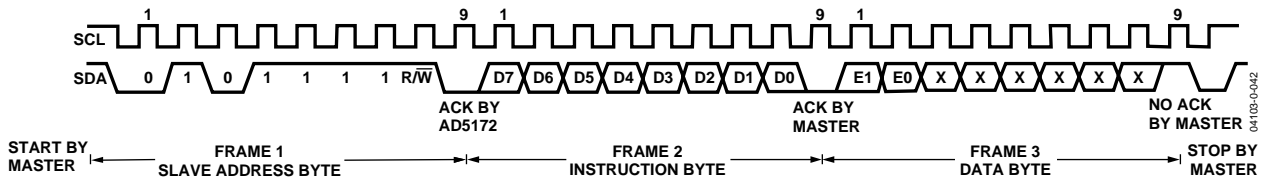


Figure 54. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5172

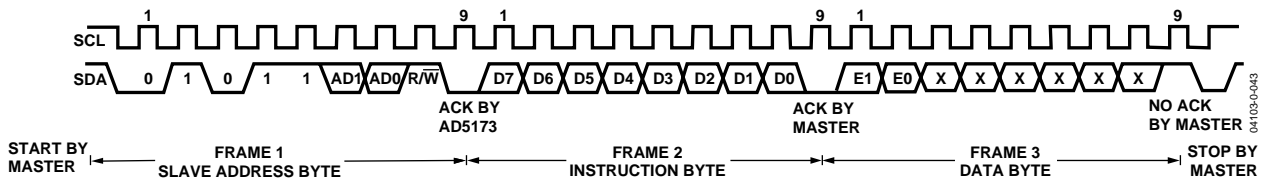


Figure 55. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5173

I²C-COMPATIBLE 2-WIRE SERIAL BUS

The 2-wire I²C serial bus protocol operates as follows.

The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 52 and Figure 53). The following byte is the slave address byte, which consists of the slave address followed by an R/W bit (this bit determines whether data is read from or written to the slave device). The AD5172 has a fixed slave address byte, whereas the AD5173 has two configurable address bits, AD0 and AD1 (see Figure 52 and Figure 53).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/W bit is high, the master reads from the slave device. If the R/W bit is low, the master writes to the slave device.

In write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is the RDAC subaddress select bit. A logic low selects Channel 1; a logic high selects Channel 2.

The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at terminal A while shorting the wiper to Terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC. Also, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

The third MSB, T, is the OTP programming bit. A logic high blows the internal fuses and programs the resistor setting permanently.

The fourth MSB must always be at Logic 0.

The fifth MSB, OW, is an overwrite bit. When raised to a logic high, OW allows the RDAC setting to be changed even after the internal fuses have been blown. However, once OW is returned to a Logic 0, the position of the RDAC returns to the setting prior to overwrite. Because OW is not static, if the device is powered off and on, the RDAC presets to midscale or to the setting at which the fuses were blown, depending on whether or not the fuses have been permanently set already.

The remainder of the bits in the instruction byte are don't cares (see Figure 52 and Figure 53).

After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 51).

In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference from write mode, where there are eight data bits followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 54 and Figure 55).

The channel of interest is the one that is previously selected in the write mode. When users need to read the RDAC values of both channels, they must program the first channel in write mode and then change to read mode to read the first channel value. After that, the user must change back to write mode with the second channel selected and read the second channel value in read mode. It is not necessary for users to issue the Frame 3 data byte in write mode for subsequent readback operation. Refer to Figure 54 and Figure 55 for the programming format.

Following the data byte, the validation byte contains two validation bits, E0 and E1. These bits signify the status of the one-time programming (see Figure 54 and Figure 55).

After all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition (see Figure 52 and Figure 53). In read mode, the master issues a No Acknowledge for the ninth clock pulse, i.e., the SDA line remains high. The master then brings the SDA line low before the 10th clock pulse, which goes high to establish a stop condition (see Figure 54 and Figure 55).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in write mode, the RDAC output is updated on each successive byte. If different instructions are needed, write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

AD5172/AD5173

Table 11. Validation Status

E1	E0	Status
0	0	Ready for programming.
1	0	Fatal error. Some fuses not blown. Do not retry. Discard this unit.
1	1	Successful. No further programming is possible.

Multiple Devices on One Bus (AD5173 Only)

Figure 56 shows four AD5173s on the same serial bus. Each has a different slave address because the states of their AD0 and AD1 pins are different. This allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C-compatible interface.

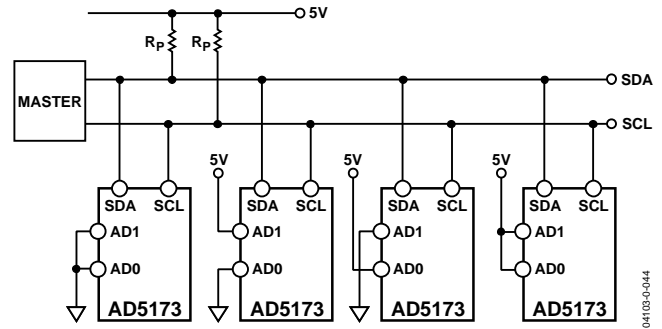
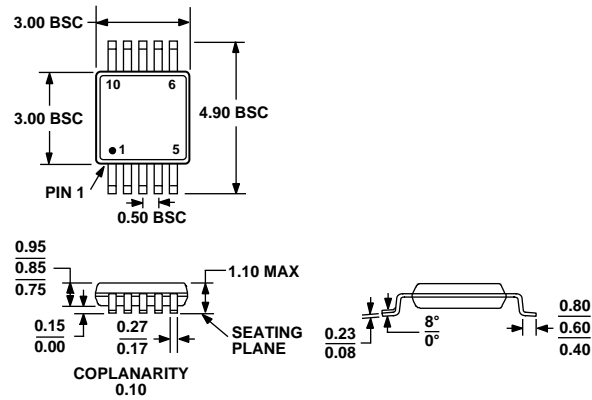


Figure 56. Multiple AD5173s on One I²C Bus

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187BA

Figure 57. 10-Lead Mini Small Outline Package [MSOP] (RM-10)
 Dimensions shown in millimeters

AD5172/AD5173

ORDERING GUIDE

Model	R _{AB} (kΩ)	Temperature Range	Package Description	Package Option	Branding
AD5172BRM2.5	2.5	-40°C to +125°C	MSOP-10	RM-10	D0U
AD5172BRM2.5-RL7	2.5	-40°C to +125°C	MSOP-10	RM-10	D0U
AD5172BRM10	10	-40°C to +125°C	MSOP-10	RM-10	D0V
AD5172BRM10-RL7	10	-40°C to +125°C	MSOP-10	RM-10	D0V
AD5172BRM50	50	-40°C to +125°C	MSOP-10	RM-10	D10
AD5172BRM50-RL7	50	-40°C to +125°C	MSOP-10	RM-10	D10
AD5172BRMZ50 ¹	50	-40°C to +125°C	MSOP-10	RM-10	D10
AD5172BRMZ50-RL7 ¹	50	-40°C to +125°C	MSOP-10	RM-10	D10
AD5172BRM100	100	-40°C to +125°C	MSOP-10	RM-10	D11
AD5172BRM100-RL7	100	-40°C to +125°C	MSOP-10	RM-10	D11
AD5172EVAL ²			Evaluation Board		
AD5173BRM2.5	2.5	-40°C to +125°C	MSOP-10	RM-10	D1K
AD5173BRM2.5-RL7	2.5	-40°C to +125°C	MSOP-10	RM-10	D1K
AD5173BRM10	10	-40°C to +125°C	MSOP-10	RM-10	D1L
AD5173BRM10-RL7	10	-40°C to +125°C	MSOP-10	RM-10	D1L
AD5173BRM50	50	-40°C to +125°C	MSOP-10	RM-10	D1M
AD5173BRM50-RL7	50	-40°C to +125°C	MSOP-10	RM-10	D1M
AD5173BRM100	100	-40°C to +125°C	MSOP-10	RM-10	D1N
AD5173BRM100-RL7	100	-40°C to +125°C	MSOP-10	RM-10	D1N
AD5173EVAL ²			Evaluation Board		

¹ Z = Pb-free part.

² The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

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