3.3V 28Mbps-2.5Gbps AnyRate™ CLOCK AND DATA RECOVERY

FEATURES

- **3.3V power supply**
- **Complies with Bellcore, ITU/CCITT and ANSI specifications for applications such as OC-1, OC-3, OC-12, OC-48*, and ATM**
- **Compatible with FDDI, Gigabit Ethernet, Fibre Channel, 2X Fibre Channel, SMPTE 259 and 292, and proprietary applications**
- **Low power**
- **Clock and data recovery from 28Mbps up to 2.5Gbps NRZ data stream**
- **Selectable reference frequencies via programmable multiplier**
- **Differential PECL and CML high-speed serial outputs**
- **Line receiver input: no external buffering needed**
- **Link fault indication**
- **100K ECL compatible I/O**
- **Available in 64-Pin EP-TQFP package**

*Meets OC-48 Jitter Tolerance and Transfer

APPLICATIONS

- **Transponders and section repeaters**
- **Multiplexer's: access, add drop (ADM), and terminal (TM)**
- **SONET/SDH/ATM: -based transmission systems, modules, and test equipment**
- **Terabit routers and broadband cross-connects**
- **Fibre optic test equipment**
- **HDTV switching and transmission**

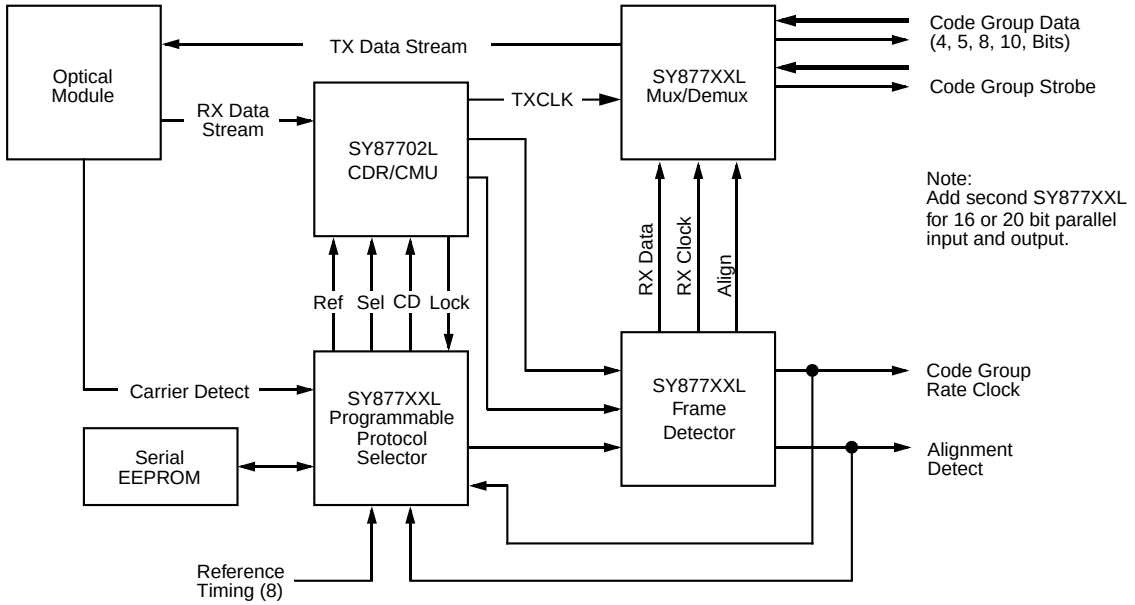
DESCRIPTION

The SY87702L is a complete Clock Recovery and Data retiming integrated circuit for data rates from 28Mbps up to 2.5Gbps NRZ. The device is ideally suited for SONET/SDH/ATM, Fibre Channel, and Gigabit Ethernet applications, as well as other high-speed data transmission applications.

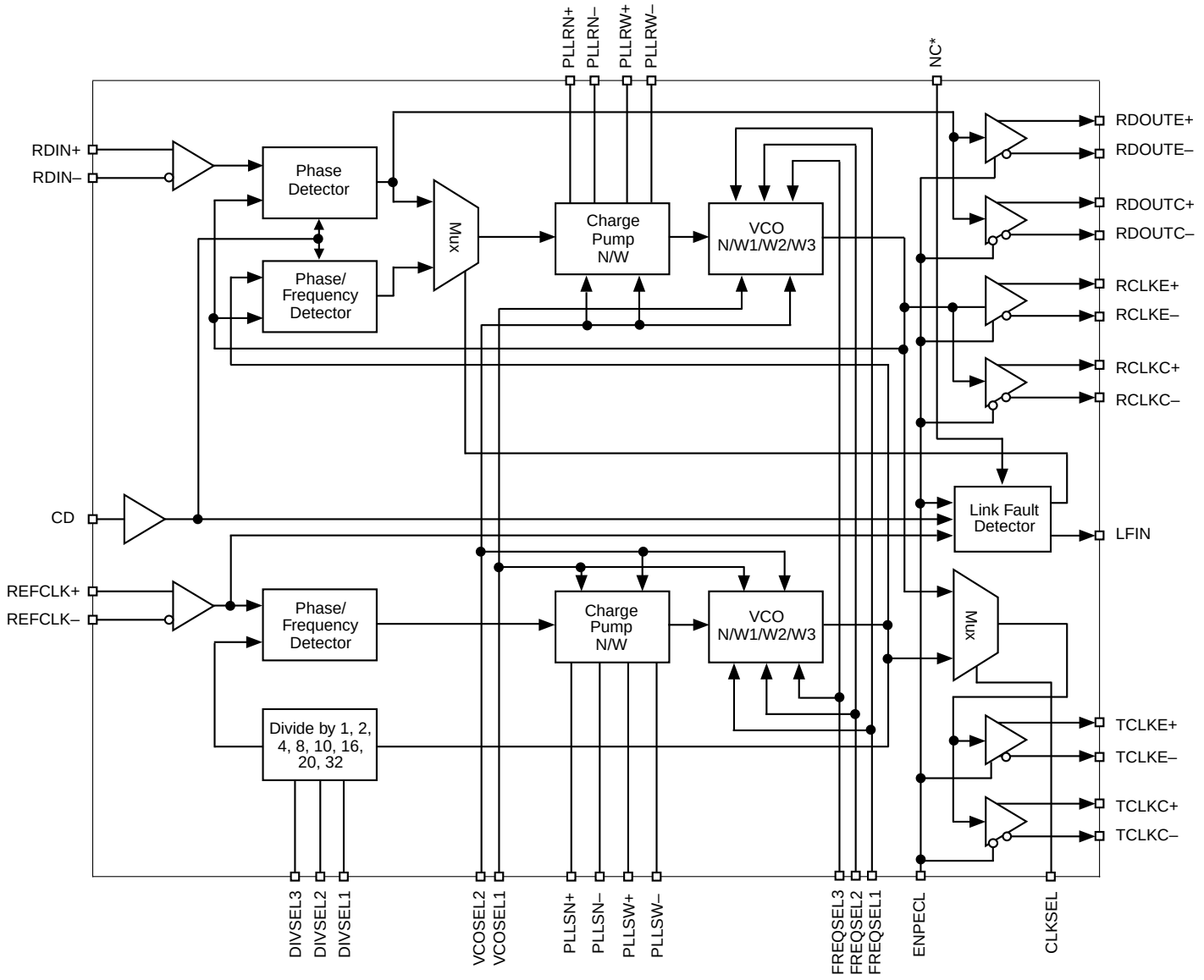
Clock recovery and data retiming is performed by synchronizing the on-chip VCO directly to the incoming data stream. The VCO center frequency is controlled by the reference clock frequency and the selected divide ratio. On-chip clock generation is performed through the use of a frequency multiplier PLL and can be used as a Clock Multiplier Unit (CMU). The integrated CMU can provide this clock signal at the TCLK outputs. Additionally, the TCLK output can be selected to provide a copy of the RCLK frequency.

For SONET/SDH applications, the SY87702L includes a Link Fault Detection circuit. This circuit, enabled by the output of an optical module driving the CD input low, causes the recovery PLL of the SY87702L to lock to the reference clock's multiplied frequency under Loss-of-Signal conditions. This low jitter clock is provided at the RCLK outputs and is at the same frequency as that provided at the TCLK output.

SYSTEM BLOCK DIAGRAM

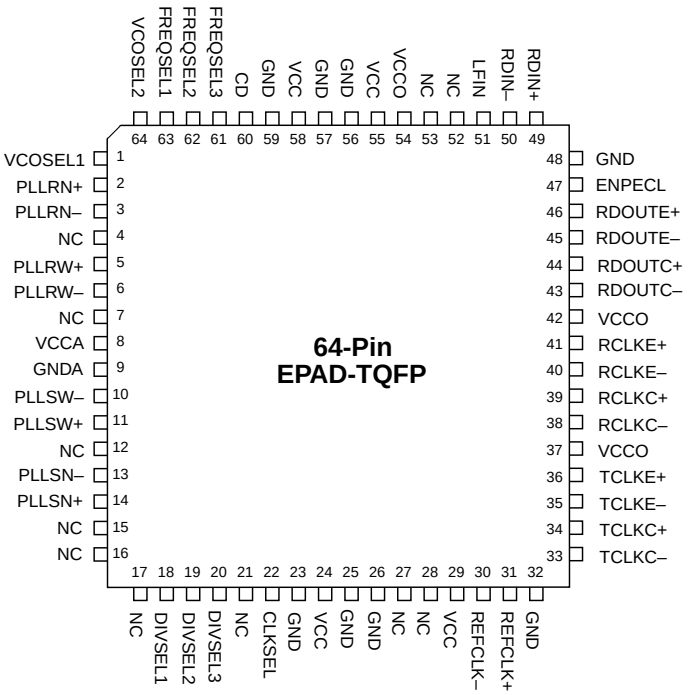


FUNCTIONAL BLOCK DIAGRAM



* Do not connect.

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

Clock Recovery

Clock Recovery, as shown in the block diagram, generates a clock that is at the same frequency as the incoming data bit rate at the Serial Data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency detector. Output pulses from the detector indicate the required direction of phase correction. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability, without incoming data, is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the Frequency of the incoming signal varies by greater than approximately 1000ppm with respect to the synthesizer frequency, the PLL will be declared out of lock, and the PLL will lock to the multiplied frequency of the reference clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a 30µs data stream of continuous 1's or 0's for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL provides jitter tolerance which is better than the specified tolerance in GR-253-CORE.

PIN NAMES

INPUTS

RDIN± [Serial Data Input] – Differential PECL

This differential input accepts the receive serial data stream. An internal receive PLL recovers the embedded clock (RCLK) and data (RDOUT) information. The incoming data rate can be within one of ten frequency ranges, or can be one of five specific frequencies, depending on the state of the FREQSEL and VCOSEL pins. The RDIN– pin has an internal 75KΩ resistor tied to V_{CC}.

REFCLK± [Reference Clock] – Differential PECL

This input is used as the reference for the internal frequency synthesizer and the "training" frequency for the receiver PLL to keep it centered in the absence of data coming in on the RDIN input. The input frequency to REFCLK is limited to 325MHz or less, depending on the setting on the DIVSEL signals. The REFCLK– pin has an internal 75KΩ resistor tied to V_{CC}.

CD [Carrier Detect] – PECL Input

This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output of optical modules or from external transition detection circuitry. When this input is HIGH, the input data stream (RDIN) is recovered normally by the Receive PLL. When this input is LOW, the data on the RDIN input will be internally forced to a constant LOW, the data output RDOUT will remain LOW, the Link Fault Indicator output LFIN forced LOW, and the clock recovery PLL forced to lock onto the clock frequency generated from REFCLK.

VCOSEL1, VCOSEL2 [VCO Select] – TTL Inputs

These inputs select the VCO frequency range via either one of three wide-band PLLs, or a SONET/SDH specific narrow-band PLL. Only the selected PLL is enabled. All other PLL's are disabled. Please refer to Table 1.

VCOSEL1	VCOSEL2	Choice
0	0	SONET/SDH
0	1	1.8 to 2.5GHz
1	0	1.25 to 1.8GHz
1	1	0.650 to 1.30GHz

Table. 1

FREQSEL1, ..., FREQSEL3 [Frequency Select] – TTL Inputs

These inputs select the output clock frequency range, as shown in Table 2.

FREQSEL1	FREQSEL2	FREQSEL3	VCOCLK Divider
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	6
1	0	0	8
1	0	1	12
1	1	0	16
1	1	1	24

Table 2.

DIVSEL1, ..., DIVSEL3 [Divider Select] – TTL Inputs

These inputs select the ratio between the output clock frequency (RCLK/TCLK) and the REFCLK input frequency as shown in Table 3. Please note that the divide by 32 selection, “011”, is only available for use when FREQSEL are set to “000.”

DIVSEL1	DIVSEL2	DIVSEL3	REFCLK Multiplier
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	32
1	0	0	8
1	0	1	10
1	1	0	16
1	1	1	20

Table 3.

CLKSEL [Clock Select] – TTL Input

This input is used to select either the recovered clock of the receiver PLL (CLKSEL = HIGH) or the clock of the frequency synthesizer (CLKSEL = LOW) to the TCLK outputs.

ENPECL [Enable PECL] – TTL Input

This input, when HIGH (ENPECL = 1), enables the differential PECL outputs TCLKE± RDOUTE±, and RCLKE±. It also disables the CML outputs, by setting TCLKC+, RDOUTC+, and RCLKC+ logic HIGH and setting TCLKC–, RDOUTC–, and RCLKC– logic LOW.

When set LOW (ENPECL = 0), this signal enables the differential CML outputs TCLKC±, RDOUTC±, and RCLKC±. It also disables the PECL outputs by setting TCLKE+, RDOUTE+, and RCLKE+ logic HIGH and setting TCLKE–, RDOUTE–, and RCLKE– logic LOW.

OUTPUTS

LFIN [Link Fault Indicate] – O.C. TTL Output

This output indicates the status of the input data stream RDIN. LFIN will go HIGH if CD is HIGH and RDIN is within the frequency range of the Receive PLL (as per ALRSEL). LFIN is an asynchronous output.

RDOUTE± [Receive Data Out] – Differential PECL

These ECL 100K outputs represent the recovered data from the input data stream (RDIN). This recovered data is sampled on the falling edge of RCLK.

RDOUTC± [Receive Data Out] – Differential CML

This is the CML version of RDOUTE±.

RCLKE± [Receive Clock Out] – Differential PECL

These ECL 100K outputs represent the recovered clock used to sample the recovered data (RDOUT).

RCLKC± [Receive Clock Out] – Differential CML

This is the CML version of RCLKE±.

TCLKE± [Transmit Clock Out] – Differential PECL

These ECL 100K outputs represent either the recovered clock (CLKSEL = HIGH) used to sample the recovered data (RDOUT) or the transmit clock of the frequency synthesizer (CLKSEL = LOW).

TCLKC± [Transmit Clock Out] – Differential CML

This is the CML version of TCLKE±.

INPUTS/OUTPUTS

PLLSN+, PLLSN– [Clock Synthesis Loop Filter]

External loop filter pins for the clock synthesis narrow-band PLL.

PLLSW+, PLLSW– [Clock Synthesis Loop Filter]

External loop filter pins for the clock synthesis wide-band PLLs.

PLLRN+, PLLRN– [Clock Recovery Loop Filter]

External loop filter pins for the clock recovery narrow-band PLL.

PLLRW+, PLLRW– [Clock Recovery Loop Filter]

External loop filter pins for the clock recovery wide-band PLLs.

OTHERS

VCC Supply Voltage
VCCO Output Supply Voltage
VCCA Analog Supply Voltage
GND Ground
GNDA Analog Ground
NC These pins are for factory test, and are to be left unconnected during normal use.

DESCRIPTION

General

The SY87702L is a complete clock and data recovery circuit, capable of dealing with NRZ data rates from 28Mbps through to 2.5Gbps. A reference PLL is used as a frequency synthesizer, both to multiply a clock to the desired transmit rate, and to train the recovery PLL in preparation for actual data recovery.

VCO Selection

SY87702L has four complete VCO circuits. Depending of the application and the frequency range, any one of these four perform data recovery.

As indicated by the VCO selection table, there are three general purpose VCOs, covering one of three frequency ranges. However, to extend the range of the device, the output of the VCO may be divided down.

In the case of the two highest frequency VCO, this divisor is always set to 1. For the lowest frequency VCO, the FREQSEL pins select which divisor, and hence, which range of frequencies the VCO will work over.

In addition, for SONET/SDH applications, there is a narrow band, extremely low jitter PLL. It also uses the FREQSEL divisor to choose the correct SONET/SDH frequency.

The various combinations of FREQSEL and VCOSEL are not arbitrary, but are limited to the subset shown in Table 4, where the range column indicates frequency in Mbps.

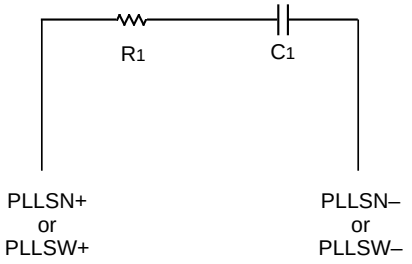
VCOSEL1	VCOSEL2	FREQSEL1	FREQSEL2	FREQSEL3	Range (Mbps)
0	0	0	0	0	2488 (OC48)
0	0	0	0	1	1244
0	0	0	1	0	622 (OC12)
0	0	1	0	0	311
0	0	1	1	0	155 (OC3)
0	1	0	0	0	1800–2500
0	1	0	0	1	900–1250(1)
1	0	0	0	0	1250–1800
1	1	0	0	0	650–1300(2)
1	1	0	0	1	325–650(3)
1	1	0	1	0	163–325
1	1	0	1	1	109–216
1	1	1	0	0	82–162
1	1	1	0	1	55–108
1	1	1	1	0	41–81
1	1	1	1	1	28–54

Table 4.(4)

NOTES:

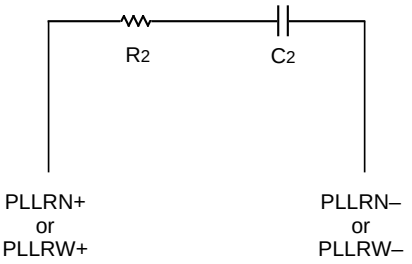
1. Suggested range for Fibre Channel applications.
2. REFCLK multiplier of 2 is not allowed in this range.
3. REFCLK multiplier of 1 is not allowed in this range.
4. Combinations of VCOSEL and FREQSEL other then those in this table result in undefined behavior, and should not be used.

LOOP FILTER COMPONENTS(1)



R1 = 1.2kΩ
C1 = 1.0µF (X7R Dielectric)

Figure 1. R1 Filter Component



R2 = 1.8kΩ
C2 = 1.0µF (X7R Dielectric)

Figure 2. R2 Filter Component

NOTE:

1. Suggested Values. Values may vary for different applications.

CML OUTPUT DIAGRAM

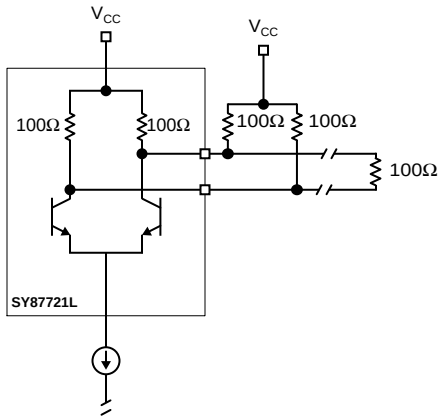


Figure 3. 50Ω Load CML Output

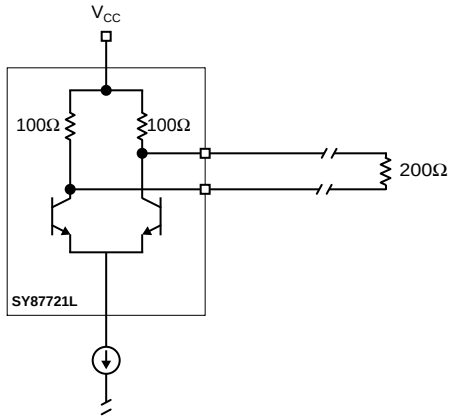
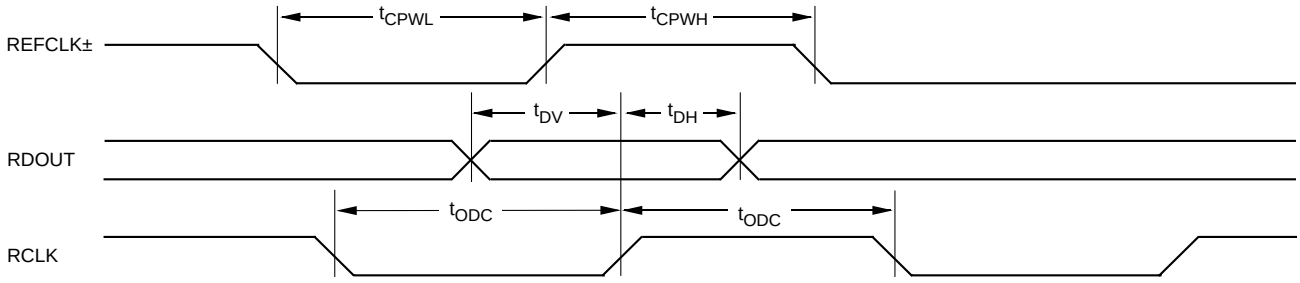


Figure 4. 100Ω Load CML Output

TIMING WAVEFORMS



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_{IN}	Input Voltage	–0.5 to V_{CC}	V
I_{OUT}	ECL Output Current –Continuous –Surge	50 100	mA
I_{CMLOUT}	CML Output Current	30	mA
T_{store}	Storage Temperature Range	–65 to +150	°C
T_A	Operating Temperature Range	–40 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; GND = GNDA = 0V; $T_A = –40°C$ to $+85°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	3.15	3.3	3.45	V	
I_{CC}	Power Supply Current	—	400	—	mA	

100K PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; GND = GNDA = 0V; $T_A = –40°C$ to $+85°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	$V_{CC} – 1.165$	—	$V_{CC} – 0.880$	V	
V_{IL}	Input LOW Voltage	$V_{CC} – 1.810$	—	$V_{CC} – 1.475$	V	
I_{IL}	Input LOW Current	0.5	—	—	µA	$V_{IN} = V_{IL}$(Min)
V_{OH}	Output HIGH Voltage	$V_{CC} – 1.075$	—	$V_{CC} – 0.830$	V	50Ω to V_{CC} –2V
V_{OL}	Output LOW Voltage	$V_{CC} – 1.860$	—	$V_{CC} – 1.570$	V	50Ω to V_{CC} –2V

CML DC ELECTRICAL CHARACTERISTICS[1]

$V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; GND = GNDA = 0V; $T_A = –40°C$ to $+85°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	—	$V_{CC} – 0.025$	—	V	
V_{OL}	Output LOW Voltage	—	$V_{CC} – 0.400$ $V_{CC} – 0.200$	—	V	100Ω Environment 50Ω Environment

NOTE:

1. Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in the 100Ω environment and a 200mV swing in the 50Ω environment. Refer to the “CML Output” diagram for more details.

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; GND = GNDA = 0V; $T_A = –40°C$ to $+85°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	—	V	
V_{IL}	Input LOW Voltage	—	—	0.8	V	
I_{IH}	Input HIGH Current	— —	— —	+20 +100	µA µA	$V_{IN} = 2.7V$, V_{CC} = Max. $V_{IN} = V_{CC}$, V_{CC} = Max.
I_{IL}	Input LOW Current	—	—	–300	µA	$V_{IN} = 0.5V$, V_{CC} = Max.
I_{OLK}	Output Leakage Current	—	—	500	µA	$V_{OUT} = V_{CC}$
V_{OL}	Output LOW Voltage	—	—	0.5	V	I_{OL} = 4mA

AC ELECTRICAL CHARACTERISTICS

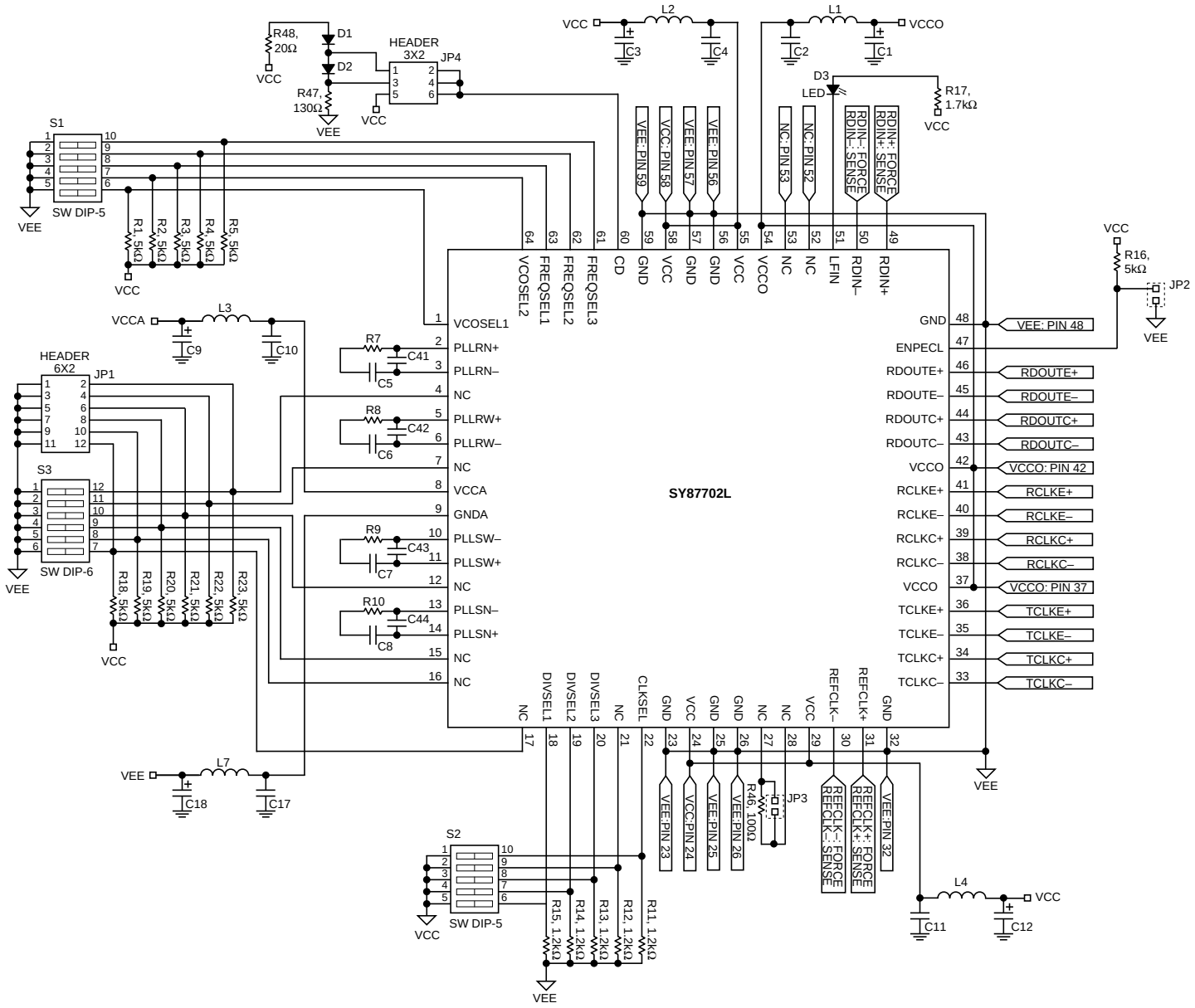
$V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; GND = GNDA = 0V; $T_A = –40°C$ to $+85°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
	RCLK, TCLK Output Jitter(1)	—	—	0.010	UI rms	REFCLK Multiplier = 16
	Lock Range/Training Range	1000	—	—	ppm	
	Acquisition Lock Time	—	15	—	µs	> 25% transition density
	RDIN Maximum Data Rate	2.5	—	—	Gbps	
	REFCLK Maximum Frequency	—	—	325	MHz	
t_{CPWH}	REFCLK Pulse Width High	1.2	—	—	ns	
t_{CPWL}	REFCLK Pulse Width Low	1.2	—	—	ns	
t_{IRF}	REFCLK Input Rise/Fall Time (20% to 80%)	—	—	1.0	ns	
t_{ODC}	Output Duty Cycle (RCLK/TCLK)	45	—	55	% of UI	
t_{RE} t_{FE}	ECL Output Rise/Fall Time (20% to 80%)	—	200	300	ps	50Ω to V_{CC}–2V
t_{RC} t_{FC}	CML Output Rise/Fall Time (20% to 80%)	—	65	120	ps	No Load
t_{DV}	Data Valid	100	—	—	ps	
t_{DH}	Data Hold	100	—	—	ps	

NOTE:

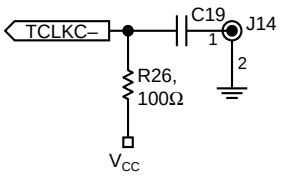
1. Except at OC-48.

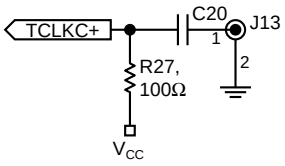
EVALUATION BOARD SCHEMATIC

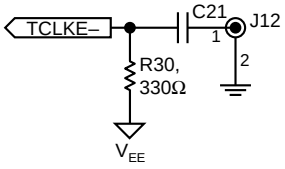


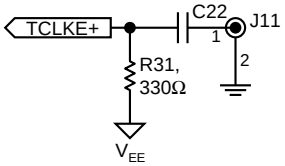
EVALUATION BOARD I/O TERMINATION SCHEMES

TCLK OUTPUTS

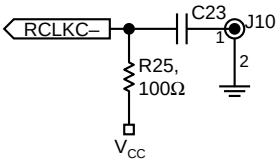


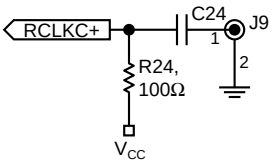


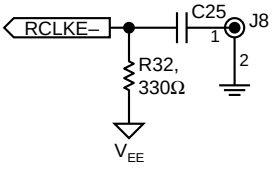


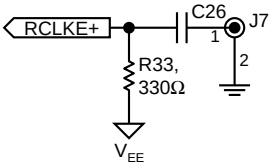


RCLK OUTPUTS

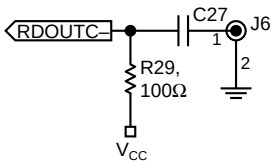


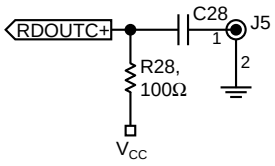


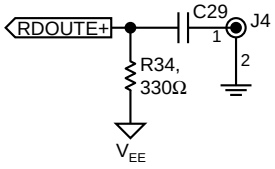


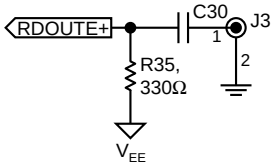


RDOUT INPUTS

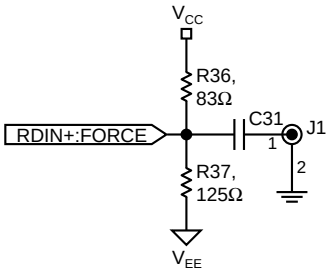


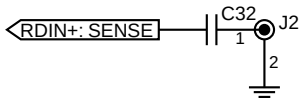


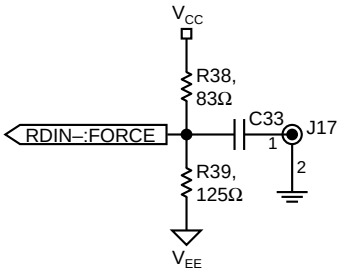


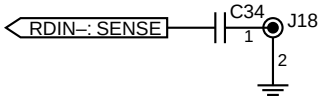


RDIN INPUTS







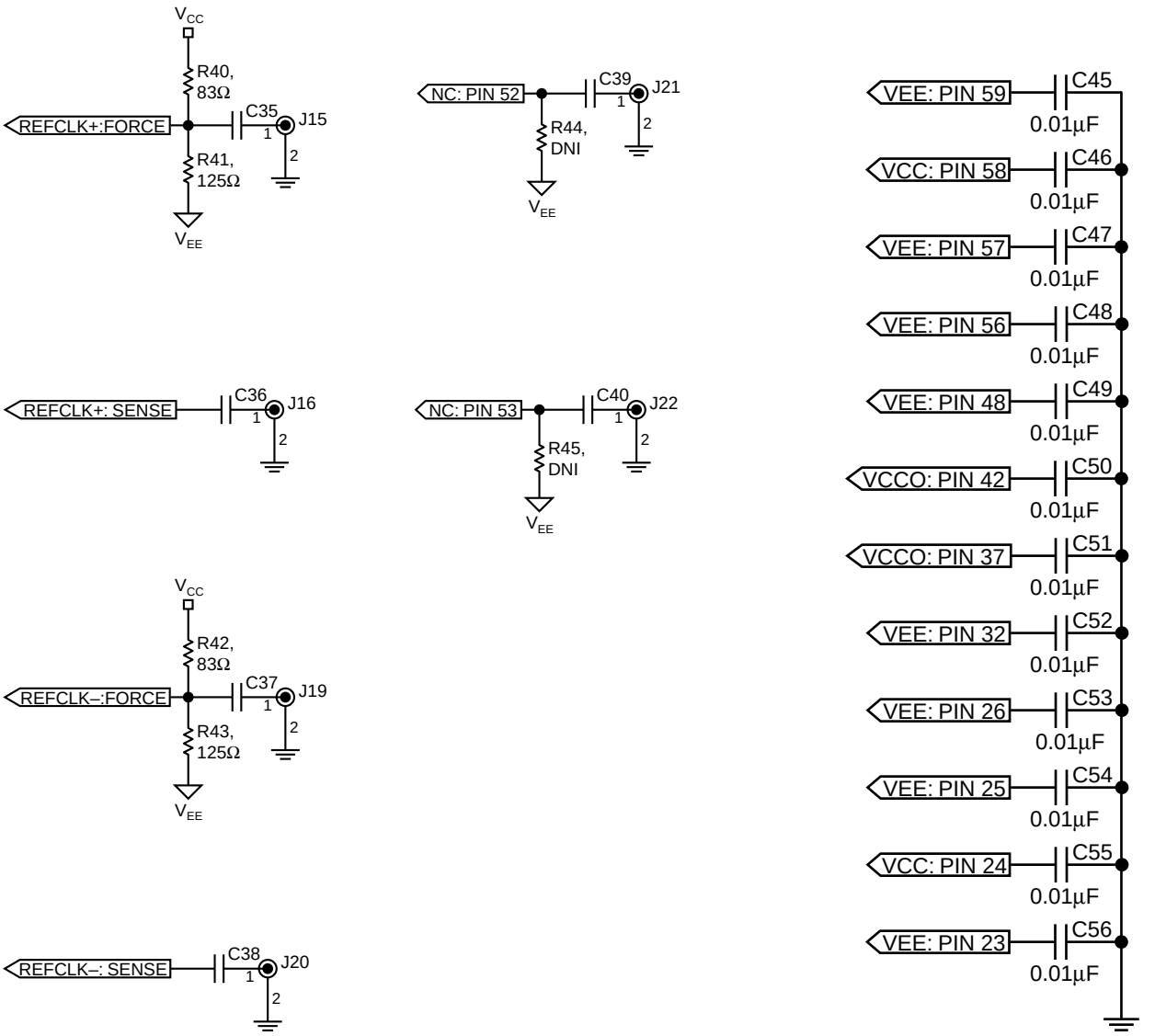


NOTES:

1. For AC coupling, include capacitors C19 thru C31, C33, C35 and C37.
2. If DC coupling, remove resistors R36 thru R43.
3. For 50Ω CML systems, include resistors R24–R29.
4. For 100Ω CML systems, see Figure 3.

REFCLK INPUTS

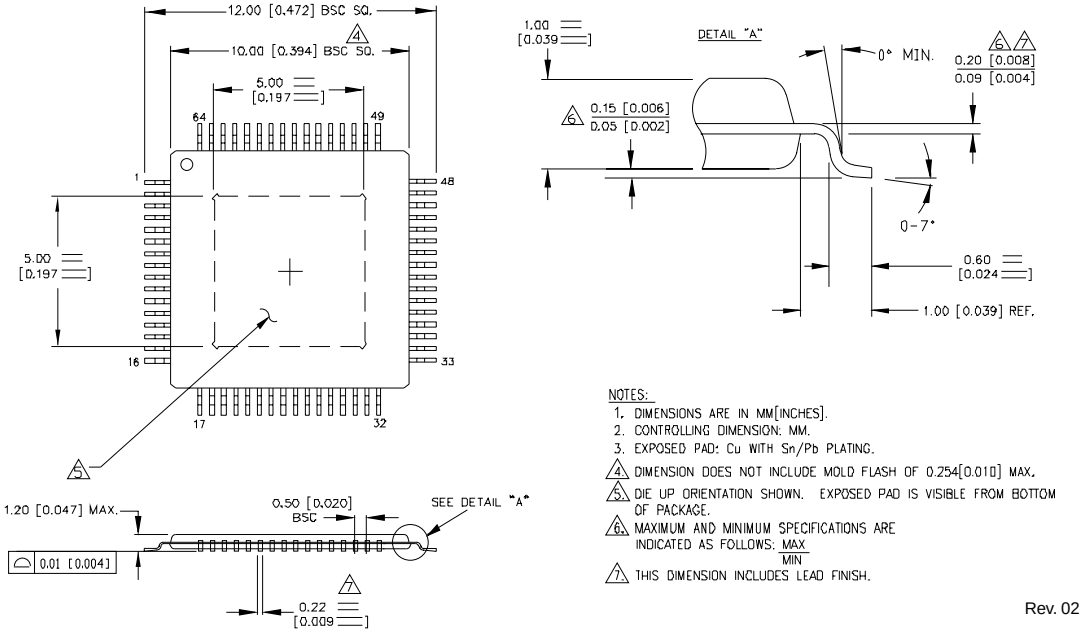
NC (FUTURE REV. OUTPUT)



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY87702LHI	H64-1	Industrial

64 LEAD EPAD H QUAD FLATPACK (H64-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 02

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