PROGRAMMABLE FLEXPC™ CLOCK FOR P4 PROCESSOR

IDTCV123

FEATURES:

- **One high precision PLL for CPU, with SSC and N programmable**
- **One high precision PLL for SRC/PCI/SATA, SSC and N programmable**
- **One high precision PLL for 96MHz/48MHz**
- **Band-gap circuit for differential outputs**
- **Supports spread spectrum modulation, down spread 0.5%**
- **Supports SMBus block read/write, index read/write**
- **Selectable output strength for REF**
- **Allows for CPU frequency to change to a higher frequency for maximum system computing power**
- **Available in SSOP package**

OUTPUTS:

- **2*0.7V current –mode differential CPU CLK pair**
- **8*0.7V current –mode differential SRC CLK pair, one dedicated for SATA**
- **One CPU_ITP/SRC selectable CLK pair**
- **8*PCI, 3 free running, 33.3MHz**
- **1*96MHz, 1*48MHz**
- **2*REF**

DESCRIPTION:

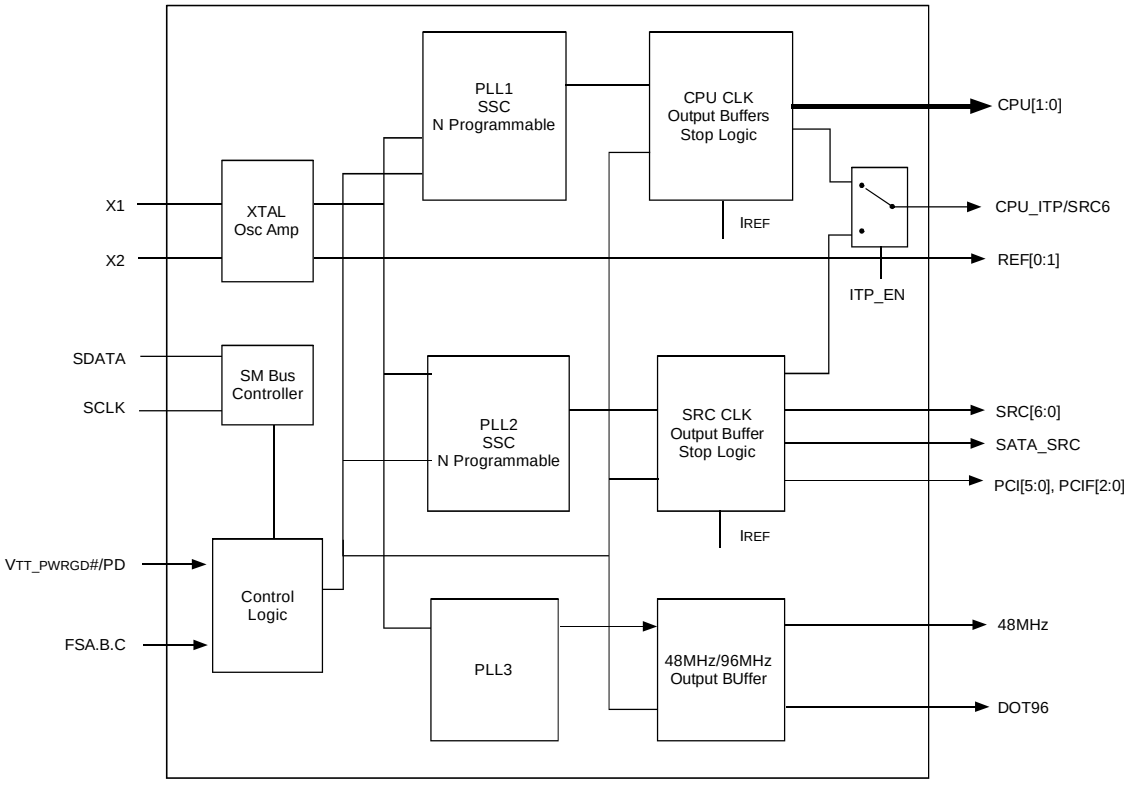
IDTCV123 is a 56 pin clock device. The CPU output buffer is designed to support up to 400MHz processor. This chip has three PLLs inside for CPU/SRC/PCI, SATA, and 48MHz/DOT96 IO clocks. One dedicated PLL for Serial ATA clock provides high accuracy frequency. This device also implements Band-gap referenced I_{REF} to reduce the impact of V_{DD} variation on differential outputs, which can provide more robust system performance.

Static PLL frequency divide error can be as low as 36 ppm, worse case 114 ppm, providing high accuracy output clock. Each CPU/SRC/PCI, SATA clock has its own Spread Spectrum selection, which allows for isolated changes instead of affecting other clock groups.

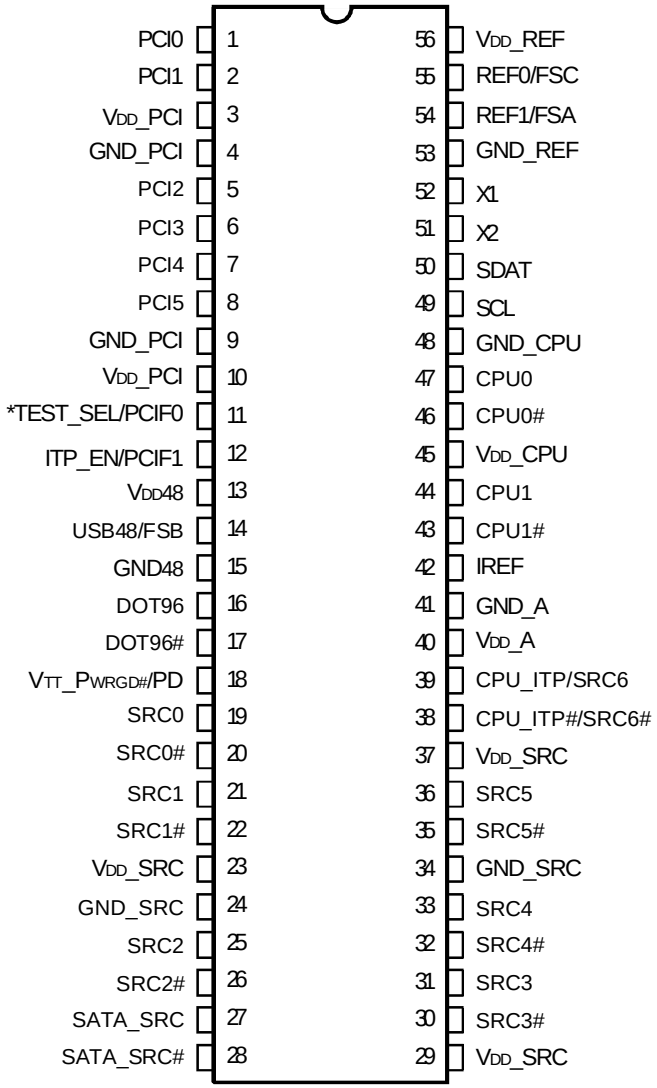
KEY SPECIFICATION:

- **CPU/SRC CLK cycle to cycle jitter < 85ps**
- **SATA CLK cycle to cycle jitter < 85ps**
- **PCI CLK cycle to cycle jitter < 250ps**
- **Static PLL frequency divide error < 114 ppm**
- **Static PLL frequency divide error for 48MHz < 5 ppm**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



* = Internal pull down

SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
VDDA	3.3V Core Supply Voltage		4.6	V
VDDIN	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
TSTG	Storage Temperature	–65	+150	°C
TAMBIENT	Ambient Operating Temperature	0	+70	°C
TCASE	Case Temperature		+115	°C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ITP_EN	pin 38	pin 39
1	CPUC2_ITP	CPUT_ITP
0	SRCC6	SRCT6

TEST CLARIFICATION TABLE

HW TEST_SEL/ PCICLK_F0	SW TEST SELECT BIT B6b6	OUTPUT	Comments
0	0	Normal	Normal Operation
1	X	Hi-Z	Power-up with TEST_SEL =1 to enter test mode. Cycle power with TEST_SEL = 0 to disable test mode
0	1	Hi-Z	If TEST_SEL HW pin is 0 during power-up, test mode can be invoked through B6b6. Cycle power with TEST_SEL = 0 to disable test mode.

FREQUENCY SELECTION TABLE

FSC, B, A	CPU Mode, MHz	SRC4	SRC[3:1], SRC[7:5]	PCI	USB	DOT96	REF
101	100	100	100	33.3	48	96	14.318
001	133	100	100	33.3	48	96	14.318
011	166	100	100	33.3	48	96	14.318
010	200	100	100	33.3	48	96	14.318
000	266	100	100	33.3	48	96	14.318
100	333	100	100	33.3	48	96	14.318
110	400	100	100	33.3	48	96	14.318
111	Reserve	100	100	33.3	48	96	14.318

PIN DESCRIPTION

Pin Number	Name	Type	Description
1	PCI0	OUT	PCI clock
2	PCI1	OUT	PCI clock
3	VDD_PCI	PWR	3.3V
4	VSS_PCI	GND	GND
5	PCI2	OUT	PCI clock
6	PCI3	OUT	PCI clock
7	PCI4	OUT	PCI clock
8	PCI5	OUT	PCI clock
9	VSS_PCI	GND	GND
10	VDD_PCI	PWR	3.3V
11	TEST_SEL/PCIF0	I/O	Test Select (sampled at VTT_PWRGD# assertion), see TEST_SEL table. PCI clock afterward, free running.
12	ITP_EN/PCIF1	OUT	Pin38, 39, CPU_ITP/SRC6 select (sampled on VTT_PWRGD# assertion), HIGH = CPU_2PCI clock. PCI clock afterward, running.
13	VDD48	PWR	3.3V
14	USB48 /FS_B	I/O	48MHz clock/ FS_B input
15	VSS48	GND	GND
16	DOT96T	OUT	96MHz 0.7V current mode differential clock output
17	DOT96C	OUT	96MHz 0.7V current mode differential clock output
18	VTT_PWRGD#/PD	I/O	3.3V LVTTL input is a level-sensitive strobe used to latch the FS_A, FS_B, FS_C, TEST_SEL and ITP_EN inputs, VTT_PWRGD# is low assertion/ After VTT_PWRGD# assertion, becomes a real-time input for asserting power down (active HIGH).
19	SRCT0	OUT	Differential Serial reference clock
20	SRCC0	OUT	Differential Serial reference clock
21	SRCT1	OUT	Differential Serial reference clock
22	SRCC1	OUT	Differential Serial reference clock
23	VDD_SRC	PWR	3.3V
24	VSS_SRC	GND	GND
25	SRCT2	OUT	Differential Serial reference clock
26	SRCC2	OUT	Differential Serial reference clock
27	SRCT_SATA	OUT	SATA clock
28	SRCC_SATA	OUT	SATA clock
29	VDD_SRC	PWR	3.3V
30	SRCC3	OUT	Differential Serial reference clock
31	SRCT3	OUT	Differential Serial reference clock
32	SRCC4	OUT	Differential Serial reference clock
33	SRCT4	OUT	Differential Serial reference clock
34	VSS_SRC	GND	GND
35	SRCC5	OUT	Differential Serial reference clock
36	SRCT5	OUT	Differential Serial reference clock
37	VDD_SRC	PWR	3.3V
38	CPUC2_ITP/ SRCC6	OUT	Selectable CPU or SRC differential clock output. ITP_EN=0 @ VTT_PWRGD# assertion = SRCC6.
39	CPUT2_ITP/ SRCT6	OUT	Selectable CPU or SRC differential clock output. ITP_EN=0 @ VTT_PWRGD# assertion = SRCT6.
40	VDD_A	PWR	3.3V
41	VSS_A	GND	GND
42	IREF	OUT	Reference current for differential output buffer

PIN DESCRIPTION (CONT.)

Pin Number	Name	Type	Description
43	CPUC1	OUT	Host 0.7V current mode differential clock output
44	CPUT1	OUT	Host 0.7V current mode differential clock output
45	V_{DD}_CPU	PWR	3.3V
46	CPUC0	OUT	Host 0.7V current mode differential clock output
47	CPUT0	OUT	Host 0.7V current mode differential clock output
48	V_{SS}_CPU	GND	GND
49	SCL	IN	SM bus clock
50	SDA	I/O	SM bus data
51	XTAL_OUT	OUT	Xtal output
52	XTAL_IN	IN	Xtal input
53	V_{SS}_REF	GND	GND
54	REF1/ FSA	I/O	14.318 MHz reference clock output. CPU frequency selection at V_{TT}_P_{WRGD}# assertion.
55	REF0/ FSC	I/O	14.318 MHz reference clock output. CPU frequency selection at V_{TT}_P_{WRGD}# assertion.
56	V_{DD}_REF	PWR	3.3V

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N, (0 is not valid
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2H
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	D3H
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes), power on is 8
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

CONTROL REGISTERS

N PROGRAMMING PROCEDURE

- Use Index byte write.
- For N programming, the user only needs to access Byte17, Byte 25, and Byte8.

1. Write Byte17 for CPU PLL N, CPU f = N* Resolution, see resolution table below Byte17.
2. Write Byte25 for SRC PLL N, SRC f = N*0.666667, PCI = SRC f /3, SATA f = SRC f.
3. Enable N Programming bit, Byte8 bit1. Once this bit is enabled, any N value will be changed on the fly.

- Center spread only works when the N Programming bit is enabled. Down spread is OK even N Programming bit is disabled
- It is OK to change N value to any value on the bench test board. In the system, IDT recommends the stepping change. It is unknown how much the system can sustain for each stepping change; the estimate is about 5. If the N changes too much in one step, the system will likely hang.
- Note that SATA is with SRC PLL. This SATA Hard Drive might not operate during SRC N programming.

Most of the Bytes, from Byte8-Byte31, are used to adjust output waveforms and SSC modulation profiles. The power on setting will be changed according to each power on frequency selection. To avoid mistakes, don't write on those byte (be careful about Block Write). It is suggested to use the Index Byte write to access bytes.

SSC MAGNITUDE CONTROL, SMC

SMC[2:0]	
000	-0.25
001	-0.5
010	-0.75
011	-1
100	±0.125
101	±0.25
110	±0.375
111	±0.5

FREQUENCY SELECTION TABLE

FS_C, B, A	CPU
101	100
001	133
011	166
010	200
000	266
100	333
110	400
111	RESERVE

RESOLUTION

CPU (MHz)	Resolution	N =
100	0.666667	150
133	0.666667	200
166	1.333333	125
200	1.333333	150
266	1.333333	200
333	2.666667	125
400	2.666667	150

BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	CPUT2, CPUC2/ SRCT6, SRCC6	Output enable	Tristate	Enable	RW	1
6	SRCT5, SRCC5	Output enable	Tristate	Enable	RW	1
5	SRCT4, SRCC4	Output enable	Tristate	Enable	RW	1
4	SRCT3, SRCC3	Output enable	Tristate	Enable	RW	1
3	SATAT, SATAC	Output enable	Tristate	Enable	RW	1
2	SRCT2, SRCC2	Output enable	Tristate	Enable	RW	1
1	SRCT1, SRCC1	Output enable	Tristate	Enable	RW	1
0	SRCT0, SRCC0	Output enable	Tristate	Enable	RW	1

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	Reserved				RW	1
6	DOT96T, DOT96C	Output enable	Tristate	Enable	RW	1
5	USB48	Output enable	Tristate	Enable	RW	1
4	REF0	Output enable	Tristate	Enable	RW	1
3	REF1	Output enable	Tristate	Enable	RW	1
2	CPUT1, CPUC1	Output enable	Tristate	Enable	RW	1
1	CPUT0, CPUC0	Output enable	Tristate	Enable	RW	1
0	Spread Spectrum	Spread Spectrum Enable	Off	On	RW	0

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	PCI5	Output enable	Tristate	Enable	RW	1
6	PCI4	Output enable	Tristate	Enable	RW	1
5	PCI3	Output enable	Tristate	Enable	RW	1
4	PCI2	Output enable	Tristate	Enable	RW	1
3	PCI1	Output enable	Tristate	Enable	RW	1
2	PCI0	Output enable	Tristate	Enable	RW	1
1	PCIF1	Output enable	Tristate	Enable	RW	1
0	PCIF0	Output enable	Tristate	Enable	RW	1

BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	CPUT2, CPUC2/ SRCT6, SRCC6	Free running, not affected by PCI/SRC_Stop bit (Byte6, bit3)	Free-Running	Stoppable	RW	0
6	SRCT5, SRCC5		Free-Running	Stoppable	RW	0
5	SRCT4, SRCC4		Free-Running	Stoppable	RW	0
4	SRCT3, SRCC3		Free-Running	Stoppable	RW	0
3	SATAT, SATAC		Free-Running	Stoppable	RW	0
2	SRCT2, SRCC2		Free-Running	Stoppable	RW	0
1	SRCT1, SRCC1		Free-Running	Stoppable	RW	0
0	SRCT0, SRCC0		Free-Running	Stoppable	RW	0

BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved					1
6	DOT96	DOT96 power down drive mode	Driven in power down	Tristate	RW	0
5	PCIF1	Free running, not affected by	Free-Running	Stoppable	RW	0
4	PCIF0	PCI/SRC_Stop bit (Byte6, bit3)	Free-Running	Stoppable	RW	0
3	Reserved					1
2	Reserved					1
1	Reserved					1
0	Reserved					1

BYTE 5

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Stopped SRC	Drive Mode in PCI_Stop	Driven	Tristate	RW	0
6	Reserved					0
5	Reserved					0
4	Reserved					0
3	SRC	SRC PWRDWN drive mode	Driven in power down	Tristate in power down	RW	0
2	CPU_ITP	CPUT2 PWRDWN drive mode	Driven in power down	Tristate in power down	RW	0
1	CPU1	CPUT1 PWRDWN drive mode	Driven in power down	Tristate in power down	RW	0
0	CPU0	CPUT0 PWRDWN drive mode	Driven in power down	Tristate in power down	RW	0

BYTE 6

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved					0
6	Test Select	Test Select	normal	All CLK outputs Hi-Z		0
5	REF1	Strength Select	1x	2x		1
4	REF0	Strength Select	1x	2x		1
3	PCI/SRC_STOP	Stop all stoppable PCI/SRCT clocks	stop	running		1
2		FS_C latch read back			R	
1		FS_B latch read back			R	
0		FS_A latch read back			R	

BYTE 7

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7		Revision ID				0
6		Revision ID				0
5		Revision ID				0
4		Revision ID				0
3		Vendor ID				0
2		Vendor ID				1
1		Vendor ID				0
0		Vendor ID				1

BYTE 8

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	SRC SSC enable	Only valid when Byte1 bit0 is 1	disable	enable	RW	1
6		CPU PLL power down	normal	Power down	RW	0
5		SRC PLL power down	normal	Power down	RW	0
4		USB PLL power down	normal	Power down	RW	0
3	USB48	USB 48 Strength control	1x	2x	RW	0
2	Reserve				RW	0
1		N Programming enable	Disable	enable	RW	0
0	One cycle read		disable	enable	RW	0

BYTE 9

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7		Must be 0	Must be 0		RW	0 (Must be 0)
6	CPU SMC2	see SMC table CPU PLL SSC control			RW	0
5	CPU SMC1				RW	0
4	CPU SMC0				RW	1
3	Reserve				RW	0
2	SRC SMC2	see SMC table SRC/PCI SSC control			RW	0
1	SRC SMC1				RW	0
0	SRC SMC0				RW	1

BYTES 10-16: OUTPUT WAVEFORM ADJUSTMENT. DON'T WRITE OVER.

BYTE 17

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	CPU_N7, MSB				RW	
6	CPU_N6				RW	
5	CPU_N5				RW	
4	CPU_N4				RW	
3	CPU_N3				RW	
2	CPU_N2				RW	
1	CPU_N1	see Resolution table			RW	
0	CPU_N0, LSB	CPU CLK = N* Resolution			RW	

BYTES 18-24: OUTPUT WAVEFORM ADJUSTMENT. DON'T WRITE OVER.

BYTE 25

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	SRC_N7, MSB				RW	
6	SRC_N6				RW	
5	SRC_N5				RW	
4	SRC_N4				RW	
3	SRC_N3				RW	
2	SRC_N2	100MHz N= 150			RW	
1	SRC_N1	Resolution = 0.666667			RW	
0	SRC_N0, LSB	SRC f = N*SRC Resolution			RW	

BYTES 26-31: OUTPUT WAVEFORM ADJUSTMENT. DON'T WRITE OVER.

ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
V_{IH_FS}	LOW Voltage, HIGH Threshold	For FSA.B.C test_mode	0.7	—	V_{DD} + 0.3	V
V_{IL_FS}	LOW Voltage, LOW Threshold	For FSA.B.C test_mode	V_{SS} - 0.3	—	0.35	V
I_{IL}	Input LeakageCurrent	0< V_{IN} < V_{DD}, no internal pull-up or pull-down	–5	—	+5	mA
$I_{DD3.3OP}$	Operating Supply Current	Full active, C_L = full load	—	—	400	mA
$I_{DD3.3PD}$	Powerdown Current	All differential pairs driven	—	—	70	mA
		All differential pairs tri-stated	—	—	12	
F_I	Input Frequency(1)	V_{DD} = 3.3V	—	14.31818	—	MHz
L_{PIN}	Pin Inductance(2)		—	—	7	nH
C_{IN}	Input Capacitance(2)	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	
C_{INX}		X1 and X2 pins	—	—	5	
T_{STAB}	Clock Stabilization(2,3)	From V_{DD} power-up or de-assertion of PD# to first clock	—	—	1.8	ms
	Modulation Frequency(2)	Triangular modulation	30	—	33	KHz
	T_{DRIVE_SRC}(2)	SRC output enable after PCI_Stop# de-assertion	—	—	15	ns
	$T_{DRIVE\_PD\#}$(2)	CPU output enable after PD# de-assertion	—	—	300	us
	$T_{FALL\_PD\#}$(2)	Fall time of PD#	—	—	5	ns
	$T_{RISE\_PD\#}$(3)	Rise time of PD#	—	—	5	ns
	$T_{DRIVE\_CPU\_Stop\#}$(2)	CPU output enable after CPU_Stop# de-assertion	—	—	10	us
	$T_{FALL\_CPU\_Stop\#}$(2)	Fall time of PD#	—	—	5	ns
	$T_{RISE\_CPU\_Stop\#}$(3)	Rise time of PD#	—	—	5	ns

NOTES:
1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_O	Current Source Output Impedance(2)	$V_O = V_X$	3000	—	—	Ω
V_{OH3}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL3}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.4	V
V_{HIGH}	Voltage HIGH(2)	Statistical measurement on single-ended signal using	660	—	850	mV
V_{LOW}	Voltage LOW(2)	oscilloscope math function	–150	—	150	
V_{OVS}	Max Voltage(2)	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{UDS}	Min Voltage(2)		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)(2)		250	—	550	mV
d - V_{CROSS}	Crossing Voltage (var)(2)	Variation of crossing over all edges	—	—	140	mV
ppm	Long Accuracy(2,3)	See T_{PERIOD} Min. - Max. values	–300	—	300	ppm
T_{PERIOD}	Average Period(3)	400MHz nominal/spread	2.4993	—	2.5008	ns
		333.33MHz nominal/spread	2.9991	—	3.0009	
		266.66MHz nominal/spread	3.7489	—	3.7511	
		200MHz nominal/spread	4.9985	—	5.0015	
		166.66MHz nominal/spread	5.9982	—	6.0018	
		133.33MHz nominal/spread	7.4978	—	7.5023	
		100MHz nominal/spread	9.997	—	10.003	
		96MHz nominal	10.4135	—	10.4198	
T_{ABSMIN}	Absolute Min Period(2,3)	400MHz nominal/spread	2.4143	—	—	ns
		333.33MHz nominal/spread	2.9141	—	—	
		266.66MHz nominal/spread	3.6639	—	—	
		200MHz nominal/spread	4.9135	—	—	
		166.66MHz nominal/spread	5.9132	—	—	
		133.33MHz nominal/spread	7.4128	—	—	
		100MHz nominal/spread	9.912	—	—	
		96MHz nominal	10.1635	—	—	
t_R	Rise Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation(2)		—	—	125	ps
d-t_F	Fall Time Variation(2)		—	—	125	ps
d_{T3}	Duty Cycle(2)	Measurement from differential waveform	45	—	55	%
t_{SK3}	Skew(2)	V_T = 50%	—	—	100	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(2)	Measurement from differential waveform	—	—	85	ps

NOTES:
1. SRC clock outputs run only at 100MHz or 200MHz. Specs for 133.33 and 166.66 do not apply to SRC clock pair.
2. This parameter is guaranteed by design, but not 100% production tested.
3. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
T_{PERIOD}	Clock Period(2)	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	0.5	—	2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	0.5	—	2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	500	ps
$t_{JCYC-CYC}$	Jitter(1)	V_T = 1.5V	—	—	250	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
T_{PERIOD}	Clock Period(2)	48MHz output nominal	20.8257	—	20.834	ns
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-29	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-23	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	29	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	27	
	Edge Rate(1)	Rising edge rate	1	—	2	V/ns
	Edge Rate(1)	Falling edge rate	1	—	2	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	1	—	2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	1	—	2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1)	See Tperiod Min. - Max. values	—	—	300	ppm
T_{PERIOD}	Clock Period	14.318MHz output nominal	69.827	—	69.855	ns
V_{OH}	Output HIGH Voltage(1)	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage(1)	I_{OL} = 1mA	—	—	0.4	V
I_{OH}	Output HIGH Current(1)	V_{OH} at Min. = 1V, V_{OH} at Max. = 3.135V	-33	—	-33	mA
I_{OL}	Output LOW Current(1)	V_{OL} at Min. = 1.95V, V_{OL} at Max. = 0.4V	30	—	38	mA
t_{R1}	Rise Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	1	—	2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.4V, V_{OH} = 2.4V	1	—	2	ns
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	500	ps
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter(1)	V_T = 1.5V	—	—	1000	ps

NOTE:
1. This parameter is guaranteed by design, but not 100% production tested.

PCI STOP FUNCTIONALITY

If PCIF (2:0) and SRC clocks are set to be free-running through SMBus programming, they will ignore the PCI_STOP register bit.

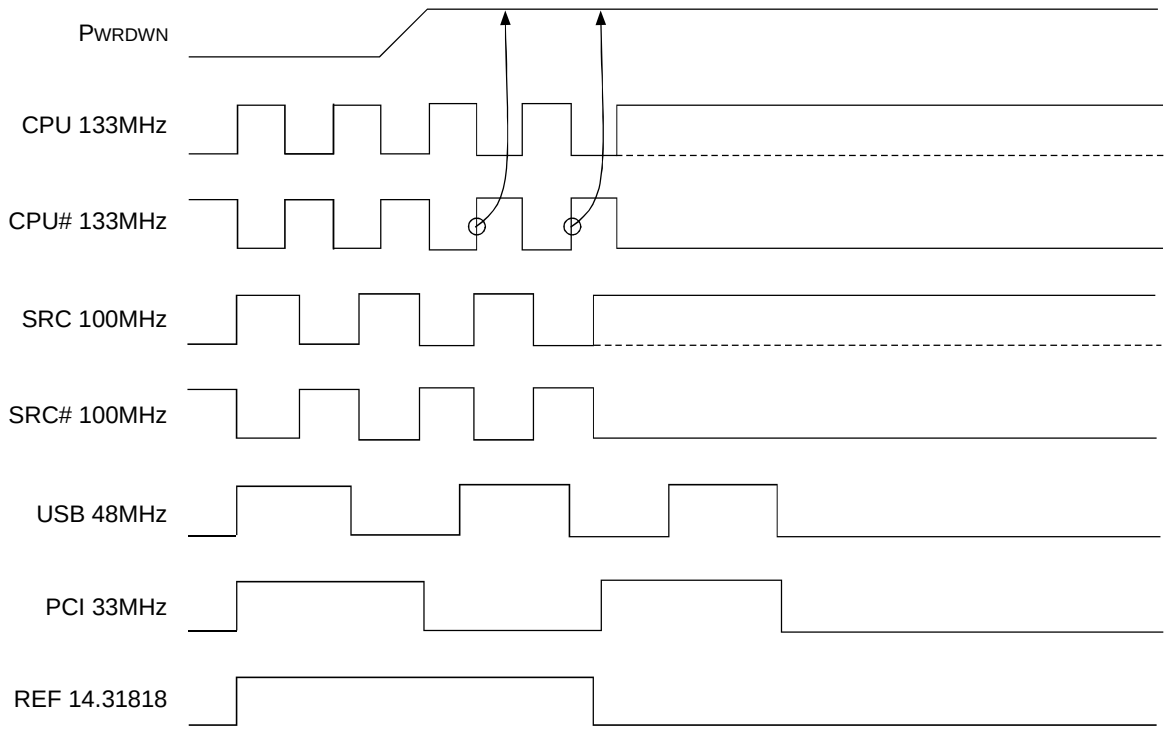
PCI_STOP (Byte 6 bit 3)	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
0	Normal	Normal	I_{REF} * 6 or float	Low	Low	48MHz	Normal	Normal	14.318MHz

PD, POWER DOWN

PD is an asynchronous active high input used to shut off all clocks cleanly prior to clock power. When PD is asserted high all clocks will be driven low before turning off the VCO. In PD de-assertion all clocks will start without glitches.

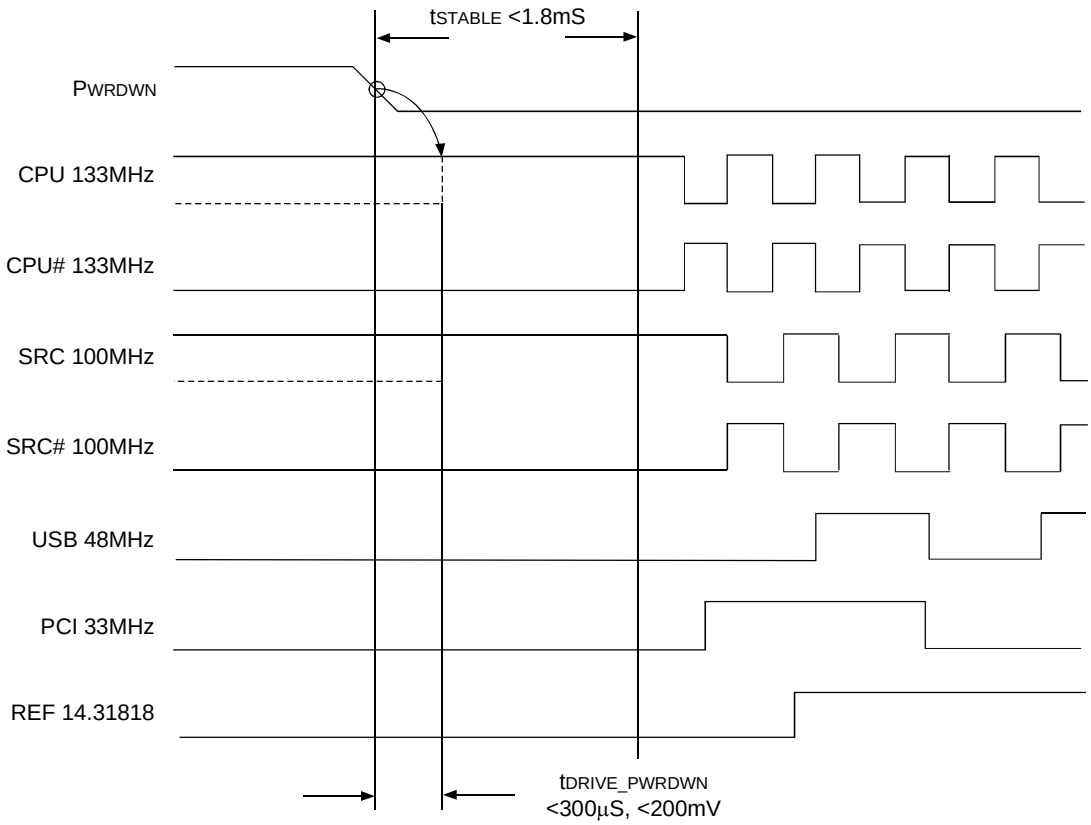
PWRDWN	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
0	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
1	IREF * 2 or float	Float	IREF * 2 or float	Float	Low	Low	IREF * 2 or float	Float	Low

PD ASSERTION

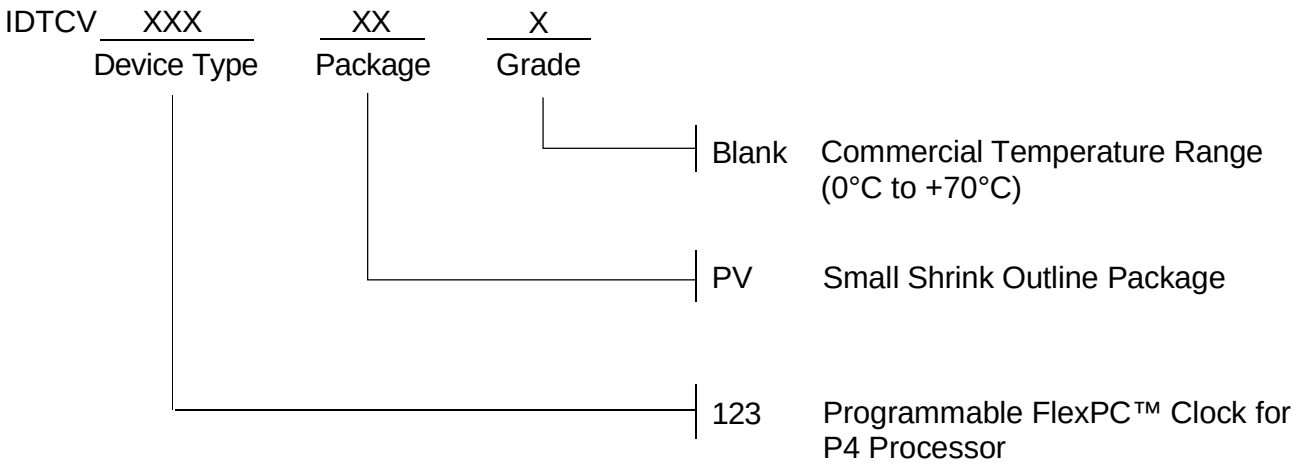


PD DE-ASSERTION

The time from the de-assertion of PD or until power supply ramps to get stable clocks will be less than 1.8ms. If the drive mode control bit for PD tristate is programmed to '1' the stopped differential pair must first be driven high to a minimum of 200mV in less than 300µs of PD deassertion.



ORDERING INFORMATION



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