

# $\mu$ PD23C512E

**65,536 x 8-Bit  
Mask-Programmable  
CMOS ROM**

## **Data Sheet**

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Electronics Inc., at its own discretion, may withdraw the device prior to production.

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## Preliminary Information

### Description

The uPD23C512E is a 524,288-bit Read-only Memory. It is static in operation, organized for direct-addressing mode with 65,536 words by 8 bits, and for page addressing mode with 4 pages, each 16,384 words by 8 bits.

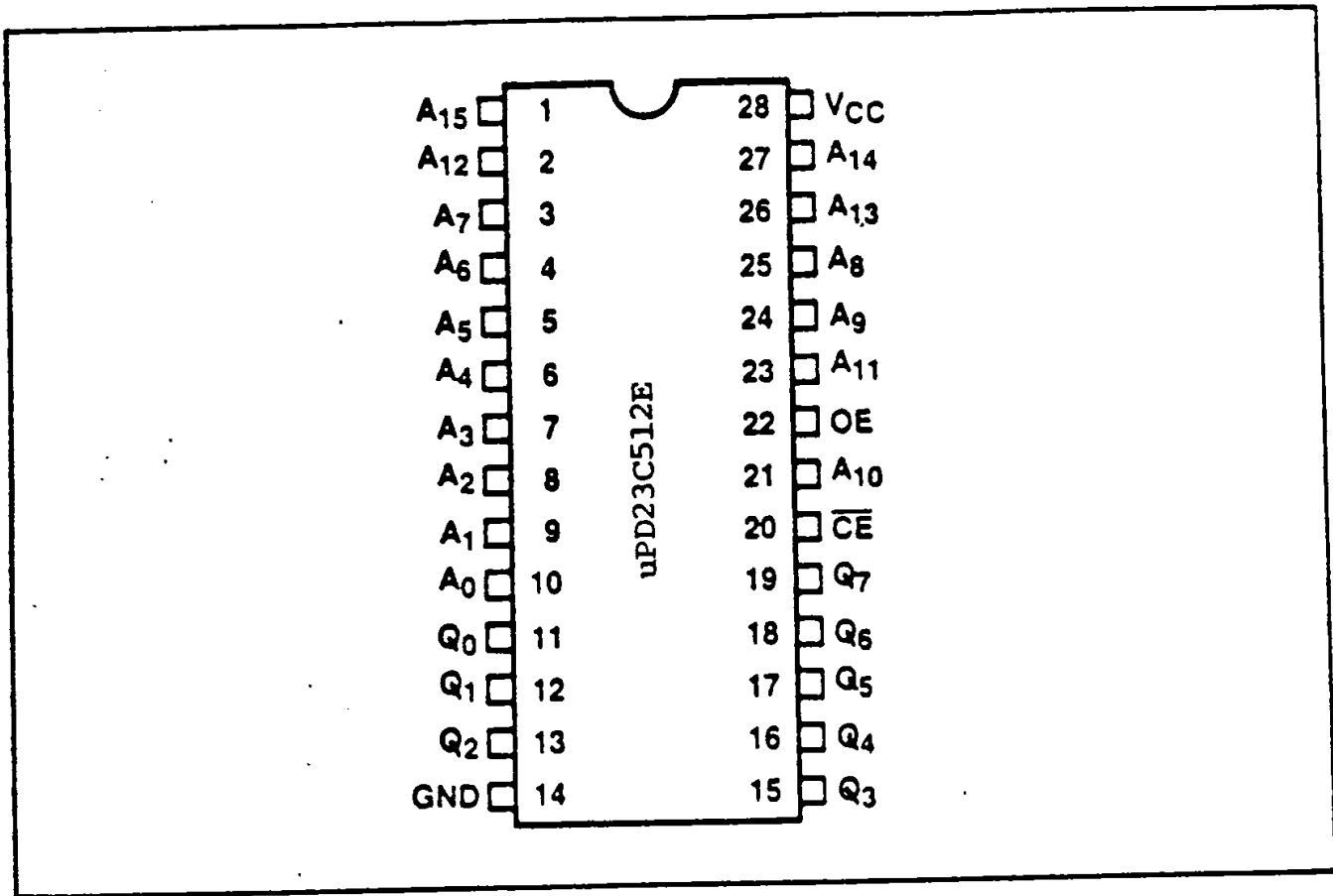
This device has three-state outputs. All inputs and outputs are fully TTL-compatible. The output enable pin is mask-programmable and can be specified by selecting 1, 0, or don't-care data.

The uPD23C512E is packaged in a 28-pin plastic DIP.

### Features

- 65,536-word x 8-bit organization (direct mode)
- 4 pages of 16,384-word x 8-bit organization (page mode)
- Mask-programmable
- I/O TTL-compatible
- Three-state output
- Single +5 V power supply
- CMOS process technology
- Low power dissipation
- 28-pin plastic DIP

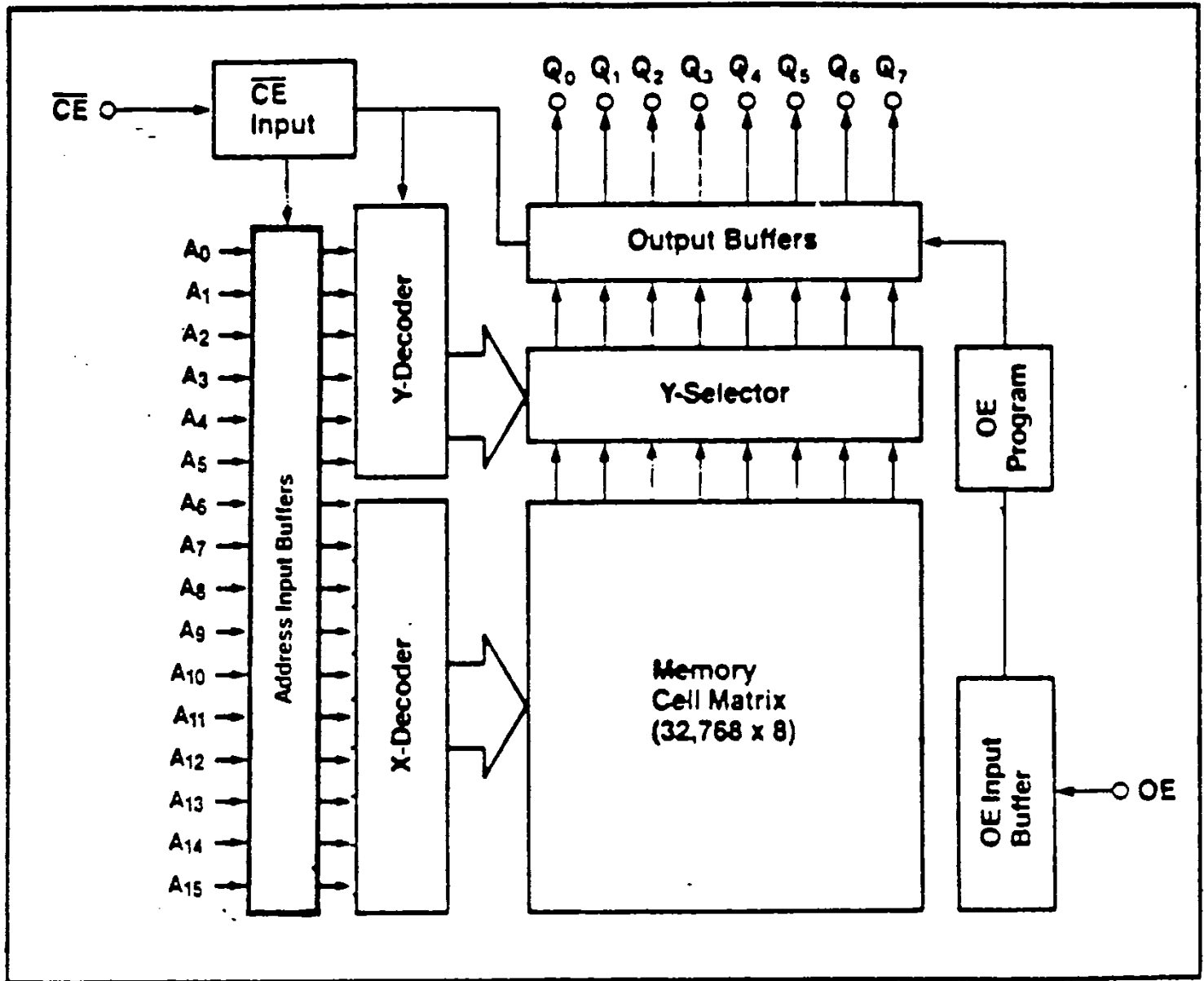
# Pin Configuration



## Pin Identification

No.	Symbol	Function
1-10, 21, 23-27	A <sub>0</sub> -A <sub>15</sub>	Address inputs
11-13, 15-19	Q <sub>0</sub> -Q <sub>7</sub>	Data outputs
14	GND	Ground
20	$\overline{\text{CE}}$	Chip enable
22	OE	Output enable
28	VCC	Power supply

# Block Diagram



## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$

Supply voltage, $V_{CC}$	-0.3 to +7 V
Input voltage, $V_I$	-0.3 to $V_{CC} + 0.3$ V
Output voltage, $V_O$	-0.3 to $V_{CC} + 0.3$ V
Operating temperature, $T_{OPT}$	$-10^\circ$ to $+70^\circ\text{C}$
Storage temperature, $T_{STG}$	$-65^\circ$ to $+150^\circ\text{C}$

## Capacitance

TA = 25°C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	CI			15	pF	f=1 MHz
Output capacitance	CO			15	pF	f=1 MHz

## DC Characteristics

TA = -10° to +70°C; VCC = +5.0 V ± 10%

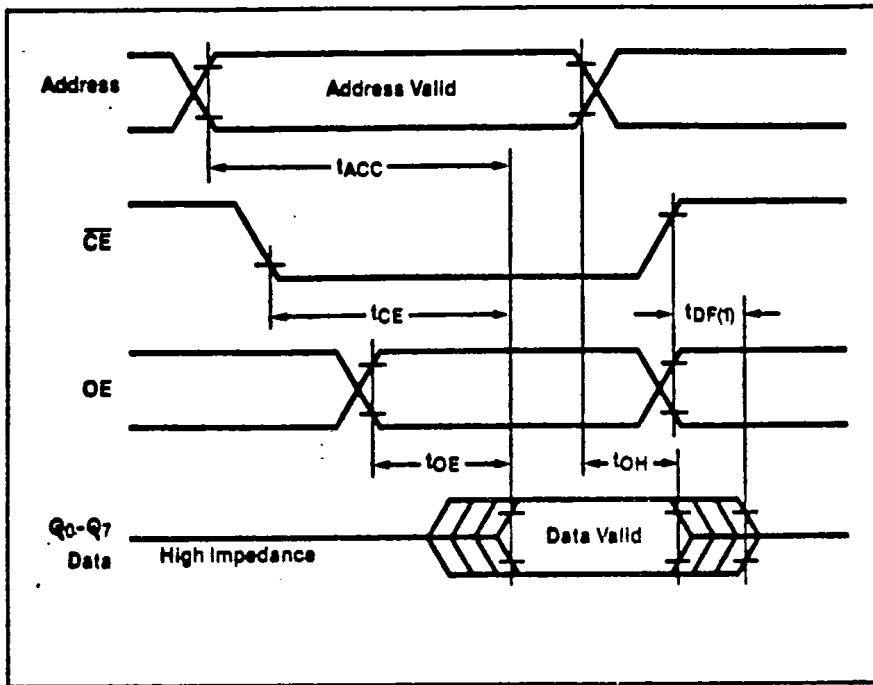
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input high voltage	VIH	2.2		VCC+0.3	V	
Input low voltage	VIL	-0.3		0.8	V	
Output high voltage	VOH	2.4			V	IOH = -400 uA
Output low voltage	VOL			0.4	V	IOL = +2.5 mA
Input leakage current high	ILIH			10	uA	VI = VCC
Input leakage current low	ILIL			-10	uA	VI = 0 V
Output leakage current high	ILOH			10	uA	VO = VCC chip deselected
Output leakage current low	ILOL			-10	uA	VO = 0 V chip deselected
Power supply current	ICC1			35	mA	$\overline{CE}$ = VIL chip selected
Power supply current	ICC2			1.5	mA	$\overline{CE}$ = VIH chip deselected
Power supply current	ICC3			100	uA	$\overline{CE}$ = VCC-0.2 V chip deselected

## AC Characteristics

TA = -10° to +70°C; VCC = +5.0 V ± 10%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Access time	tACC			200	ns	
Chip enable access time	tCE			200	ns	Input voltage tr, tf = 20 ns
Output hold time	tOH	0			ns	Input and output reference levels are 0.8 + 2.0 V
Output disable time	tDF			70	ns	Load = 1 TTL + 100 pF
Output enable access time	tOE			70	ns	

# Timing Waveform Read Operation (Direct/Page Mode)



## PACKAGING INFORMATION

### 28-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 <sup>+ .004</sup> <sub>- .005</sub>
E	33.02	1.300
F	1.2 min	.047 min
G	3.6 ± .30	.142 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.225 max
K	15.24 [TP]	.600 [TP]
L	13.20	.520
M	.25 <sup>+ .10</sup> <sub>- .05</sub>	.010 <sup>+ .004</sup> <sub>- .003</sub>

**Notes:**

[1] Each lead centerline is located within .25 mm (.010 inch) of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

