ADVANCE PRODUCT INFORMATION

December 1986

μPD23C512E

65,536 x 8-Bit Mask-Programmable CMOS ROM

Data Sheet

uPD23C512E
65,536 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Preliminary Information

Description

The uPD23C512E is a 524,288-bit Read-only Memory. It is static in operation, organized for direct-addressing mode with 65,536 words by 8 bits, and for page addressing mode with 4 pages, each 16,384 words by 8 bits.

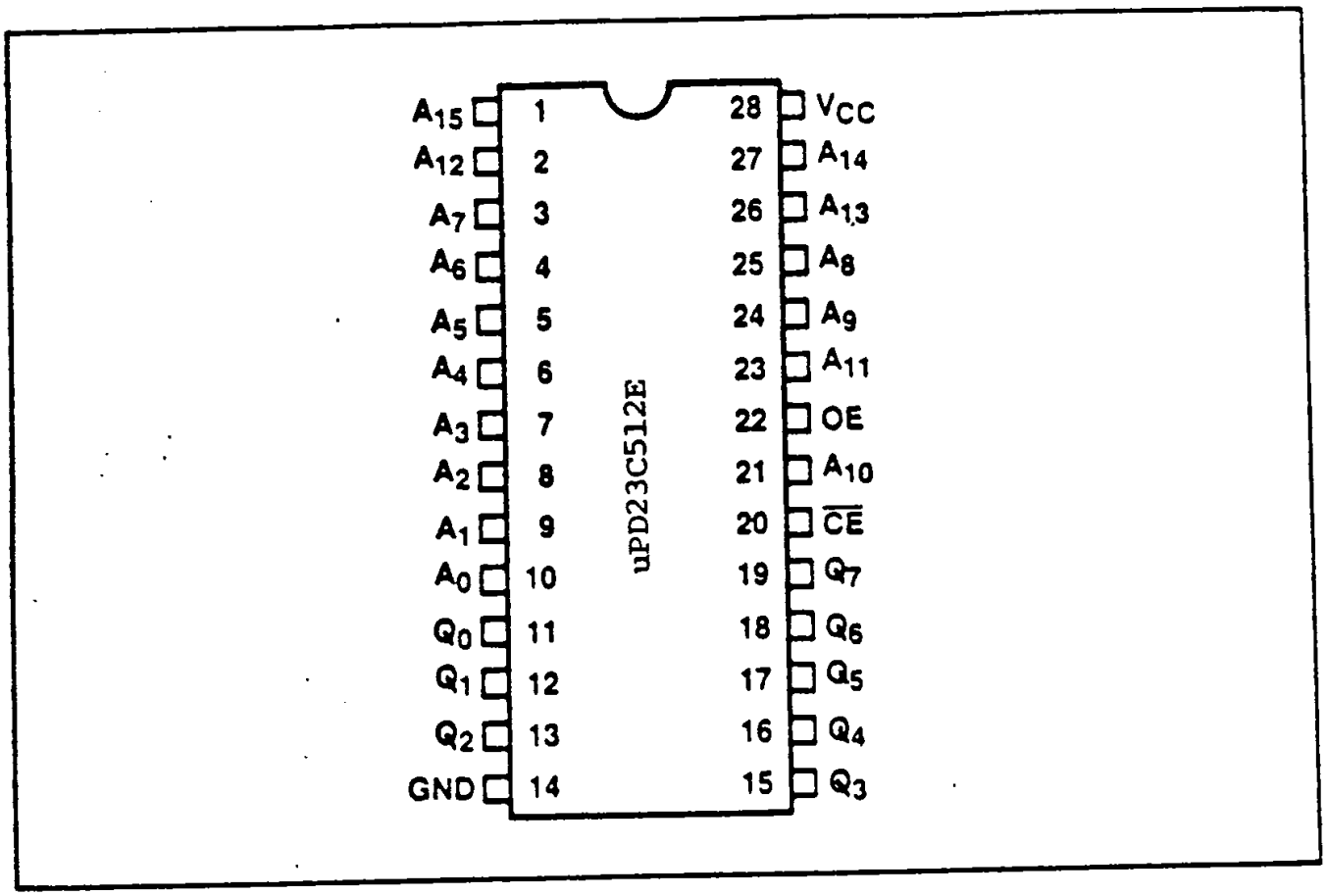
This device has three-state outputs. All inputs and outputs are fully TTL-compatible. The output enable pin is mask-programmable and can be specified by selecting 1, 0, or don't-care data.

The uPD23C512E is packaged in a 28-pin plastic DIP.

Features

- 65,536-word x 8-bit organization (direct mode)
- 4 pages of 16,384-word x 8-bit organization (page mode)
- Mask-programmable
- I/O TTL-compatible
- Three-state output
- Single +5 V power supply
- CMOS process technology
- Low power dissipation
- 28-pin plastic DIP

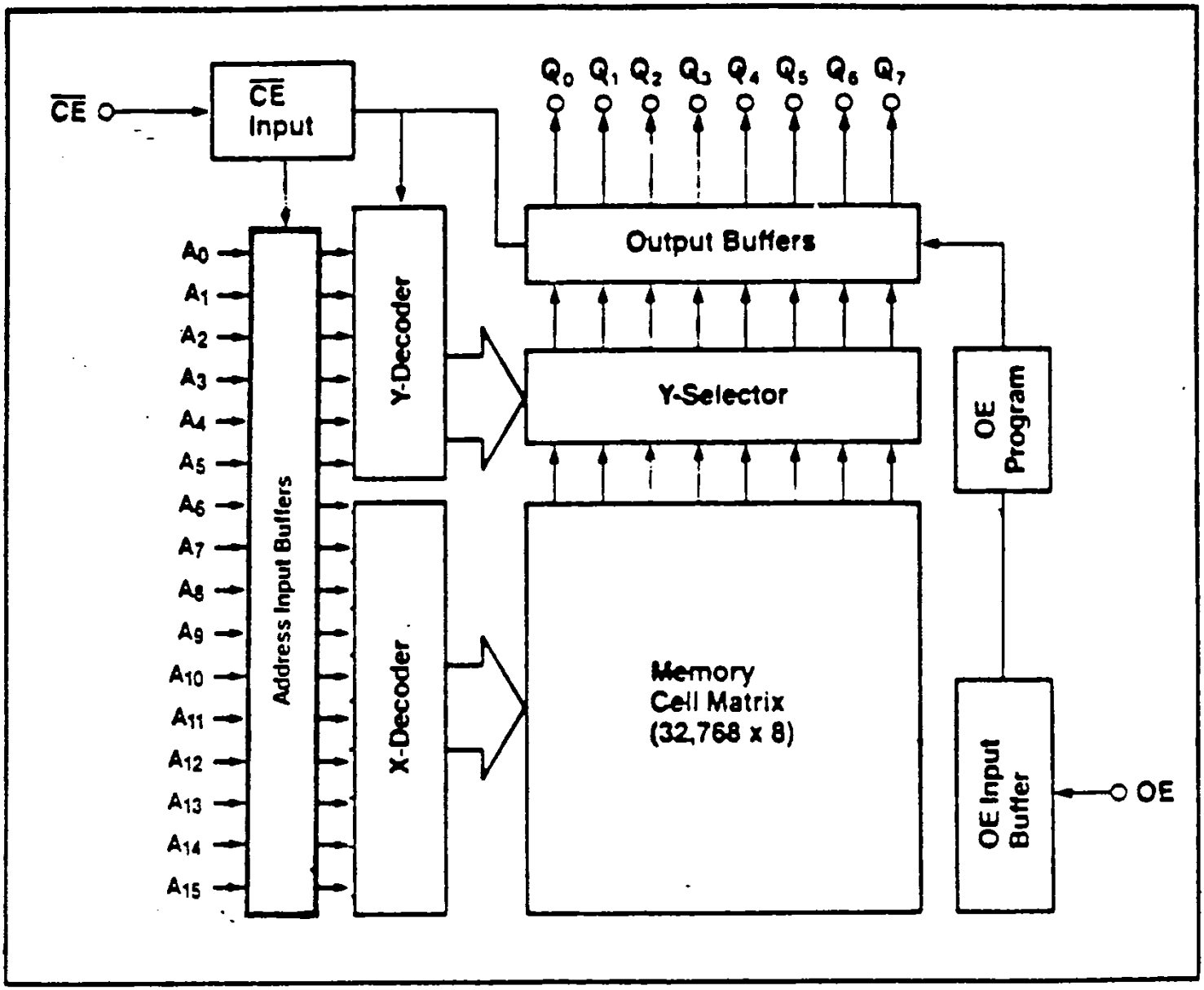
Pin Configuration



Pin Identification

No.	Symbol	Function
1-10,21, 23-27	A0-A15	Address inputs
11-13, 15-19	Q0-Q7	Data outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	OE	Output enable
28	VCC	Power supply

Block Diagram



Absolute Maximum Ratings
TA = 25°C

Supply voltage, VCC	-0.3 to +7 V
Input voltage, VI	-0.3 to VCC+.3 V
Output voltage, VO	-0.3 to VCC+.3 V
Operating temperature, TOPT	-10° to + 70°C
Storage temperature, TSTG	-65° to +150°C

Capacitance

T_A = 25°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	CI			15	pF	f=1 MHz
Output capacitance	CO			15	pF	f=1 MHz

DC Characteristics

T_A = -10° to +70°C; V_{CC} = +5.0 V ± 10%

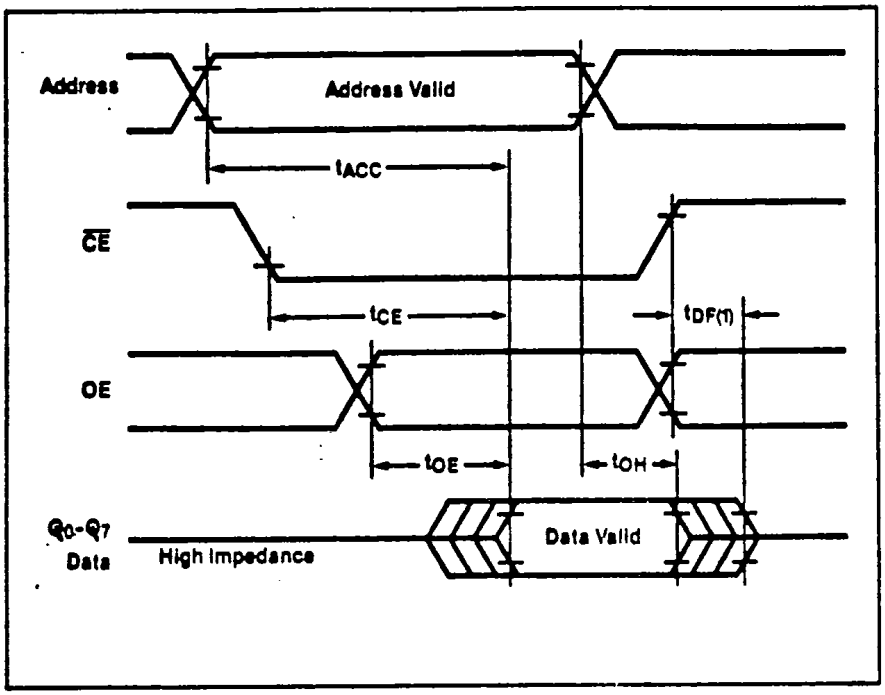
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input high voltage	VIH	2.2		VCC+0.3	V	
Input low voltage	VIL	-0.3		0.8	V	
Output high voltage	VOH	2.4			V	IOH = -400 uA
Output low voltage	VOL			0.4	V	IOL = +2.5 mA
Input leakage current high	ILIH			10	uA	VI = VCC
Input leakage current low	ILIL			-10	uA	VI = 0 V
Output leakage current high	ILOH			10	uA	VO = VCC chip deselected
Output leakage current low	ILOL			-10	uA	VO = 0 V chip deselected
Power supply current	ICC1			35	mA	$\overline{CE}$ = VIL chip selected
Power supply current	ICC2			1.5	mA	$\overline{CE}$ = VIH chip deselected
Power supply current	ICC3			100	uA	$\overline{CE}$ = VCC-0.2 V chip deselected

AC Characteristics

T_A = -10° to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Access time	tACC			200	ns	
Chip enable access time	tCE			200	ns	Input voltage tr, tf = 20 ns
Output hold time	tOH	0			ns	Input and output reference levels
Output disable time	tDF			70	ns	are 0.8 + 2.0 V Load = 1 TTL + 100 pF
Output enable access time	tOE			70	ns	

Timing Waveform Read Operation (Direct/Page Mode)



PACKAGING INFORMATION

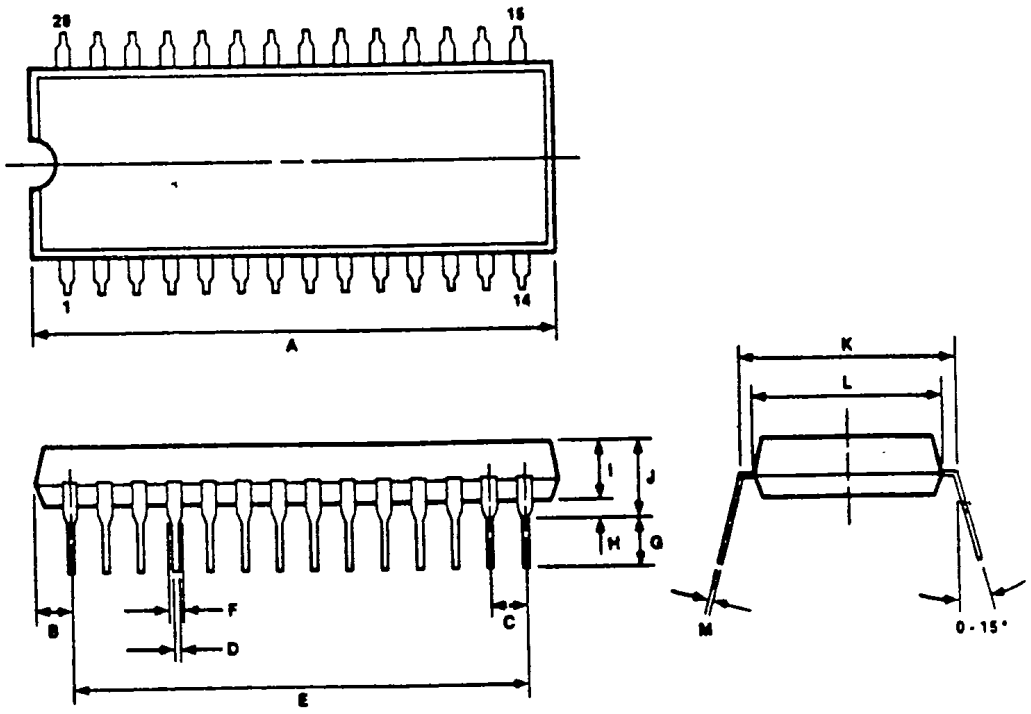
28-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	36.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	33.02	1.300
F	1.2 min	.047 min
G	3.6 ± .30	.142 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.20	.520
M	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



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