CHERRY SEMICONDUCTOR

CS-117/117R

2, 4 or 6-Channel

WINCHESTER READ/WRITE CIRCUIT

DESCRIPTION

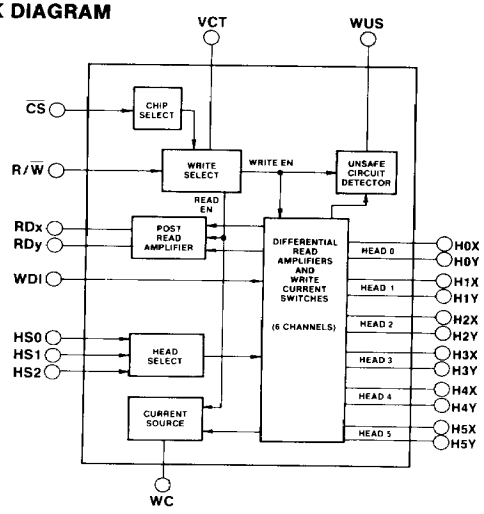
The CS-117 is a monolithic Read/Write IC designed for use in Winchester disk drive magnetic memory systems. The circuit interfaces with up to six heads to provide the necessary R/W functions, as well as control and data protect functions. LSTTL interfaces are used for the Write Data, Head Select, R/$\overline{W}$ Select, Write Unsafe, and Chip Select circuits. Write current is generated internally as a function of an external resistor. Write current transitions occur at each negative transition of the write data input. The low noise read amplifier has a typical voltage gain of 100. Balanced emitter follower outputs are used in the read amplifier. The CS-117 operates on +5V and +12V supplies.

The CS-117R performs the same function as the CS-117 with the addition of internal damping resistors.

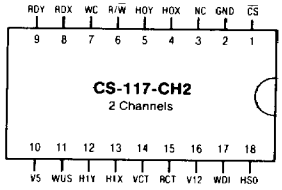
FEATURES:

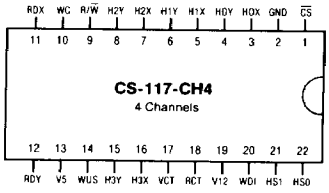
- Controls up to 6 R/W channels
- On-chip write current source, externally set
- Drives center-tapped ferrite heads
- Independent read and write busses
- TTL write data input
- LSTTL control interface
- Emitter follower read amplifier outputs
- 5V & 12V power supplies

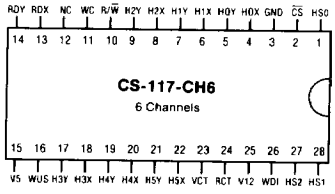
BLOCK DIAGRAM

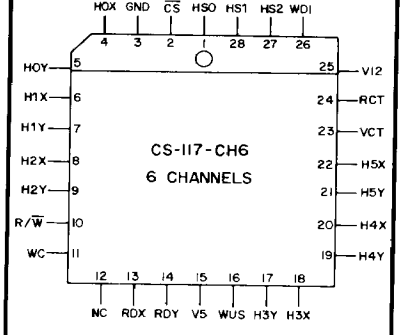


PIN CONNECTIONS









Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
(401) 885-3600 Telefax (401) 885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS: V5=4.5 to 5.5V, V12=10.8 to 13.2V, $25°C \leq T_J \leq 125°C$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply				
+5V Supply Current	Read/Idle Modes	—	25	mA
+5V Supply Current	Write Mode	—	30	mA
+12V Supply Current	Read Mode	—	50	mA
+12V Supply Current	Write Mode	—	30 + IW	mA
+12V Supply Current	Idle Mode	—	25	mA
Power Dissipation	Read Mode, T_J = 125°C	—	600	mW
Power Dissipation	Write Mode, T_J = 125°C IW = 35mA, RCT = 130	—	700	mW
Power Dissipation	Write Mode, T_J = 125°C IW = 35mA, RCT = 0	—	1050	mW
Power Dissipation	Idle Mode, T_J = 125°C	—	400	mW
Logic Signals				
Input Low Voltage (VIL)		-0.3	0.8	V
Input Low Current	VIL = 0.8V	-0.4	—	mA
Input High Voltage (VIH)		2.0	V5 + 0.3	V
Input High Current	VIH = 2.0V	—	100	μA
US Low Level Voltage (VLUS)	ILUS = 8mA (Denotes Safe Condition)	—	0.5	V
US High Level Current (IHUS)	VHUS = 5.0V (Denotes unsafe condition)	—	100	μA
Write Mode Iw=25mA, Lh=10uH, Rd=750Ω, f(Data)=5MHz, CL (RDX, RDY)≤20pF				
Write Current Range		10	35	mA
Write Current Constant "K"		133	147	V
Differential Head Voltage Swing		5.7	—	VpK
Unselected Diff. Head Current		—	2	mApK
Differential Output Capacitance		—	15	pF
Differential Output Resistance		10k	—	Ω
WDI Transition Frequency	WUS=Low	125	—	kHz
Read Mode (Vin is referenced to Vct)				
Differential Voltage Gain	Vin = 1mVpp @ 300kHz Z_L = 1kohm per side	80	120	V/V
Bandwidth (-3dB)	Z_S<5Ω, Vin = 1mVpp	30	—	MHz
Input Noise Voltage	BW = 15MHz, Lh = 0, Rh = 0	—	2.1	nV/√Hz
Differential Input Capacitance	f = 5MHz	—	23	pF
Differential Input Resistance	f = 5MHz	2k	—	Ω
Input Bias Current (per side)		—	45	μA
Dynamic Range	DC input voltage where gain falls by 10% (tested with .5mVpp input @ 300 kHZ)	-2.0	2.0	mV
Common Mode Rejection Ratio	Vcm =Vct +100mV	50	—	dB
Power Supply Rejection Ratio	100mVpp on V5 or V12, f = 5MHz	45	—	dB
Channel Separation	Unselected channels driven with Vin = 100mVpp, f = 5MHz	45	—	dB
Output Offset Voltage		-480	+480	mV
Common Mode Output Voltage		5.0	7.0	V
Single Ended Output Resistance	f = 5MHz	—	30	Ω
Switching Characteristics T_J=25°C, I_w=35 mA, Lh=10vH, Rd=750Ω, f(Data)=5MHz				
Read to Write Transition Time	Delay to 90% of Write Current	—	1.0	μS
Write to Read Transition Time	Delay to 90% of 100mV 10MHz Read Signal Envelope Write Current Delay to 10%	—	1.0	μS
Head Select Switching Delay	Delay to 90% of 100mV 10MHz Read Signal Envelope	—	1.0	μS
Chip Disable Transition Time Read/Write to Idle Idle to Read/Write	Delay to 90% Decay of Write Current Delay to 90% of Write Current or to 90% of 100mV 10MHz read signal envelope	—	1.0	μS
Head Current Transition Time	IW = 35mA, Lh = 0, Rh = 0 10% to 90% points	—	20	nS
Unsafe to Safe Delay After Write Data Begins	IW = 20mA, Lh = 10μH	—	1.0	μS
Safe to Unsafe Delay	IW = 35mA, Lh = 10μH	1.6	8.0	μS
Head Current Switching Delay a) Time b) Asymmetry	35mA, Lh = 0μH, Rh = 0 50% VIL input to 50% output WDI has 50% Duty Cycle and 1nS Rise/Fall time	—	25 2	nS nS

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-117-2DW	18 Lead SO Wide
CS-117-2N	18 Lead PDIP
CS-117-4DW	24 Lead SO Wide
CS-117-4N	24 Lead PDIP
CS-117-6DW	28 Lead SO Wide
CS-117-6FN	28 Lead PLCC
CS-117-6N	28 Lead PDIP

WITH INTERNAL DAMPING RESISTORS

CS-117-2RDW	18 Lead SO Wide
CS-117-2RN	18 Lead PDIP
CS-117-4RDW	24 Lead SO Wide
CS-117-4RN	24 Lead PDIP
CS-117-6RDW	28 Lead SO Wide
CS-117-6RFN	28 Lead PLCC
CS-117-6RN	28 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

REV. 5/86