REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
F	Change to vendor similar part number for vendor CAGE 18324. Changes to table I parameters t_{EA} and C_{OUT}. Add vendor CAGE 18324 to device types 03 and 04 as a source of supply. Add new device design for device 04 for vendor CAGE 07933. Removed table III, figure 5, and programming procedures. Editorial changes throughout.	91-10-30	M. A Frye
G	Changes in accordance with NOR 5962-R010-93	93-02-12	M. A Frye
H	Changes in accordance with NOR 5962-R205-93	93-08-10	M. A Frye
J	Updated boilerplate. Sheet 4, change V_{OH} conditions from I_{OH} = -2.0 mA to -1.6 mA; change C_{IN} max. limit from 10 pF to 15 pF; change C_{OUT} max. limit for devices 01, 02, and 04 from 13 pF to 20 pF; add footnote 3 to t_{DA} test column. Removed logic diagrams. Remove vendors CAGE 50364 and 34335 as suppliers, and removed their associated switching time test circuits.	97-05-29	Raymond Monnin

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV	J	J	J	J	J	J	J	J	J	J	J	J											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12											

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
James E. Jamison

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
82-09-01

REVISION LEVEL
J

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316-5000

MICROCIRCUITS, MEMORY, DIGITAL, SCHOTTKY BIPOLAR 32K PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	82008

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN number shall be as shown in the following example:

82008	01	J	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-PRF-38535 appendix A

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device types	Generic number	Circuit function	Access time
01	See 6.6	4096 words x 8 bits per word PROM, T.S.	95
02	See 6.6	4096 words x 8 bits per word PROM, T.S.	55
03	See 6.6	4096 words x 8 bits per word PROM, T.S.	45
04	See 6.6	4096 words x 8 bits per word PROM, T.S.	70

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	flat package
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line
X	CQCC1-N32	32	rectangular leadless chip carrier
3	CQCC1-N28	28	square leadless chip carrier
Y	CDFP4-F24	24	flat package

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.3 V dc to +7.0 V dc
Input voltage range	5.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835 1/
Output voltage applied	-0.3 V dc to +V_{CC}
Output sink current	100 mA
Maximum power dissipation (P_D) 2/	1.04 W dc
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Normalized fanout (each output)	12 mA
Case operating temperature range (T_C)	-55°C to +125°C

1/ Heat sinking is recommended to reduce the junction temperature.
2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 2. When required in group A or C inspection (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed).

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Device type	Group A sub-groups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = minimum, I_{OH} = -1.6 mA	All	1,2,3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = minimum, I_{OL} = 16 mA	All	1,2,3		0.5	V
Input clamp voltage	V_{IC}	I_{IN} = -18 mA	All	1,2,3		-1.5	V
High impedance (off-state) output high current	I_{OHZ}	V_{CC} = V_{CC} maximum, V_O = 2.4 V	01	1,2,3		100	µA
			02, 03, 04			40	
High impedance (off-state) output low current	I_{OLZ}	V_{CC} = V_{CC} maximum, V_O = 0.4 V	01	1,2,3		-100	µA
		V_{CC} = V_{CC} maximum, V_{CC} = 0.4 V	02, 03, 04			-40	
High level input current	I_{IH}	V_{IH} = V_{CC} maximum	All	1,2,3		40	µA
Low level input current	I_{IL}	V_{IL} = 0.4 V, V_{CC} = V_{CC} maximum	All	1,2,3		-250	µA
Short circuit output current	I_{OS}	V_{OUT} = 0.2 V 1/	All	1,2,3	-15	-100	mA
Supply current	I_{CC}	V_{CC} = V_{CC} maximum, all inputs grounded	All	1,2,3		190	mA
Input capacitance	C_{IN}	V_{CC} = 5 V, f = 1 MHz, V_{IN} = 2.0 V, see 4.3.1c	All	4		15	pF
Output capacitance	C_{OUT}	V_{CC} = 5 V, f = 1 MHz, V_{OUT} = 2.0 V, see 4.3.1c	01,02, 04	4		20	pF
			03			12	
Address access time	t_{AA}	V_{CC} = 4.5 V and 5.5 V, see figure 4	01	9,10,11		95	ns
			02			55	
			03			45	
			04			70	
Chip enable access time	t_{EA}		01,04	9,10,11		45	ns
			02			35	
			03				
Chip disable access time 2/ 3/	t_{DA}		01	9,10,11		45	ns
			02,03, 04			35	

1/ Not more than one output shall be grounded at one time, for a maximum of 1 second.
2/ $C_L \ge 5$ pF.
3/ May not be tested but is guaranteed to the limits specified in table I.

Device types	All		
Case outlines	J, K, Y, L	X	3
Terminal number	Terminal symbol		
1	A_7	NC	NC
2	A_6	NC	A_7
3	A_5	A_7	A_6
4	A_4	A_6	A_5
5	A_3	A_5	A_4
6	A_2	A_4	A_3
7	A_1	A_3	A_2
8	A_0	A_2	A_1
9	O_1	A_1	A_0
10	O_2	A_0	NC
11	O_3	NC	O_1
12	GND	O_1	O_2
13	O_4	O_2	O_3
14	O_5	O_3	GND
15	O_6	NC	NC
16	O_7	GND	O_4
17	O_8	O_4	O_5
18	CE_2	NC	O_6
19	A_{11}	O_5	O_7
20	$\overline{CE}_1$	O_6	O_8
21	A_{10}	O_7	NC
22	A_9	O_8	CE_2
23	A_8	NC	A_{11}
24	V_{CC}	CE_2	$\overline{CE}_1$
25	—	A_{11}	A_{10}
26	—	$\overline{CE}_1$	A_9
27	—	NC	A_8
28	—	A_{10}	V_{CC}
29	—	A_9	—
30	—	A_8	—
31	—	NC	—
32	—	V_{CC}	—

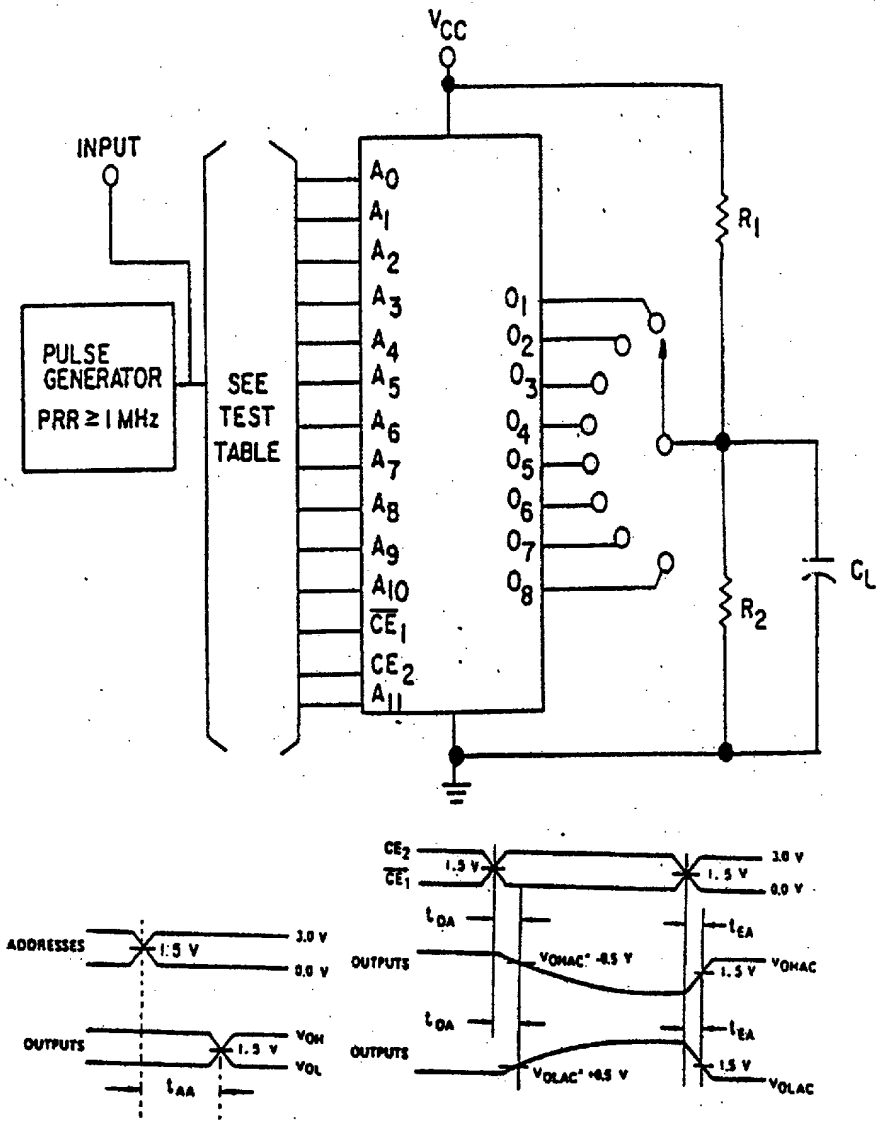
FIGURE 1. Terminal connections

Word number	$\overline{CE}_1$	CE_2	Address												Data							
			A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
NA	L	H	X	X	X	X	X	X	X	X	X	X	X	X	See Note 5							
	H	X	X	X	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC

NOTES:
1. NA = Not applicable.
2. X = Input may be high level, low level or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with enable input at low level.
5. The outputs for an unprogrammed device shall be high for circuits C and F.

FIGURE 2. Truth table (unprogramed).

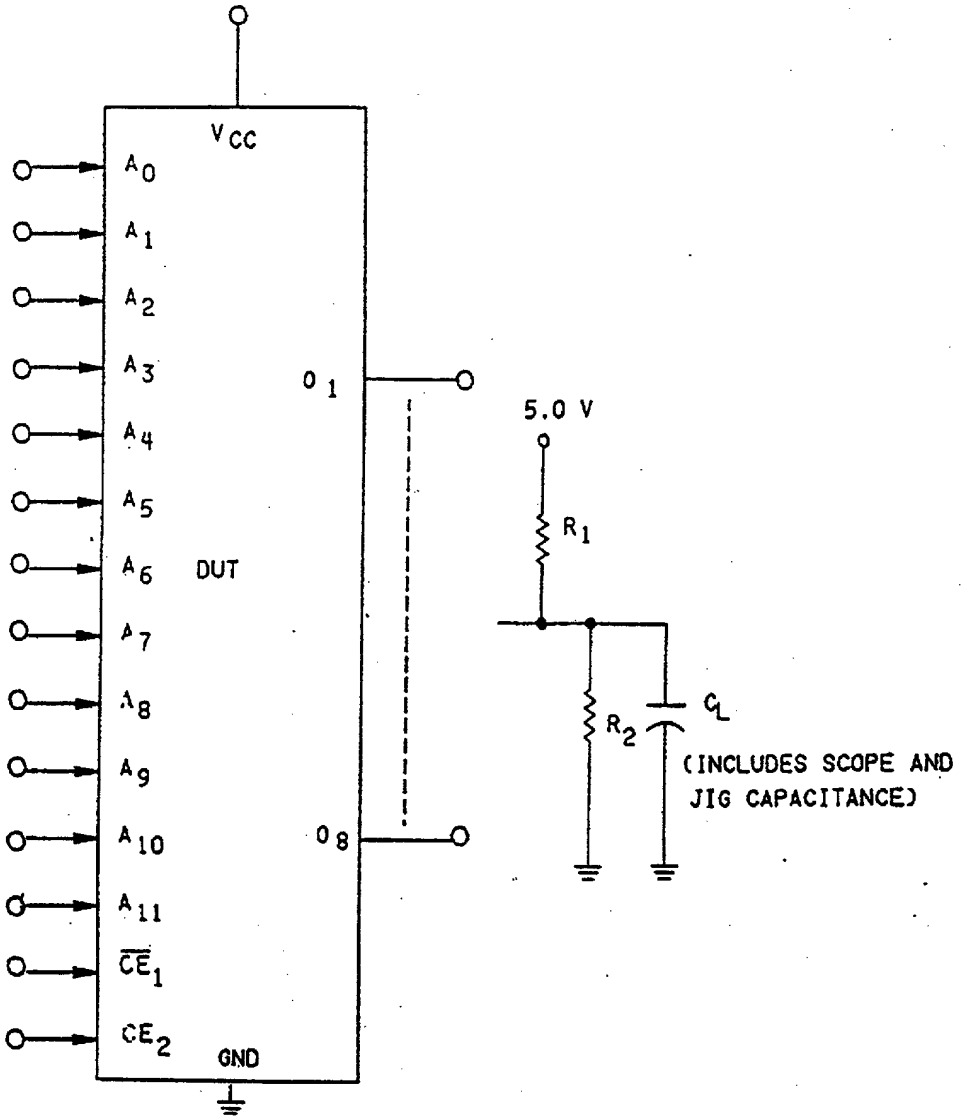
Circuit F



NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration of the resulting read-only memory.
2. C_L = 30 pF minimum, including jig and probe capacitance: R_1 = 300Ω and R_2 = 600Ω.
3. Outputs may be under load simultaneously.
4. V_{OLAC} and V_{OHAC} are the measured output voltage levels while enabled.

FIGURE 3. Switching time test circuits and waveforms.

Circuit C



NOTE: $R_1 = 270\Omega$, $R_2 = 600\Omega$ and $C_L = 50$ pF.

FIGURE 3. Switching time test circuits and waveforms - Continued.

Circuit C

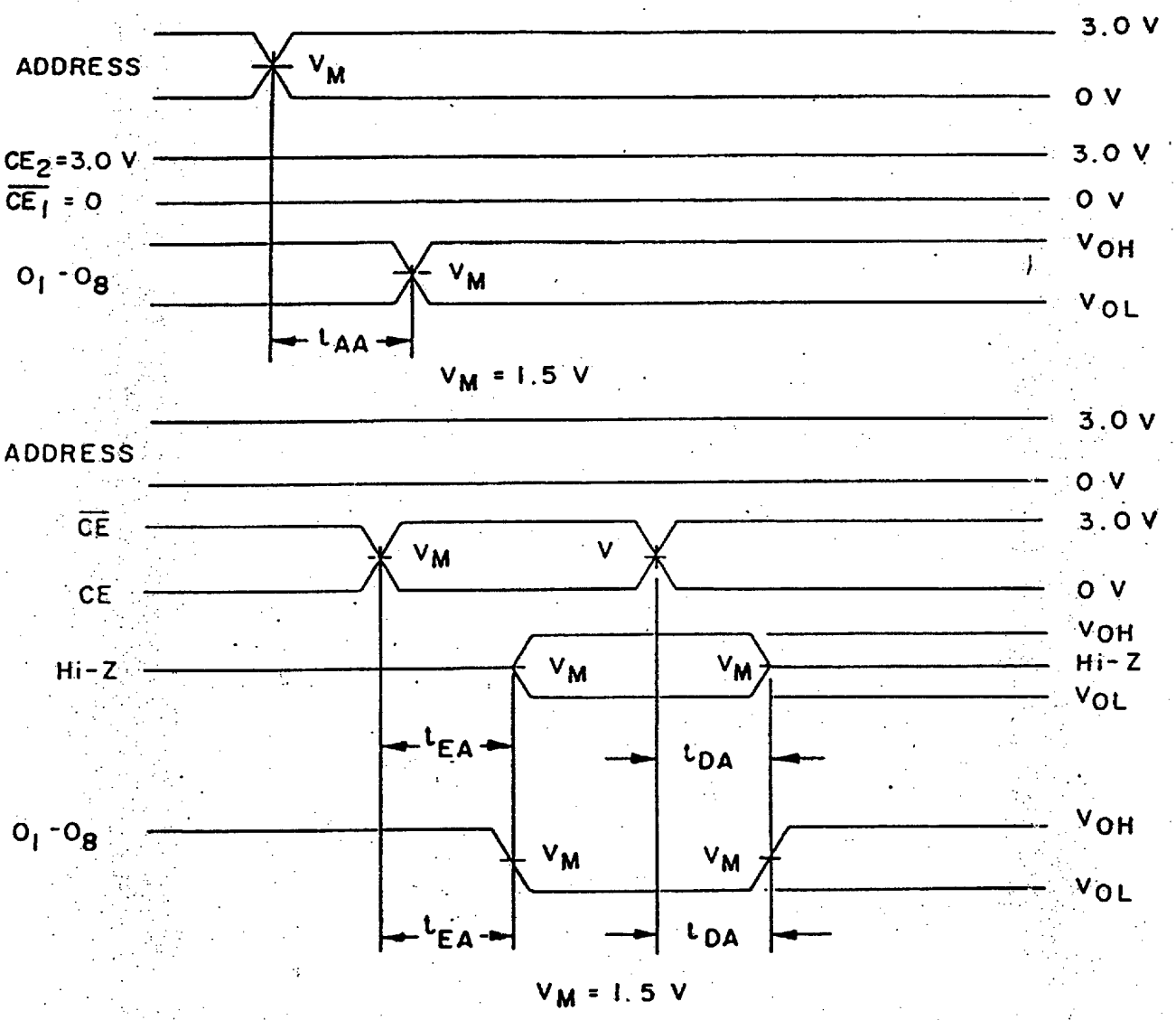


FIGURE 3. Switching time test circuits and waveforms - Continued.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of ROM configurations, two processing options are provided for selection, using an altered item drawing.

3.10.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II herein. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*,8A, 8B
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8A, 8B,9
Group A test requirements (method 5005)	1,2,3,4,7,8A, 8B,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8A,8B,

1/ * PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high speed testers.
3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming. If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. (Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.)

e. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883 conditions.

(1) Test condition A, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Circuit designator. For CAGE code and vendor association, see MIL-HDBK-103. Circuit C is 18324, and circuit F is 07933.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-05-29

Approved sources of supply for SMD 82008 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard 1/ 2/ microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 3/	Replacement military specification PIN
8200801JA	18324 4/ 4/ 07933	82HS321A/BJA 53S3281J/883B AM27S43/BJA R29771DM/883B	
8200801KA	18324 4/ 4/	82HS321A/BKA AM27S43/BKA 53S3281W/883B	
8200801LA	07933	R29771SM/883B	
8200801XX	4/	AM27S43/BUA	
82008013A	18324 4/ 07933 4/	82HS321A/B3A 53S3281L/883B R29771LM/883B AM27S43/B3A	
8200802JA	4/ 4/ 18324	53S3281AJ/883B AM27S43A/BJA 82HS321A/BJA	
8200802KA	4/ 18324 4/	AM27S43A/BKA 82HS321A/BKA 53S3281AW/883B	
8200802XX	4/	AM27S43A/BUA	
82008023A	4/ 18324 4/	AM27S43A/B3A 82HS321A/B3A 53S3281AL/883B	
8200803JA	4/ 18324	53S3281BJ/883B 82HS321B/BJA	
8200803KA	4/ 18324	53S3281BW/883B 82HS321B/BKA	

See footnotes at end of table.

Standardized military drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Replacement military specification PIN
82008033A	4/ 18324	53S3281BL/883B 82HS321B/B3AB	
8200804JA	4/ 18324	R29771DM/883B 82HS321C/BJA	
8200804KA	18324 4/	82HS321C/BKA R29771FM/883B	
8200804LA	4/	R29771SM/883B	
82008043A	4/ 18324	R29771LM/883B 82HS321C/B3A	

1/ Military drawing and DSCC drawing PIN's formerly had a programming procedure letter within the military drawing PIN: these parts are interchangeable with parts that are now marked without the programming procedure letter within the military drawing number, i.e. 82008C1JX is interchangeable with 8200801JX.

2/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

4/ Not available from an approved source.

Vendor CAGE number	Vendor name and address	Fusible link
07933	Raytheon Co. 350 Ellis St. P.O. Box 7016 Mountain View, CA 94039-7016	NICR
18324	Signetics Corporation 811 E. Arques Avenue P.O. Box 3409 Sunnyvale, CA 94008-3409	Zapped vertical emitter

The information contained here is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.