V104AJ36, V104AJ236 (256K x 36, 512K x 36) CMOS MEMORY MODULES

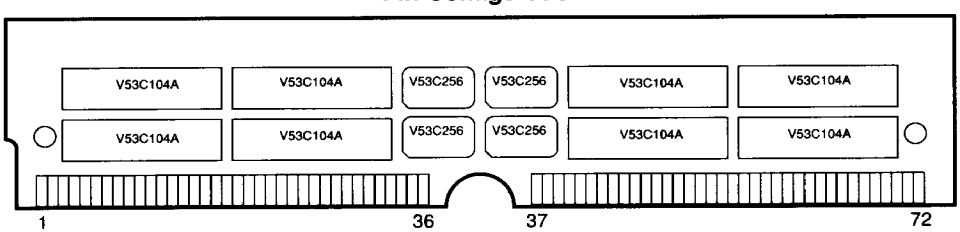
Features

- 262,144 x 36 bit or 524, 288 x 36 bit organizations
- Utilizes 256K x 4 and 256K x 1 CMOS DRAMs
- Fast access times 70 ns, 80 ns, 100 ns
- Fast Page mode operation
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, and Hidden refresh capability
- Single 5 V ±10% supply
- All I/O are fully TTL compatible
- Standard 72-lead single-in-line module

Description

The V104AJ36 Memory Module is organized as 262,144 x 36 bits in a 72-lead single-in-line module. The 256K x 36 memory module uses 8 Vitelic 256K x 4 DRAMs and 4 Vitelic 256K x 1 DRAMs. The V104AJ236 is organized as 524, 288 x 36 bits in the 72 lead single-in-line module and uses 16 Vitelic 256K x 4 DRAMs and 8 Vitelic 256K x 1 DRAMS. The x36 modules are ideal for use in systems where high memory density and fast access times are needed. This includes IBM PS/2 compatibles as well as advanced PC/Workstation systems.

V104AJ36/236 Pin Configuration



1	VSS	16	A4	31	A8	*45	NC [$\overline{RAS1}$]	59	VDD
2	DQ0	17	A5	32	NC	46	NC	60	DQ32
3	DQ18	18	A6	*33	NC [$\overline{RAS3}$]	47	$\overline{W}$	61	DQ14
4	DQ1	19	NC	34	$\overline{RAS2}$	48	NC	62	DQ33
5	DQ19	20	DQ4	35	DQ26	49	DQ9	63	DQ15
6	DQ2	21	DQ22	36	DQ8	50	DQ27	64	DQ34
7	DQ20	22	DQ5	37	DQ17	51	DQ10	65	DQ16
8	DQ3	23	DQ23	38	DQ35	52	DQ28	66	NC
9	DQ21	24	DQ6	39	VSS	53	DQ11	67	*1
10	VDD	25	DQ24	40	$\overline{CAS0}$	54	DQ29	68	*2
11	NC	26	DQ7	41	$\overline{CAS2}$	55	DQ12	69	*3
12	A0	27	DQ25	42	$\overline{CAS3}$	56	DQ30	70	*4
13	A1	28	A7	43	$\overline{CAS1}$	57	DQ13	71	NC
14	A2	29	NC	44	$\overline{RAS0}$	58	DQ31	72	VSS
15	A3	30	VDD						

* Signal in [ ] is V104AJ236 only, otherwise pins are identical

V104AJ36

	-70	-80	-10
*1	VSS	VSS	VSS
*2	NC	NC	NC
*3	VSS	NC	VSS
*4	NC	VSS	VSS

V104AJ236

	-70	-80	-10
*1	NC	NC	NC
*2	VSS	VSS	VSS
*3	NC	VSS	NC
*4	VSS	VSS	NC

Device Usage Chart

Operating Temperature Range	Organization		Module Type	Access Time (ns)			Power	
	256K x 36	512K x 36	S	70	80	100	Std	Low
0°C–70°C	•	•	•	•	•	•	•	•

V104J36/J236 Rev. 00

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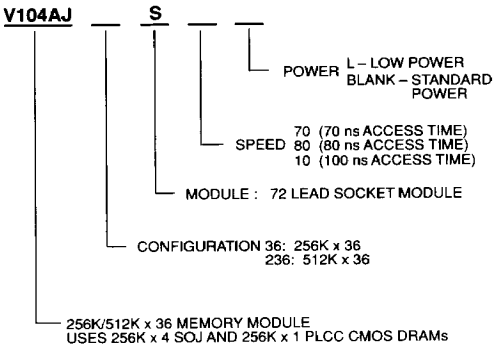
Part Number Information



Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... –1.0 to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... –1.0 to +7.0 V
Data Out Current ..... 50 mA
V104AJ36 Power Dissipation ..... 12.0 W
V104AJ236 Power Dissipation ..... 24.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

V104AJ36 Pin Names

Name	Description
A0–A8	Address Inputs
$\overline{RAS}$, $\overline{RAS2}$	Row Address Strobes
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobes
$\overline{W}$	Read/Write Input
DQ0–DQ35	Data In/Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

V104AJ236 Pin Names

Name	Description
A0–A8	Address Inputs
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobes
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobes
$\overline{W}$	Read/Write Input
DQ0–DQ35	Data In/Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

V104AJ36 Capacitance*

T_A = 0°C TO 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		88	pF
C_{IN}	Input Capacitance, $\overline{W}$		104	pF
$C_{IN(DQ)}$	Input Capacitance, Data Inputs		17	pF
$C_{IN(RAS)}$	Input Capacitance, $\overline{RAS0}$, $\overline{RAS2}$		57	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS0}$–$\overline{CAS3}$		36	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.2		µF

*Note: Capacitance is sampled and not 100% tested

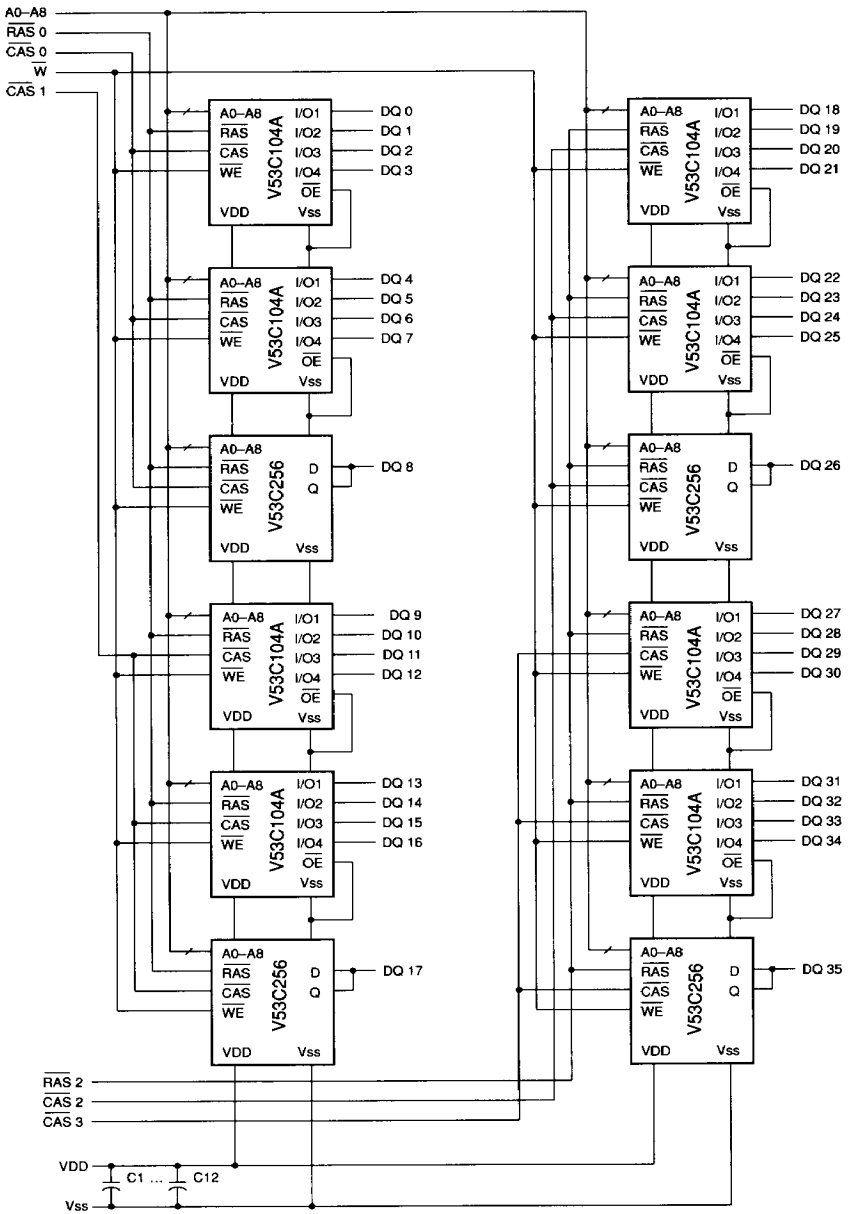
V104AJ236 Capacitance*

T_A = 0°C TO 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		176	pF
C_{IN}	Input Capacitance, $\overline{W}$		208	pF
$C_{IN(DQ)}$	Input Capacitance, Data Inputs		17	pF
$C_{IN(RAS)}$	Input Capacitance, $\overline{RAS0}$–$\overline{RAS3}$		57	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS0}$–$\overline{CAS3}$		36	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.2		µF

*Note: Capacitance is sampled and not 100% tested

V104AJ36 Functional Diagram



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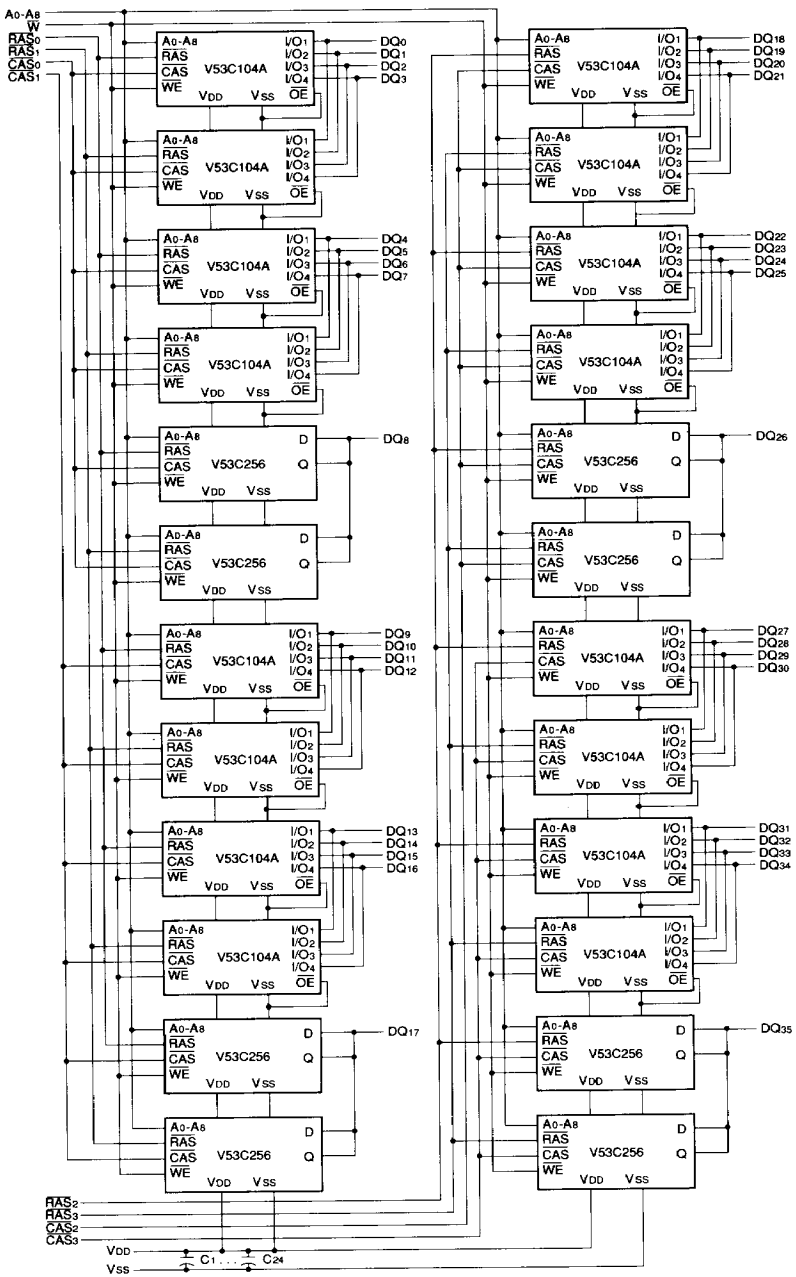
V104AJ236 Functional Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Power	Access Time (ns)	V104AJ36		V104AJ236		Unit	Test Conditions	Notes
				Min.	Max.	Min	Max			
I_{LI}	Input Leakage Current (any input pin)				10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)				10		10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		70		960		1920	mA	$t_{RC} = t_{RC}$ (min.)	1,2
			80		840		1680			
			100		720		1440			
I_{DD2}	V_{DD} Supply Current, TTL Standby	STD			30		60	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			24		48			
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh		70		960		1920	mA	$t_{RC} = t_{RC}$ (min.)	2
			80		840		1680			
			100		720		1440			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		70		700		1400	mA	Minimum Cycle	1,2
			80		600		1200			
			100		540		1080			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			40		80	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
		LOW			26		52			
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD			20		40	mA	$\overline{RAS} \ge V_{DD}-0.2$ V, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			12.8		25.6			
V_{IL}	Input Low Voltage (all inputs)			−1	0.8	−1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)			2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage			2.4		2.4		V	I_{OH} = −5 mA	

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AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		70		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	25	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		20		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20		25	ns	6,7
17	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	6,8,9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		45	ns	6,7,10
19	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
20	t_{CH2QZ}	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	20	0	20	0	20	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		75		ns	
22	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	11

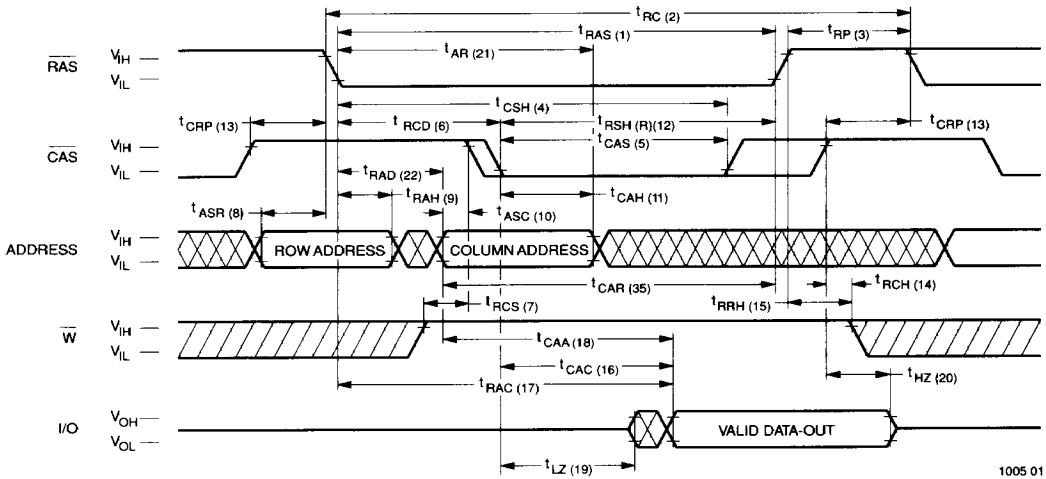
AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		25		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		20		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		20		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		75		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		ns	
30	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		20		ns	14
32	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	75		75		90		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		ns	
34	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55		60		75		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
39	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
40	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		30		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (512 Cycles)		8		8		8	ms	17

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit and are not referenced to the output voltage levels.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

Waveforms of Read Cycle



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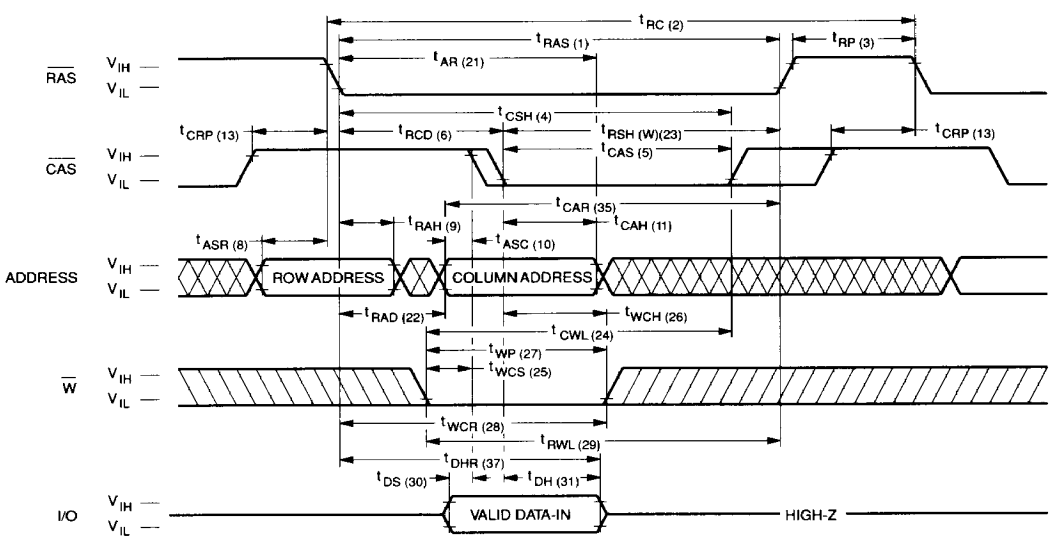
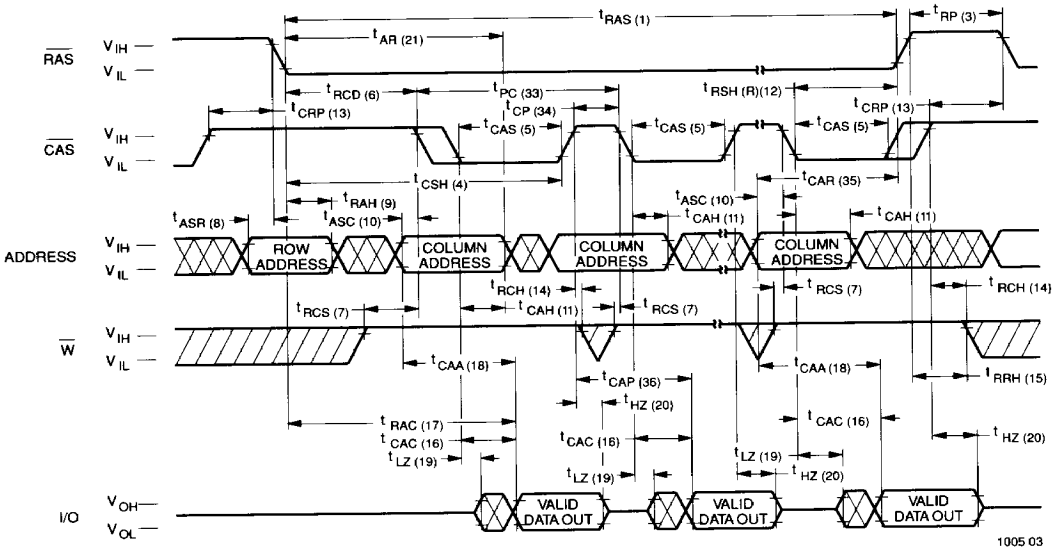
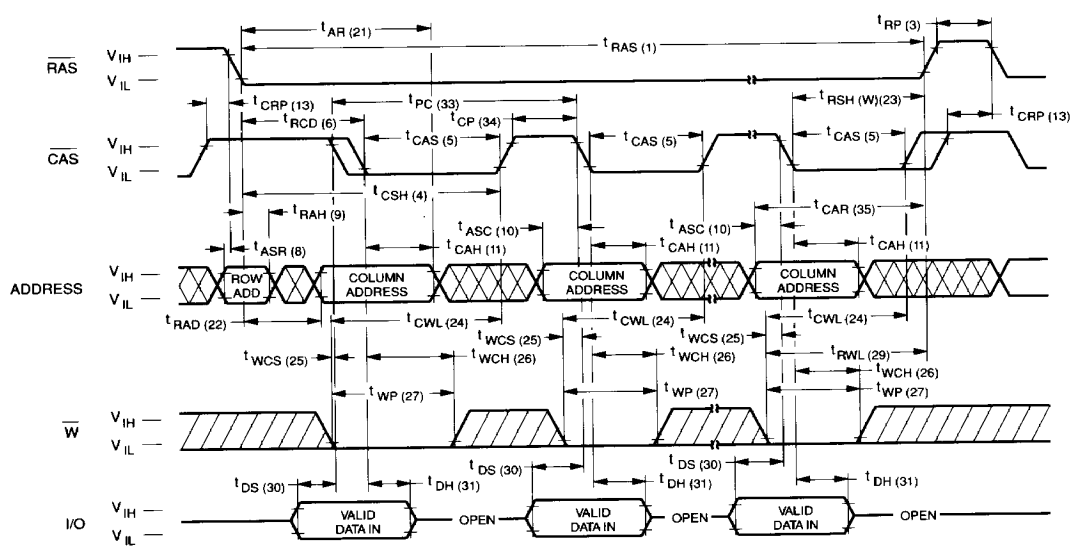
Waveforms of Early Write Cycle



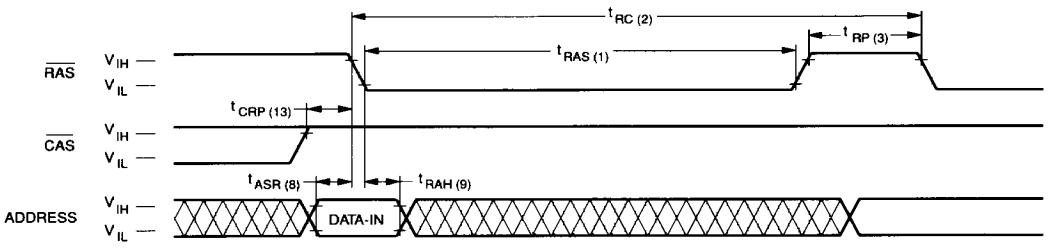
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle

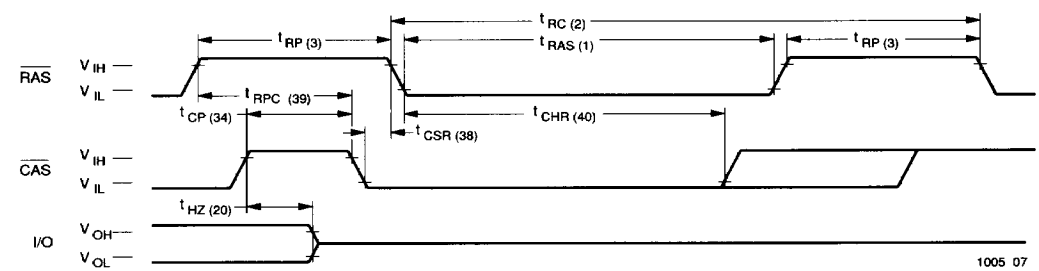


Waveforms of $\overline{RAS}$-Only Refresh Cycle



NOTE: $\overline{W}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



NOTE: $\overline{W}$, $A_0 - A_8$ = Don't care

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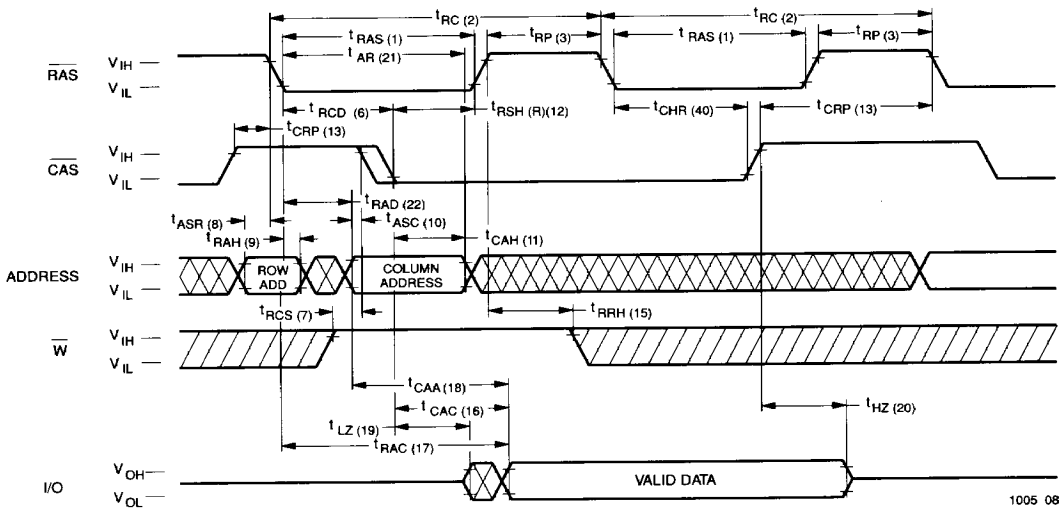
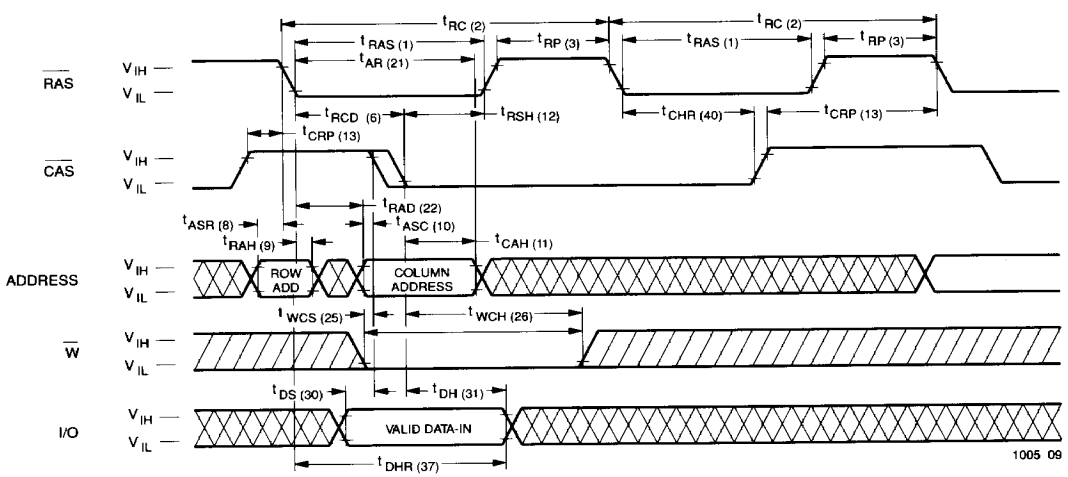
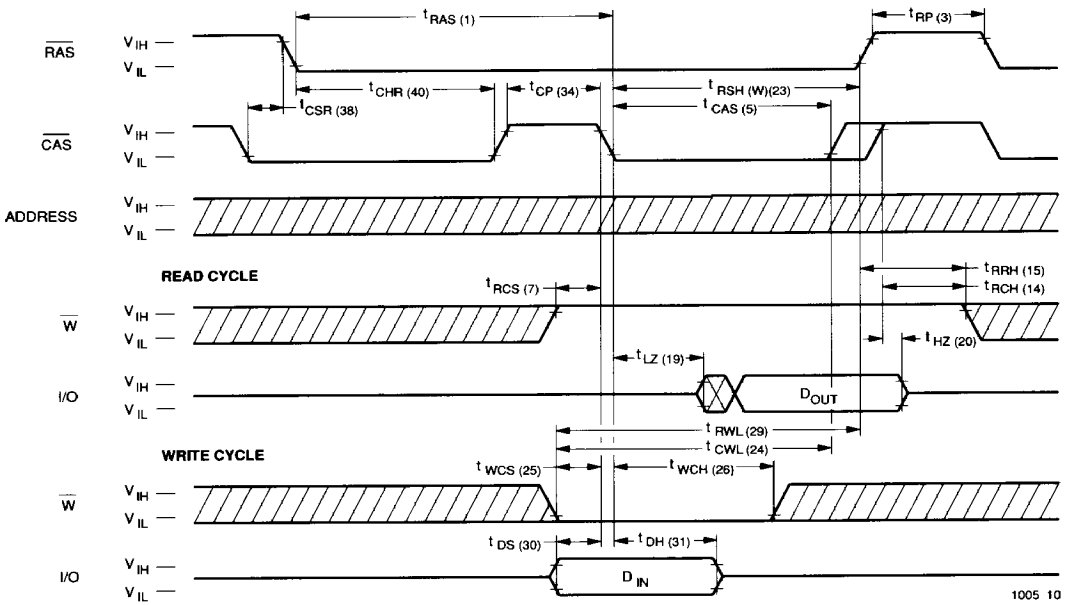
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Refresh Counter Test Cycle



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