MOS INTEGRATED CIRCUIT
μPD9322

YC INTERPOLATION (YCI) LSI FOR IMPROVED DEFINITION TV

DESCRIPTION

The μPD9322 is a YC interpolation (YCI) LSI for the improved definition TV (IDTV). This LSI generates interpolation signals for double-speed conversion from the luminance and color signals obtained by the YC processing LSI (YCP).

In combination with five LSIs (YCS, YCP, MDP, CDU, and CKG), this LSI can be used to configure an IDTV signal processing system.

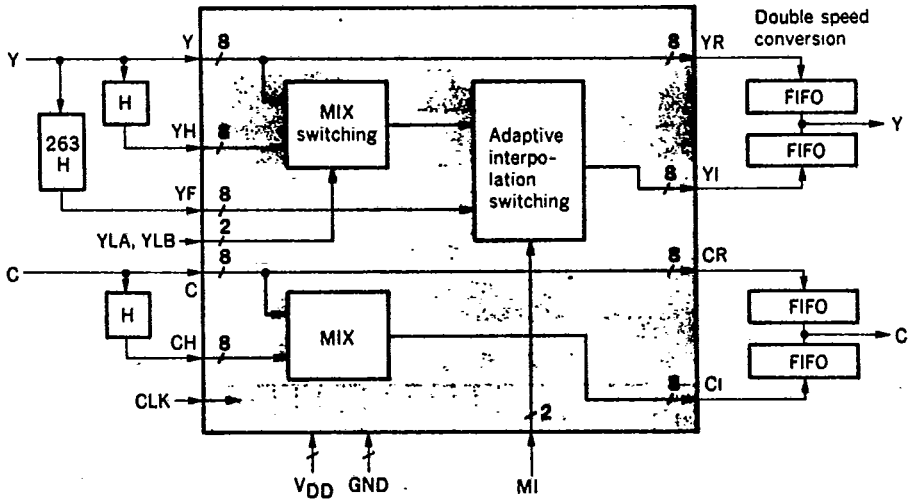
FEATURES

- Capable of selecting optimum Y interpolating filter accordingly to the displayed picture:
  - Interfield interpolation
  - Interline interpolation
- Built-in color interpolation filter circuit.
- +5 volt single power supply.
- Low-power consumption due to CMOS circuiting.

ORDERING INFORMATION

Part Number	Package
μPD9322GF-3BA	100 PIN PLSTIC QFP (14 x 20)

BLOCK DIAGRAM



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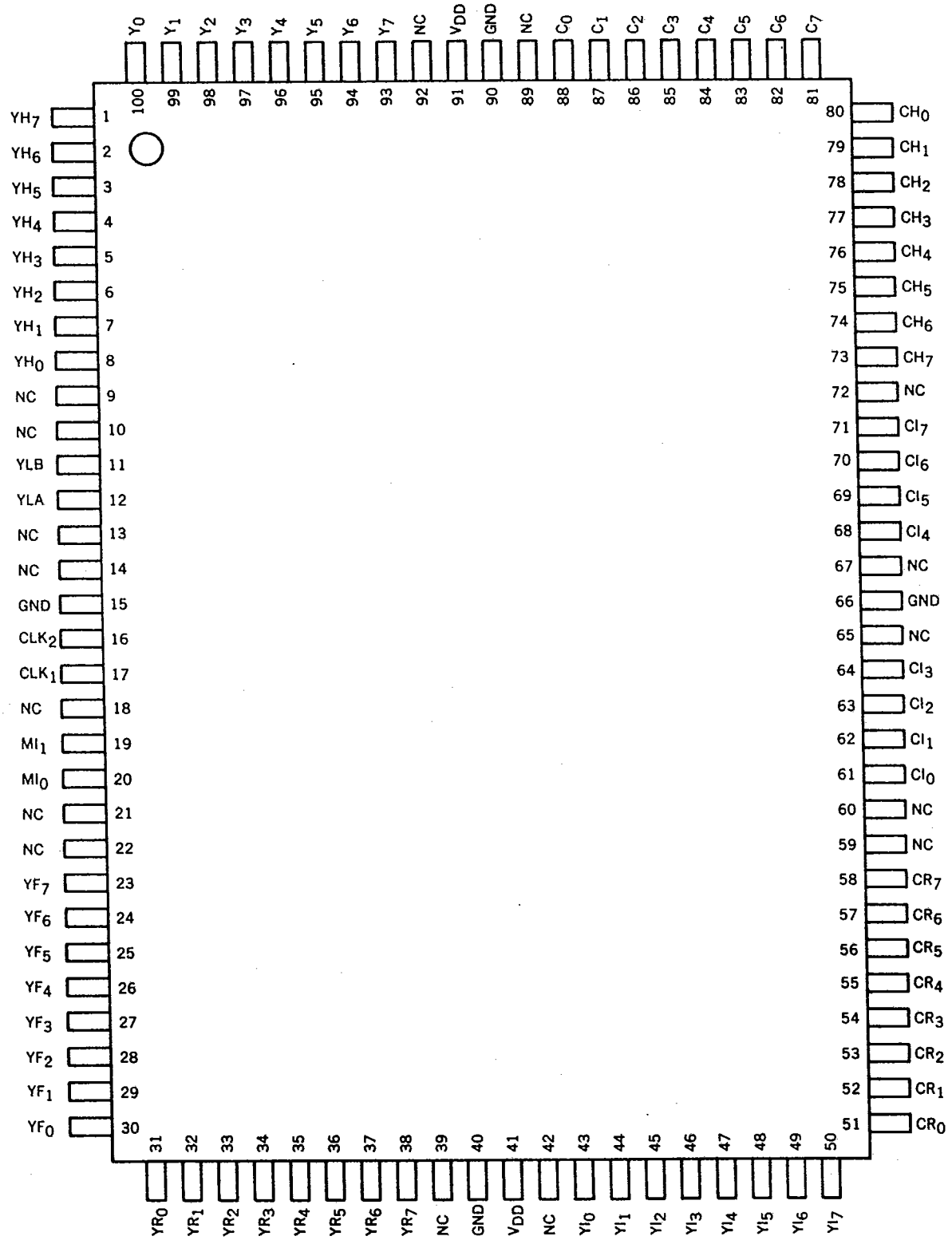
CONNECTION DIAGRAM (Top View)



LSI SYSTEM CONFIGURATION FOR THE IDTV

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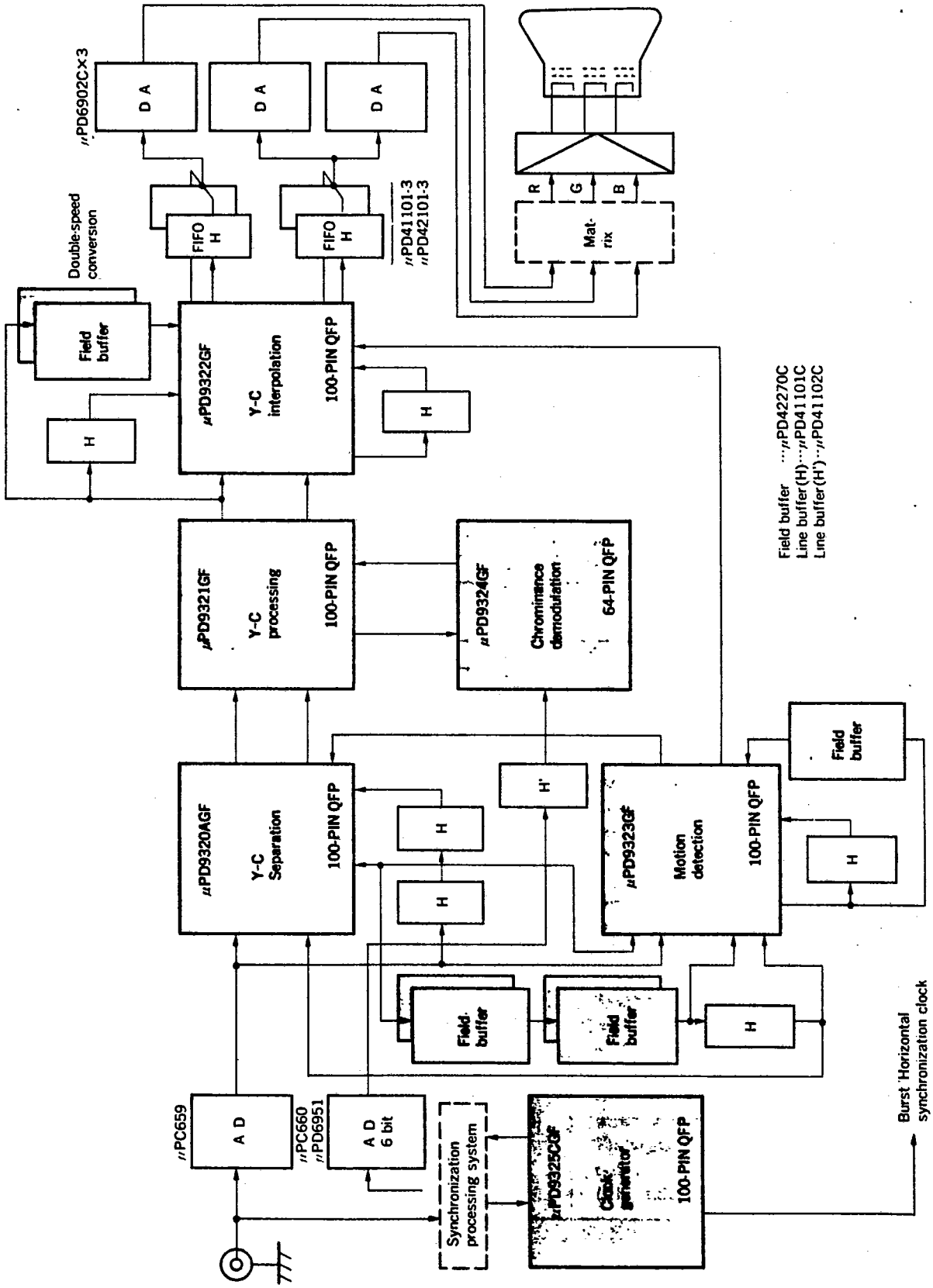

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ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Source Voltage	V_{DD}	−0.5 to 7.0	V
Input Voltage	V_{IN}	−0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	20	mA
Package Allowable Dissipation	P_D	400	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Source Voltage	V_{DD}	4.5	5.0	5.5	V	
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD}	V	Input terminals: Y, C, MI, and CLK (CMOS input)
High-Level Input Voltage	V_{IH}	0.7 V_{DD}			V	
Low-Level Input Voltage	V_{IL}	0		0.8	V	Input terminals: YH, YF, and CH (TTL input)
High-Level Input Voltage	V_{IH}	2.4			V	
Clock Frequency	F_{CLK}		14.3		MHz	

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ±10 %, T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{DD}		20		mA	
Low-Level Output Current	I_{OL}	4	11		mA	V_{OL} = 0.4 V
High-Level Output Current	$-I_{OH}$	4	8		mA	$V_{OH} = V_{DD} - 0.4$ V
Input Current	$\pm I_I$			10	μA	$V_I = V_{DD}$ or GND
Input Current	$-I_I$	25	80	260	μA	V_I = GND
Input Current	I_I	25	80	260	μA	$V_I = V_{DD}$
Output Delay Time	T_D		15		ns	
Input Terminal Capacitance	C_{IN}			10	pF	$V_{DD} = V_I = 0$ f = 1 MHz
Output Terminal Capacitance	C_{OUT}			15	pF	

TERMINAL DESCRIPTION (YCI)

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TERMINAL SYMBOL	TERMINAL NAME	TERMINAL NUMBER	FUNCTIONS	
Y_0 to Y_7	Luminance input	100 to 93	Input (CMOS)	Inputs the YCP luminance output. (Y_0: LSB, Y_7: MSB)
YH_0 to YH_7	Luminance input (1H-delayed)	8 to 1	Input (TTL)	Inputs the 1H delayed luminance signal. Used as the input for the Y interline interpolation of the YC separation. (YH_0: LSB, YH_7: MSB)
YF_0 to YF_7	Luminance input (1F-delayed)	30 to 23	Input (TTL)	Inputs the 1 Field (263 H) delayed luminance signal. Used as the input for the Y field interpolation of the YC separation. (YF_0: LSB, YF_7: MSB)
C_0 to C_7	Chrominance input (1F-delayed)	88 to 81	Input (CMOS)	Inputs the YCP chrominance output. (C_0: LSB, C_7: MSB)
CH_0 to CH_7	Chrominance input (delayed by 1H)	80 to 73	Input (TTL)	Inputs the YCP chrominance output delayed by 1H. Used as input for C-line interpolation. (CH_0: LSB, CH_7: MSB)
YR_0 to YR_7	Luminance signal output	31 to 38	Output (CMOS)	Outputs the signal to the FIFO for double-speed conversion. This terminal outputs the main line luminance signal delayed with respect to the Y input by three clocks. (YR_0: LSB, YR_7: MSB)
YI_0 to YI_7	Interpolation luminance output	43 to 50	Output (CMOS)	The output is transferred to the FIFO for double-speed conversion. The signal is the interpolation luminance output. (YI_0: LSB, YI_7: MSB)
CR_0 to CR_7	Chrominance output	51 to 58	Output (CMOS)	Sends the output to the FIFO for double-speed conversion. The signal is the main line chrominance output. The timing is delayed with respect to the C input by three clocks. (CR_0: LSB, CR_7: MSB)
CI_0 to CI_7	Interpolation chrominance input	61 to 64 68 to 71	Output (CMOS)	Sends the output to the FIFO for double-speed conversion. The signal is the interpolation chrominance output. (CI_0: LSB, CI_7: MSB)

YCI

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TERMINAL SYMBOL	TERMINAL NAME	TERMINAL NUMBER	FUNCTIONS	
MI_0 MI_1	Motion signal input	20 19	Input (CMOS)	Inputs the Y interpolation motion signal MI from the MDP. Adaptively selects the line/field output of the luminance interpolation output. (MI_0: LSB, MI_1: MSB)
YLA YLB	Interpolation mode selection	12 11	Input (CMOS) Pull-up-R Pull-down-R	Selects the interline Y interpolation mode. The average and double write features are available. The normal operation is based on the average; YLA is connected to the V_{DD} and YLB to the GND terminal.
CLK_1 CLK_2	Clock	17 16	Input (CMOS)	The clock is input from the CKG. The clock is the 4 F_{SC} (14.3 MHz) system clock.
V_{DD}	Supply terminal	41 91		The supply input terminal. Apply +5 volts to this terminal.
GND	Grounding terminal	15 40 66 90		Grounding terminal.

DESCRIPTION OF FUNCTIONS

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The μPD9322 has a built-in capability to generate the Y (luminance) interpolation signal for double-speed conversion and the C (color) interpolation signal.

1. Y Interpolation Circuit

This circuit generates the luminance interpolation signal from the luminance signal that has been processed by the μPD9321 and delayed by the μPD9324 (CDU).

The luminance interpolation signal is adaptively selected by the Y interpolation motion signal (MI) supplied from the motion detection IC (the μPD9323) (either the in-the-field up/down interline interpolation or the field interpolation).

The Y interpolation motion signal (MI) is input in two bits.

When this signal is set to "00," the interpolation luminance output (YI) selects the one field-delayed outputs; when set to "11," the average of the upper and lower interline distance in the field.

Table 1 Selection of Interpolation Luminance Output

Motion signal input		Interpolation luminance output (YI)	
MI_1	MI_0	Interline interpolation	Field interpolation
0	0	× 0	× 1
0	1	× 0.375	× 0.625
1	0	× 0.625	× 0.325
1	1	× 1	× 0

YI = interline interpolation + field interpolation

The average of the up and down line is usually selected as the interline interpolation data. However, by using the interpolation mode selection terminal (YLA, YLB), the upper and the lower line data can be selected (called double writing).

Table 2 Line Interpolation Mode Selection

Interpolation mode selection		Line interpolation output
YLB	YLA	
0	0	Double writing of upper line
0	1	Average of the upper and lower line
1	0	–
1	1	Double writing of the lower line

The luminance output (YR) and interpolation luminance output (YI) are delayed with respect to the luminance output (Y) by three clocks.

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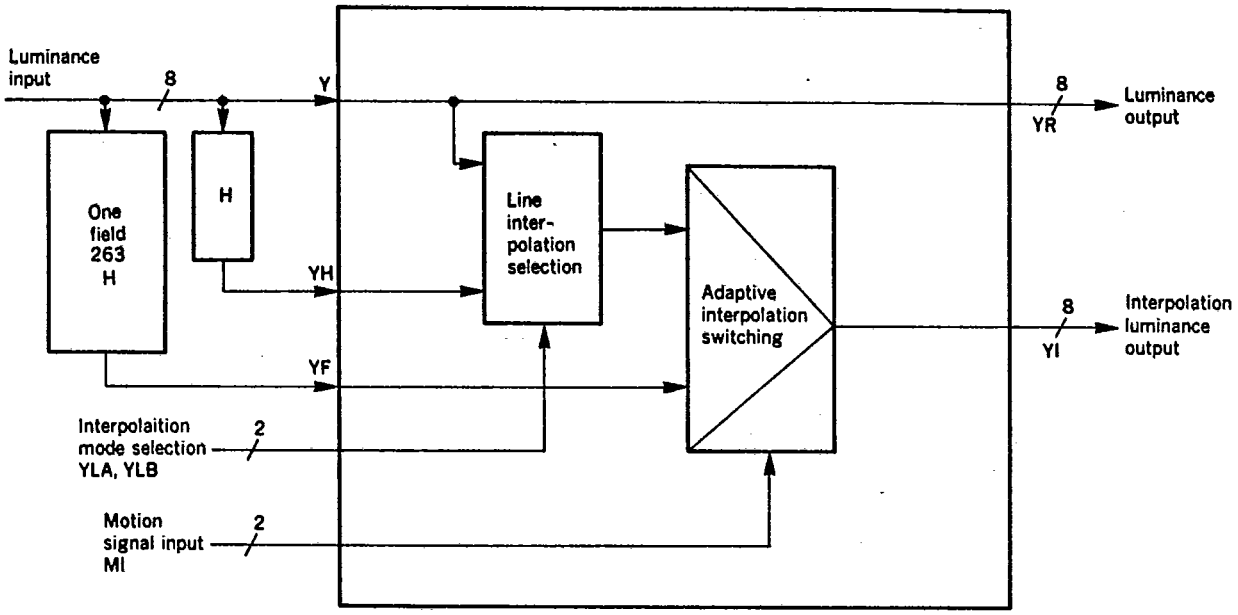
Fig. 1 Diagram of the Y Interpolation Circuit



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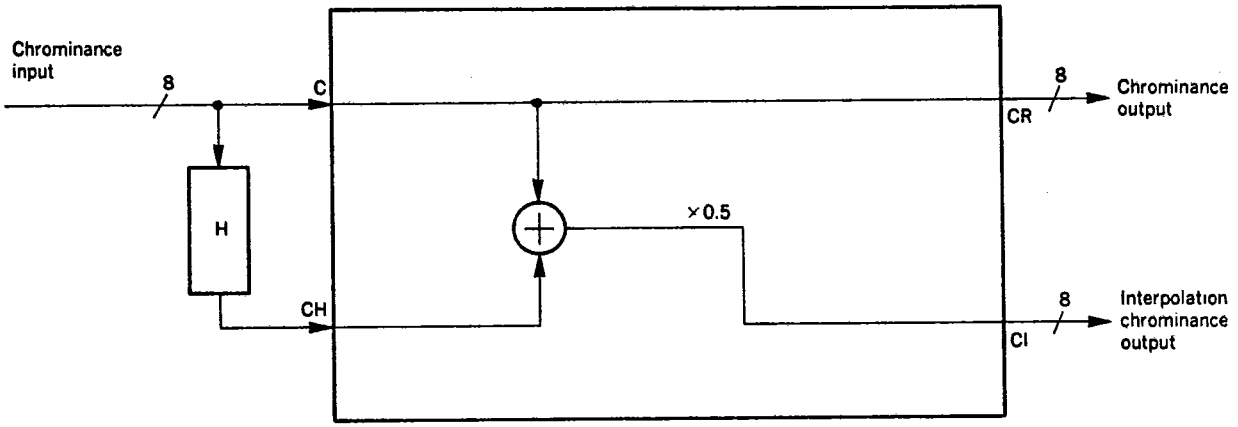
2. Color Interpolation Circuit

This circuit generates the color interpolation signal.

The interpolation signal is generated from the chrominance signal processed by the μPD9321 for chrominance demodulation by averaging the distance between the up and down line.

The timings of the chrominance output (CR) and the interpolation chrominance output (CI) are delayed by three clocks with respect to the chrominance input (C).

Fig. 2 Color Interpolation Circuit



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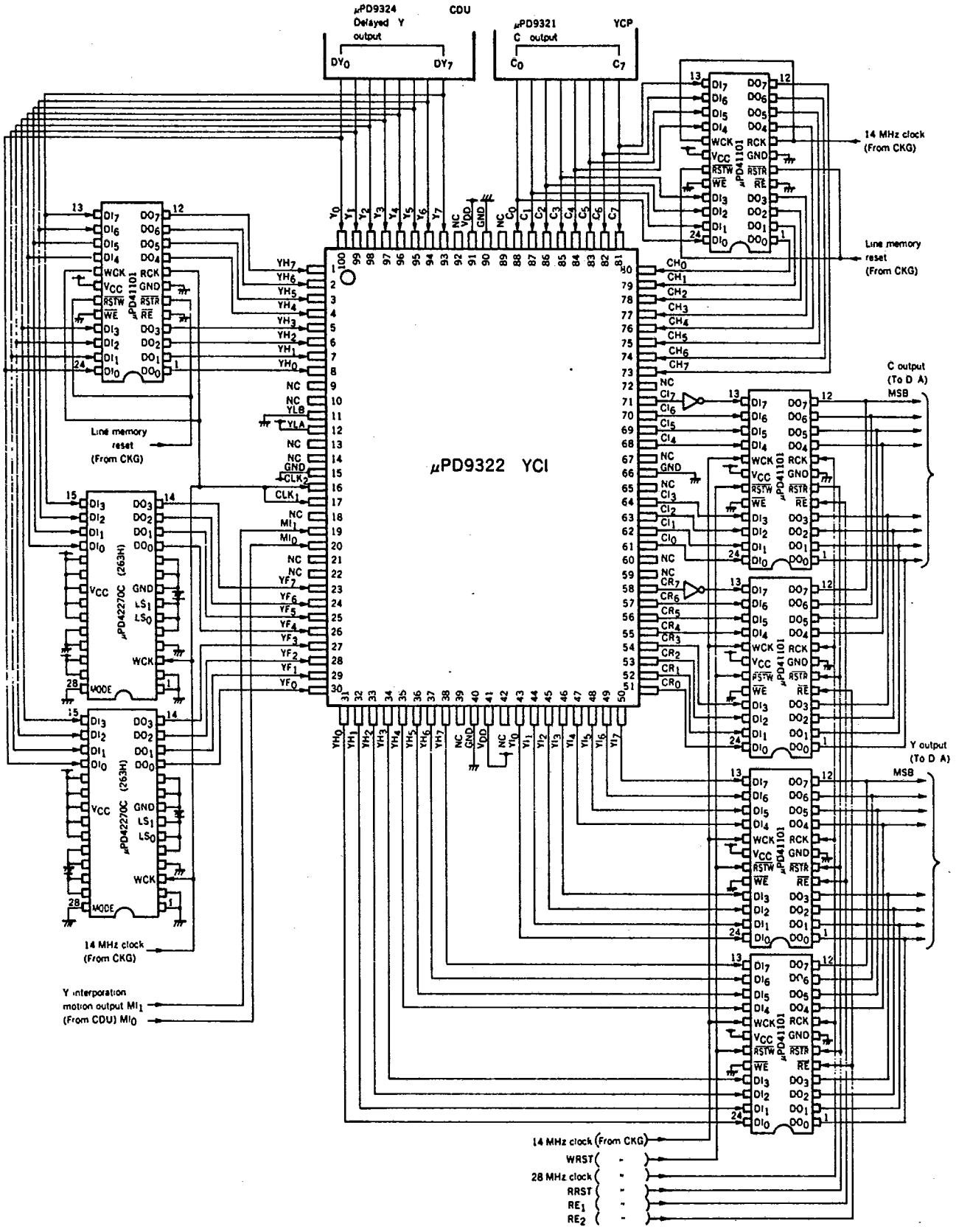
APPLICATION CIRCUIT



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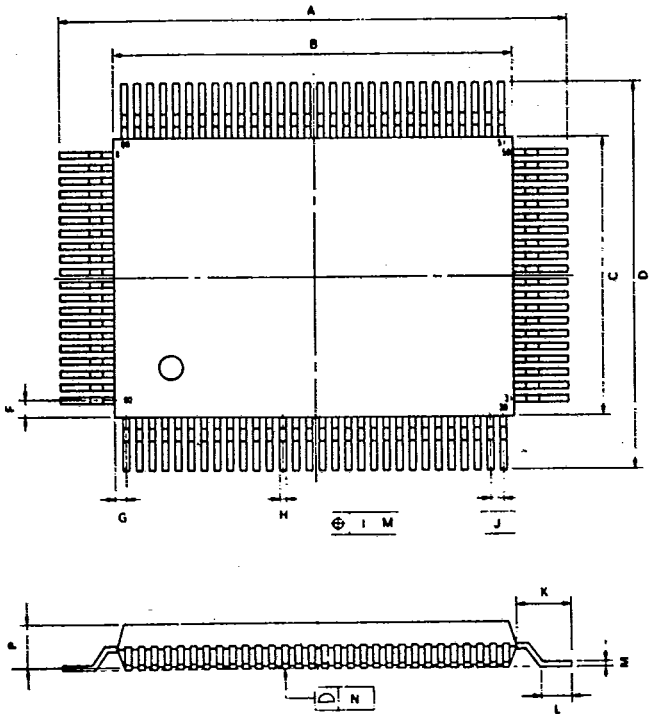
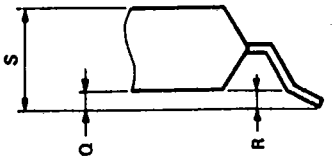
100-PIN PLASTIC QFP (14 x 20)



detail of lead end



P100GF-65-3BA-1

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.6^{\pm 0.4}$	$0.929^{\pm 0.016}$
B	$20.0^{\pm 0.2}$	$0.795^{+0.008}_{-0.009}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
D	$17.6^{\pm 0.4}$	$0.693^{\pm 0.016}$
F	0.8	0.031
G	0.6	0.024
H	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	$1.8^{\pm 0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.