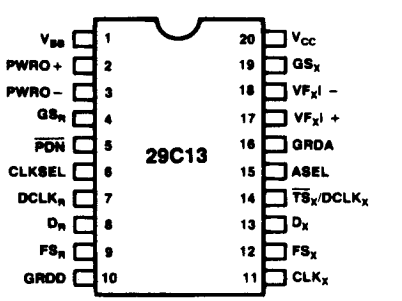
29C13 AND 29C14
CHMOS COMBINED SINGLE-CHIP PCM CODEC AND FILTER

- **29C14 Asynchronous Clocks, 8th Bit Signaling, Loop Back Test Capability**
- **29C13 Synchronous Clocks Only, 300 Mil Package**
- **Low-Power Pin Compatible Version of Intel's 2913 and 2914**
- **28-Pin Plastic Leaded Chip Carrier (PLCC) for Higher Integration**
- **AT&T D3/D4 and CCITT Compatible**
- **3 Low-Power Modes**
  - **— 3.5 mW Typical Power Down**
  - **— 3.5 mW Typical Standby**
  - **— 64 mW Typical Operating**
- **Direct Interface with Transformer or Electronic Hybrids**
- **TTL and CMOS Compatible**

Intel's 29C13 and 29C14 are CHMOS versions of Intel's HMOS 2913 and 2914 family members. CHMOS is a technology built on HMOS-II, thus realizing the high performance and density obtained in that process while achieving the low power consumption typical of CMOS circuits.

The 29C13 and 29C14 retain all the features of the 2913 and 2914: push/pull power amplifiers, μ/A law pin select, on-chip auto zero, sample and hold and precision voltage references, power up clear and tri-state on clock interrupt, two timing modes and two power down modes.



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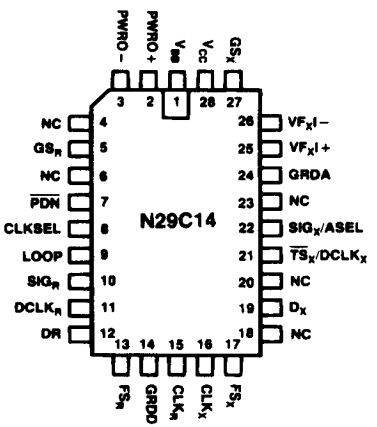

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Figure 1. Pin Configurations

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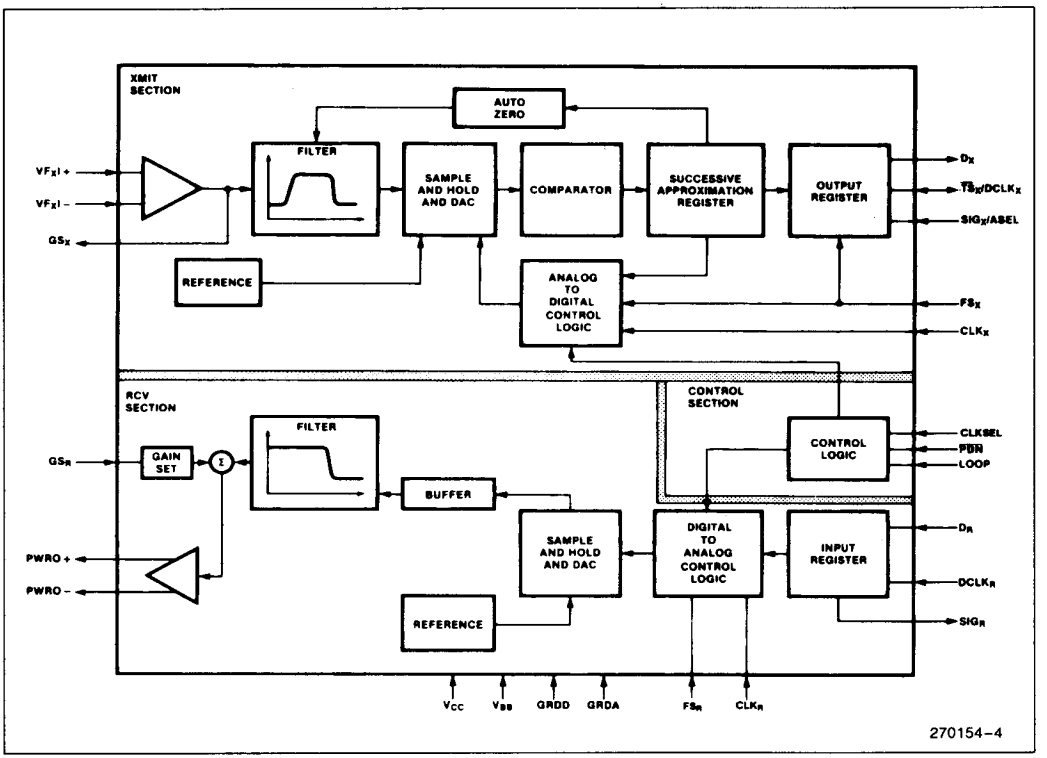


Figure 2. Block Diagram

Table 1. Pin Names

Name	Description	Name	Description
V_{BB}	Power (−5V)	GS_X	Transmit Gain Control
PWRO+, PWRO−	Power Amplifier Outputs	VF_XI-, VF_XI+	Analog Inputs
GS_R	Receive Gain Control	GRDA	Analog Ground
$\overline{PDN}$	Power Down Select	NC	No Connect
CLKSEL	Master Clock Frequency Select	SIG_X	Transmit Signaling Input
LOOP	Analog Loop Back	ASEL	μ- or A-law Select
SIG_R	Receive Signaling Bit Output	$\overline{TS_X}$	Timeslot Strobe/Buffer Enable
$DCLK_R$	Receive Variable Data Clock	$DCLK_X$	Transmit Variable Data Clock
D_R	Receive PCM Input	D_X	Transmit PCM Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+5V)	CLK_R	Receive Master Clock (29C14 only, internally connected to CLK_X on 29C13)

Table 2. Pin Description

Symbol	Function
V_{BB}	Most negative supply; input voltage is −5 volts ±5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO−	Inverting output of power amplifier. Functionally identical and complementary to PWRO+.
GS_R	Input to the gain setting network on the output power amplifier. Transmission level can be adjusted over a 12 dB range depending on the voltage at GS_R.
$\overline{PDN}$	Power down select. When $\overline{PDN}$ is TTL high, the device is active. When low, the device is powered down.
CLKSEL	Input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. CLKSEL = V_{BB} ..... 2.048 MHz CLKSEL = GRDD ..... 1.544 MHz CLKSEL = V_{CC} ..... 1.536 MHz
LOOP	Analog loopback. When this pin is TTL high, the analog output (PWRO+) is internally connected to the analog input (VF_XI+), GS_R is internally connected to PWRO−, and VF_XI- is internally connected to GS_X. A 0 dBm0 digital signal input at D_R is returned as a +3 dBm0 digital signal output at D_X.
SIG_R	Signaling bit output, receive channel. In fixed data rate mode, SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock which operates at TTL levels from 64 Kb to 2.048 Mb data rates.
D_R	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock; CLK_R in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8 KHz frame synchronization clock input/timeslot enable, receive channel. A multi-function input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 600 microseconds.
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK_R	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
CLK_X	Transmit master and data clock for the fixed data rate mode; transmit master clock only in variable data rate mode.
FS_X	8 KHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 600 microseconds.
D_X	Transmit PCM output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock: CLK_X in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64 Kb to 2.048 Mb data rates.
SIG_X/ASEL	A dual purpose pin. When connected to V_{BB}, A-law operation is selected. When it is not connected to V_{BB} this pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D_X lead. If not used as an input pin, ASEL should be strapped to either V_{CC} or GRDD.
NC	No Connect
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI+	Non-inverting analog input to uncommitted transmit operational amplifier.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of transmit input channel op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply; input voltage is +5 volts ±5%.

FUNCTIONAL DESCRIPTION

The 29C13 and 29C14 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended to be used at the analog termination of a PCM line or trunk.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

SWITCHING

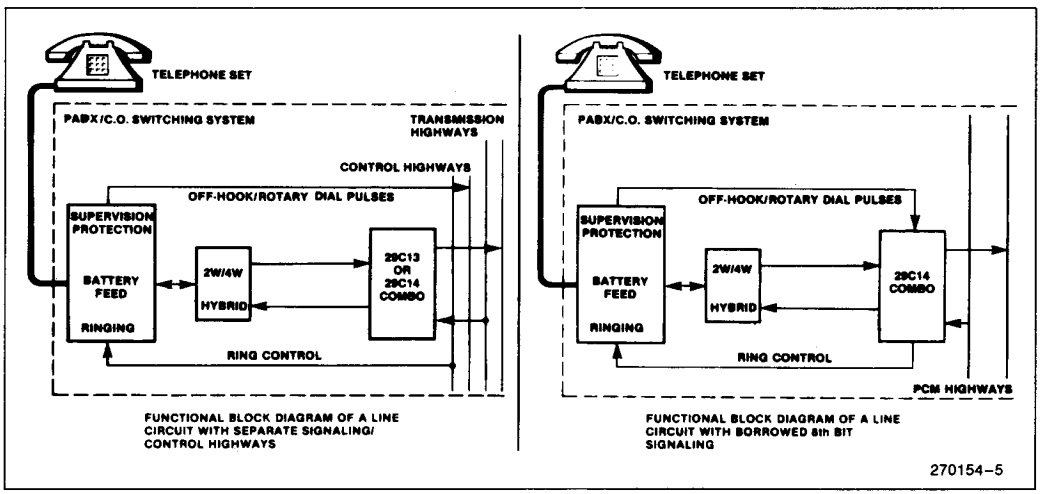


Figure 3a. Typical Line Terminations

CHANNEL BANKS

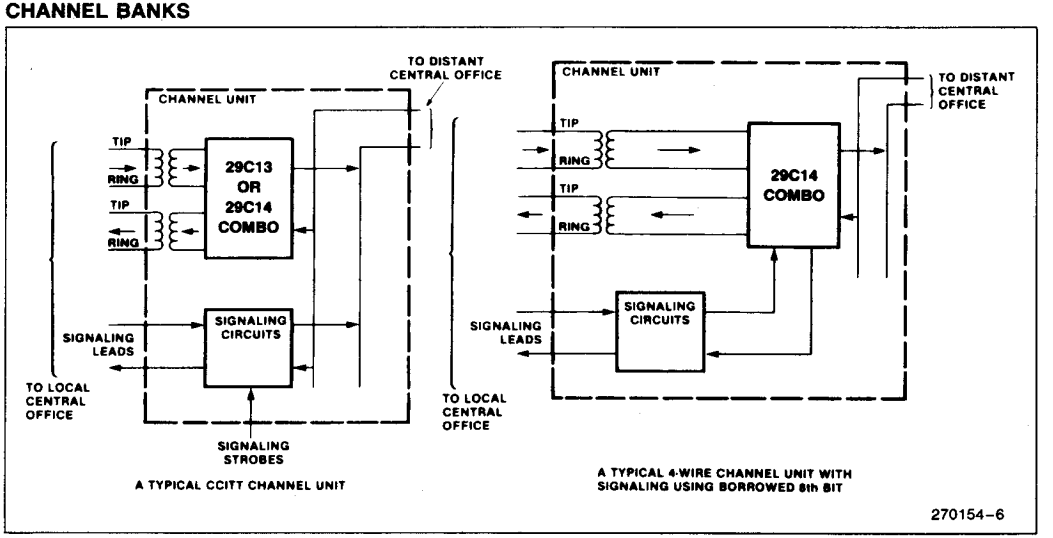


Figure 3b. Typical Line Terminations

GENERAL OPERATION

System Reliability Features

The combochip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The 29C13 and 29C14 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS}_X$ are held in a high impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, D_X, $\overline{TS}_X$, and signaling will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 milliseconds to reach their equilibrium value due to the autozero circuit settling time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIG_R is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIG_R will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability, $\overline{TS}_X$ and D_X will be placed in a high impedance state approximately 30 μs after an interruption of CLK_X. Similarly, SIG_R will be held low approximately 30 μs after an interruption of CLK_R. These interruptions could possibly occur with some kind of fault condition.

Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most 29C13/C14 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to the value shown in Table 3. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumption is reduced to the value shown in Table 3. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Fixed Data Rate Mode

Fixed data rate timing, which is 2910A and 2911A compatible, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clocks CLK_X and CLK_R, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

Table 3. Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	$\overline{PDN}$ = TTL low	3.5 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state within 10 μs.
Standby Mode	FS_X and FS_R are TTL low	3.5 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state 600 microseconds after FS_X and FS_R are removed.
Only transmit is on Standby	FS_X is TTL low	35 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 300 milliseconds.
Only receive is on Standby	FS_R is TTL low	35 mW	SIG_R is placed in a TTL low state within 600 microseconds.

CLK_X and CLK_R serve both as master clocks to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS_X and FS_R are 8 KHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by their pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables the signaling function. $\overline{TS}_X$ is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK_X following the rising edge of FS_X. Similarly, on the receive side, data is received on the first eight falling edges of CLK_R. The frequency of CLK_X and CLK_R is selected by the CLKSEL pin to be either 1.536, 1.544, or 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clocks CLK_X and CLK_R, bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, which can be asynchronous in the case of the 29C14, synchronous in the case of the 29C13, from 64 KHz to 2.048 MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125 μs frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

Signaling

Signaling can only be performed with the 24-pin device in the fixed data rate timing mode ($DCLK_R = V_{BB}$). Signaling frames on the transmit and receive sides are independent of one another and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the codec will encode the incoming analog signal and substitute the signal present on SIG_X for the least significant bit of the encoded PCM word. Similarly, in a receive signaling frame, the codec will decode the seven most significant bits according to CCITT recommendation G.733 and output the logical state of the LSB on the SIG_R lead until it is updated in the next signaling frame. Timing relationships for signaling operation are shown in Figure 4.

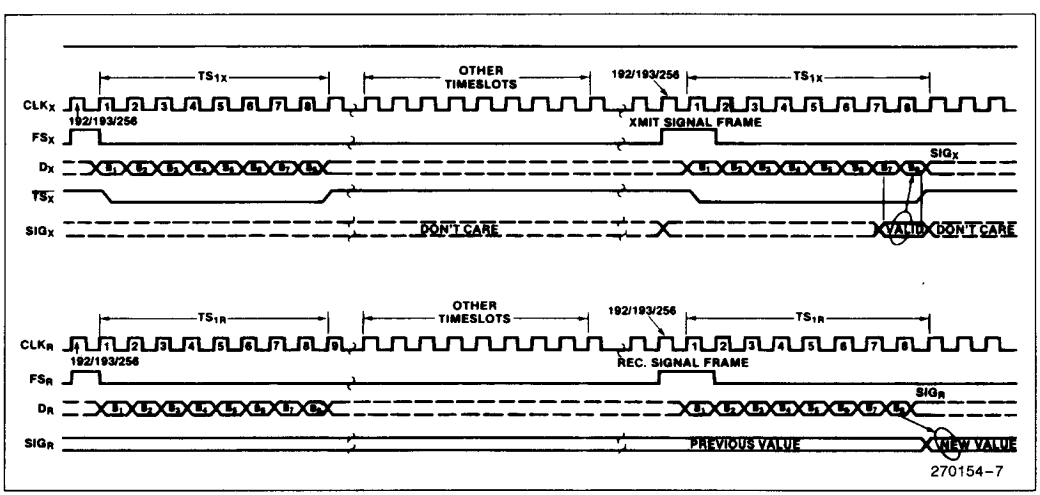


Figure 4. Signaling Timing (Used Only with Fixed Data Rate Mode)

Asynchronous Operation

The 29C14 can be operated with asynchronous clocks in either the fixed or variable data rate modes. In order to avoid crosstalk problems associated with special interrupt circuitry, the design of the Intel 29C13/C14 combochip includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. CLK_X and $DCLK_X$ are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (refer to Variable Data Rate Timing Diagrams). This approach requires the provision of two separate master clocks, even in variable data rate mode, but avoids the use of a synchronizer which can cause intermittent data conversion errors.

Analog Loopback

A distinctive feature of the 29C14 is its analog loopback capability. This feature allows the user to send a control signal which internally connects the analog input and output ports. As shown in Figure 5, when LOOP is TTL high the analog output (PWRO+) is internally connected to the analog input (VF_XI+), GS_R is internally connected to PWRO−, and VF_XI- is internally connected to GS_X.

With this feature, the user can test the line circuit remotely by comparing the digital codes sent into the receive channel (D_R) with those generated on the transmit channel (D_X). Due to the difference in transmission levels between the transmit and receive sides, a 0 dBm0 code sent into D_R will emerge from D_X as a +3 dBm0 code, an implicit gain of 3 dB. Thus, the maximum signal input level which can be tested using analog loopback is 0 dBm0.

Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections and each is trimmed independently during the manufacturing process. The reference value is then further trimmed in the gain setting op-amps to a final precision value. With this method the combochip can achieve the extremely accurate Digital Milliwatt Responses specified in the transmission parameters, providing the user a significant margin for error in other board components.

Conversion Laws

The 29C13 and 29C14 are designed to operate in both μ-law and A-law systems. The user can select either conversion law according to the voltage present on the SIG_X/ASEL pin. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for μ-law and A-law conversion. If A-law operation is desired, SIG_X should be tied to V_{BB}. Thus, signaling is not allowed during A-law operation. If μ = 255-law operation is selected, then SIG_X is a TTL level input which modifies the LSB of the PCM output in signaling frames.

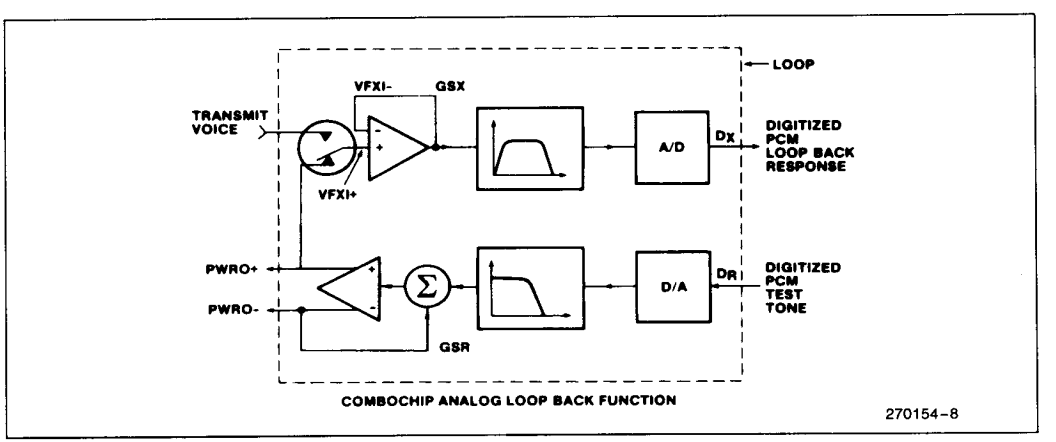


Figure 5. Simplified Block Diagram of 29C14 Combochip in the Analog Loopback Configuration

TRANSMIT OPERATION

Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of ±2.17 volts, a DC offset of 25 mV, and a typical voltage gain of 10,000. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10 kilohms in parallel with less than 50 pF. A DC path must be provided at VF_XI+. The input op amp can also be used in the inverting mode or differential amplifier mode (see Figure 6).

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.714. The 29C13 and 29C14 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 8.

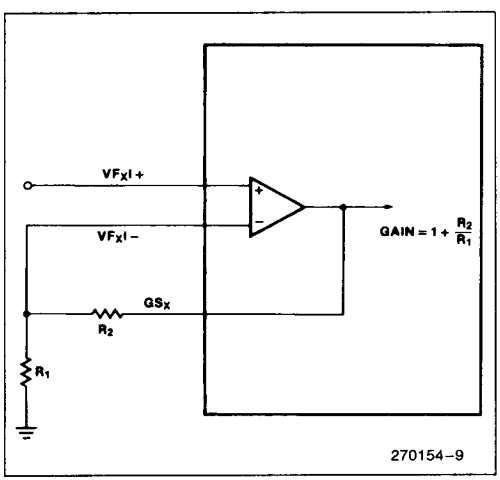


Figure 6. Transmit Filter Gain Adjustment

A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique; the sign bit from the encoder output is long term averaged and subtracted from the input to the encoder. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.714. The filter contains the required compensation for the (sin x)/x response of such decoders. The receive filter characteristics and specifications are shown in Figure 9.

Table 4. Zero Transmission Level Points

Symbol	Parameter	Value	Units	Test Conditions
$0TLP1_X$	Zero Transmission Level Point Transmit Channel (0 dBm0) μ-law	+2.76 +1.00	dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_X$	Zero Transmission Level Point Transmit Channel (0 dBm0) A-law	+2.79 +1.03	dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP1_R$	Zero Transmission Level Point Receive Channel (0 dBm0) μ-law	+5.76 +4.00	dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_R$	Zero Transmission Level Point Receive Channel (0 dBm0) A-law	+5.79 +4.03	dBm dBm	Referenced to 600Ω Referenced to 900Ω

Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended or 600 ohms differentially.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS_R input. GS_R is internally connected to an analog gain setting network. When GS_R is strapped to PWRO−, the receive level is unattenuated; when it is tied to PWRO+, the level is attenuated by 12 dB. The output transmission level interpolates between 0 and −12 dB as GS_R is interpolated (with a potentiometer) between PWRO+ and PWRO−. The use of the output gain set is illustrated in Figure 7.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

OUTPUT GAIN SET: DESIGN CONSIDERATIONS

(Refer to Figure 7.)

PWRO+ and PWRO− are low impedance complementary outputs. The voltages at the nodes are:

V_O+ at PWRO+
V_O- at PWRO−

$V_O = (V_O+) - (V_O-)$ (total differential response)

R_1 and R_2 are a gain setting resistor network with the center tap connected to the GS_R input.

A value greater than 10K ohms for $R_1 + R_2$ and less than 100K ohms for R_1 in parallel with R_2 is recommended because:

(a) The parallel combination of $R_1 + R_2$ and R_L sets the total loading.

(b) The total capacitance at the GS_R input and the parallel combination of R_1 and R_2 define a time constant which has to be minimized to avoid inaccuracies.

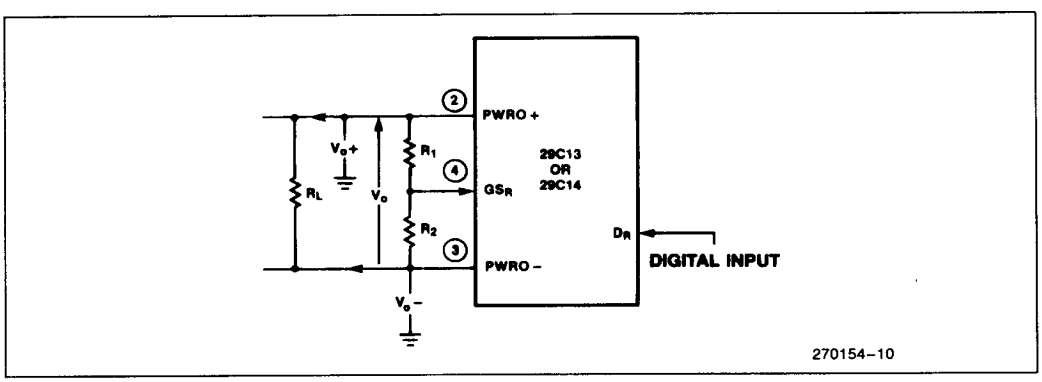


Figure 7. Gain Setting Configuration

A is the gain of the power amplifiers,

where $A = \frac{1 + (R_1/R_2)}{4 + (R_1/R_2)}$

For design purposes, a useful form is R_1/R_2 as a function of A.

$$R_1/R_2 = \frac{4A - 1}{1 - A}$$

(Allowable values for A are those which make R_1/R_2 positive.)

Examples are:

If A = 1 (maximum output), then

$R_1/R_2 = \infty$ or $V(GS_R) = V_O-$; i.e., GS_R is tied to PWRO−

If A = ½, then

$R_1/R_2 = 2$

If A = ¼, (minimum output) then

$R_1/R_2 = 0$ or $V(GS_R) = V_O+$; i.e., GS_R is tied to PWRO+

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
V_{CC} and GRDD with Respect to V_{BB} .. −0.3V to 15V
All Input and Output Voltages with Respect to V_{BB} ..... −0.3V to 15V
All Input and Output Voltages with Respect to V_{CC} ..... −15V to +0.3V
Power Dissipation 1.35W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.) Typical values are for T_A = 25°C and nominal power supply values.

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	μA	GRDD ≤ V_{IN} ≤ V_{IL} (Note 1)
I_{IH}	High Level Input Current			10	μA	V_{IH} ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input Low Voltage, except CLKSEL	−0.3		0.8	V	(Note 2)
V_{IH}	Input High Voltage, except CLKSEL	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA at D_X, $\overline{TS}_X$ and SIG_R
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 80 μA at D_X, SIG_R
V_{ILO}	Input Low Voltage, CLKSEL(2)	V_{BB}		V_{BB} +0.5	V	
V_{IIO}	Input Intermediate Voltage, CLKSEL	GRDD −0.5		0.5	V	
V_{IHO}	Input High Voltage, CLKSEL	V_{CC} −0.5		V_{CC}	V	
C_{OX}	Digital Output Capacitance(3)		5		pF	
C_{IN}	Digital Input Capacitance		5	10	pF	

POWER DISSIPATION

All measurements made at f_{DCLK} = 2.048 MHz, outputs unloaded.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CCI}	V_{CC} Operating Current		6.6		mA	
I_{BBI}	V_{BB} Operating Current		−6.2		mA	
I_{CCO}	V_{CC} Power Down Current		0.5		mA	$\overline{PDN} \leq V_{IL}$
I_{BBO}	V_{BB} Power Down Current		−0.2		mA	$\overline{PDN} \leq V_{IL}$
I_{CCS}	V_{CC} Standby Current		0.5		mA	FS_X, $FS_R \leq V_{IL}$; after 600 μs
I_{BBS}	V_{BB} Standby Current		−0.2		mA	FS_X, $FS_R \leq V_{IL}$; after 600 μs
P_{DI}	Operating Power Dissipation(4)		64		mW	
P_{DO}	Power Down Dissipation(4)		3.5		mW	$\overline{PDN} \leq V_{IL}$
P_{ST}	Standby Power Dissipation(4)		3.5		mW	FS_X, $FS_R \leq V_{IL}$

NOTES:
1. V_{IN} is the voltage on any digital pin.
2. SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC}; they are also pinstraps for mode selection when tied to V_{BB}. Under these conditions V_{ILO} is the input low voltage requirement.
3. Timing parameters are guaranteed based on a 100 pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pF.
4. With nominal power supply values.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input Leakage Current, VF_XI+, VF_XI-			100	nA	$-2.17V \leq V_{IN} \leq 2.17V$
R_{IXI}	Input Resistance, VF_XI+, VF_XI-	10			MΩ	
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-			25	mV	
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	55			dB	$-2.17 \leq V_{IN} \leq 2.17V$
A_{VOL}	DC Open Loop Voltage Gain, GS_X	5000				
f_C	Open Loop Unity Gain Bandwidth, GS_X		0.4		MHz	
C_{LXI}	Load Capacitance, GS_X			50	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			KΩ	

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output Resistance, PWRO+, PWRO−		1		Ω	
V_{OSRA}	Single-Ended Output DC Offset, PWRO+ PWRO−		75	±150	mV	Relative to GRDA
C_{LRA}	Load Capacitance, PWRO+, PWRO−			100	pF	

A.C. CHARACTERISTICS—TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave.(1) Input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration.(2) All output levels are (sin x)/x corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response Tolerance	−0.18	±0.04	+0.18	dBm0	Signal input of 1.064 Vrms μ-law Signal input of 1.068 Vrms A-law T_A = 25°C, V_{BB} = −5V, V_{CC} = +5V
EmW_{TS}	EmW Variation with Temperature and Supplies	−0.07	±0.02	+0.07	dB	±5% supplies, 0 to 70°C Relative to nominal conditions
DmW	Digital Milliwatt Response Tolerance	−0.18	±0.04	+0.18	dBm0	Measure relative to $0TLP_R$. T_A = 25°C; V_{BB} = −5V, V_{CC} = +5V. R_L = ∞
DmW_{TS}	DmW Variation with Temperature and Supplies	−0.07	±0.02	+0.07	dB	±5% supplies, 0 to 70°C

NOTES:
1. 0 dBm0 is defined as the zero reference point of the channel under test (0TLP). This corresponds to an analog signal input of 1.064 volts rms or an output of 1.503 volts rms for μlaw. See Table 4.
2. Unity gain input amplifier: GS_X is connected to VF_XI-, Signal input VF_XI+; Maximum gain output amplifier; GS_R is connected to PWRO−, output to PWRO+.

GAIN TRACKING

Reference Level = −10 dBm0

Symbol	Parameter	Min	Max	Unit	Test Conditions
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input; μ-law		±0.25 ±0.5 ±1.2	dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input; A-law		±0.25 ±0.5 ±1.2	dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input; μ-law		±0.25 ±0.5 ±1.2	dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0 Measured at PWRO+, R_L = 300Ω
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input; A-law		±0.25 ±0.5 ±1.2	dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0 Measured at PWRO+, R_L = 300Ω

NOISE(All receive channel measurements are single ended)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
N_{XC1}	Transmit Noise, C-Message Weighted			15	dBrnc0	VF_XI+ = GRDA, VF_XI- = GS_X
N_{XC2}	Transmit Noise, C-Message Weighted with Eighth Bit Signaling			18	dBrnc0	VF_XI+ = GRDA, VF_XI- = GS_X; 6th frame signaling
N_{XP}	Transmit Noise, Psophometrically Weighted			−75	dBm0p	VF_XI+ = GRDA, VF_XI- = GS_X
N_{RC1}	Receive Noise, C-Message Weighted: Quiet Code			11	dBrnc0	D_R = 11111111
N_{RC2}	Receive Noise, C-Message Weighted: Sign bit toggle			12	dBrnc0	Input to D_R is Quiet code with sign bit toggle at 1 KHz rate
N_{RP}	Receive Noise, Psophometrically Weighted: Quiet Code			−79	dBm0p	D_R = 10101010
N_{SF}	Single Frequency Noise End to End Measurement			−50	dBm0	CCITT G.712.4.2 Measure at PWRO+
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit or Receive Channel		−35		dB	Idle channel; 200 mV P-P signal on V_{CC}; 0 to 50 KHz, measure at D_X
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit or Receive Channel		−35		dB	Idle channel; 200 mV P-P signal on V_{BB}; 0 to 50 KHz, measure at D_X
CT_{TR}	Crosstalk, Transmit to Receive			−71	dB	VF_XI+ = 0 dBm0, 1.02 KHz, D_R = Quiet code
CT_{RT}	Crosstalk, Receive to Transmit			−71	dB	D_R = 0 dBm0, 1.02 KHz, VF_XI+ = GRDA

DISTORTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$SD1_X$	Transmit Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.714-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_X$	Transmit Signal to Distortion, A-Law Sinusoidal Input; CCITT G.714-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD1_R$	Receive Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.714-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_R$	Receive Signal to Distortion, A-Law Sinusoidal Input; CCITT G.714-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
DP_X	Transmit Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
DP_R	Receive Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
IMD_1	Intermodulation Distortion, End to End Measurement			−35	dB	CCITT G.712 (7.1)
IMD_2	Intermodulation Distortion, End to End Measurement			−49	dBm0	CCITT G.712 (7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			−25	dBm0	CCITT G.712 (6.1)
SIS	Spurious in Band Signals, End to End Measurement			−40	dBm0	CCITT G.712 (9)
D_{AX}	Transmit Absolute Group Delay		220		μs	Fixed Data Rate, CLK_X = 2.048 MHz; 0 dBm0, 1.4 KHz signal at VF_XI+ Measure at D_X.
D_{DX}	Transmit Differential Group Delay Relative to D_{AX}		170 95 45 75		μs μs μs μs	f = 500 − 600 Hz f = 600 − 1000 Hz f = 1000 − 2600 Hz f = 2600 − 2800 Hz
D_{AR}	Receive Absolute Group Delay		140		μs	Fixed Data Rate, CLK_R = 2.048 MHz; 0dBm0, 0.3 KHz Measure at PWRO+.
D_{DR}	Receive Differential Group Delay Relative to D_{AR}		35 35 110 135		μs μs μs μs	f = 500 − 600 Hz f = 600 − 1000 Hz f = 1000 − 2600 Hz f = 2600 − 2800 Hz

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS

Input amplifier is set for unity gain, noninverting; maximum gain output.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02 KHz					0 dBm0 Signal input at VF_XI+
	16.67 Hz			−30	dB	
	50 Hz			−25	dB	
	60 Hz			−23	dB	
	200 Hz	−1.8		−0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.10	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−32	dB	

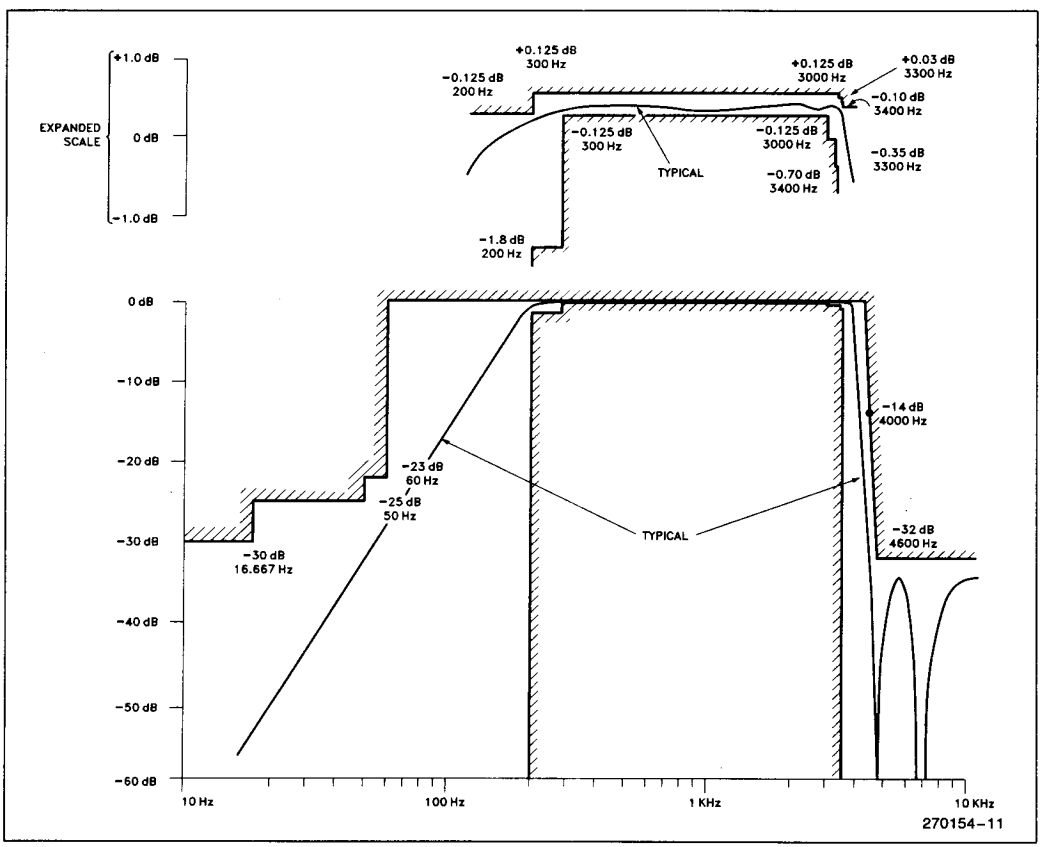


Figure 8. Transmit Voice Frequency Characteristics

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RR}	Gain Relative to Gain at 1.02 KHz					0 dBm0 Signal input at D_R
	Below 200 Hz			+0.125	dB	
	200 Hz	−0.5		+0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.1	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−30	dB	

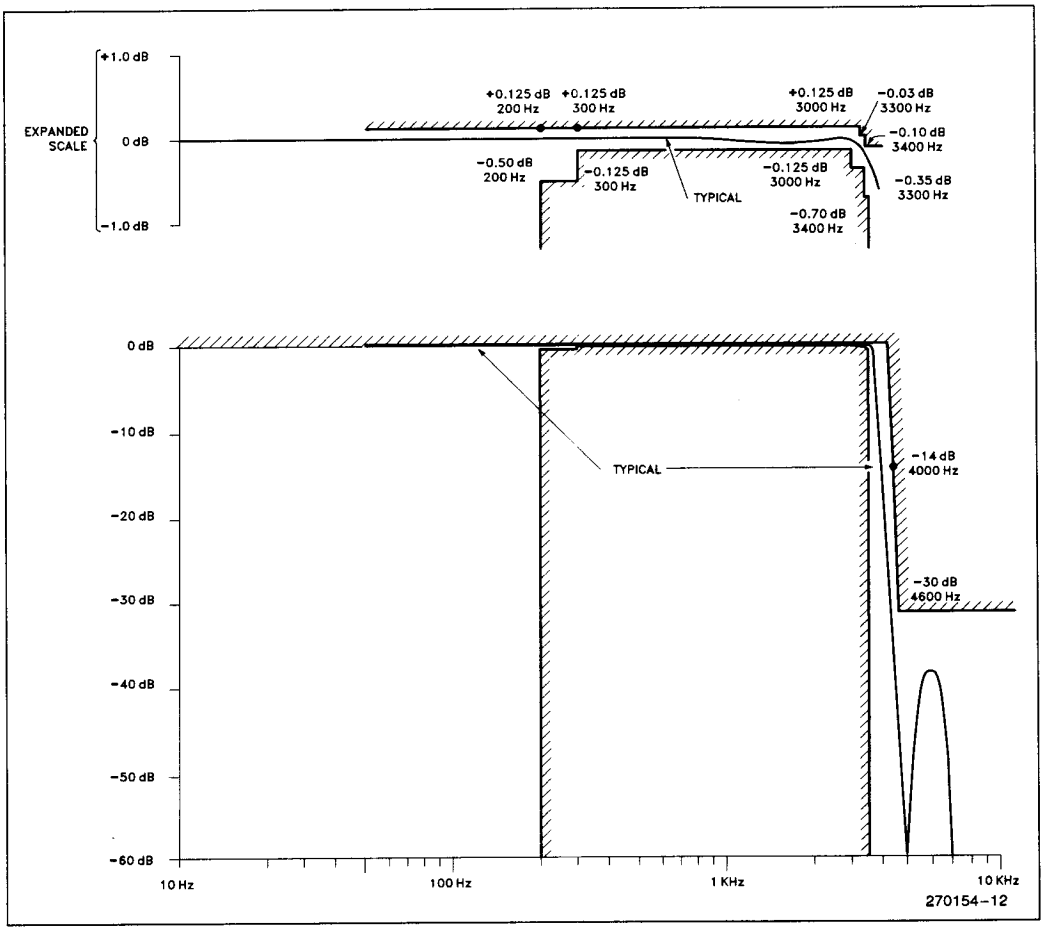


Figure 9. Receive Voice Frequency Characteristics

A.C. CHARACTERISTICS—TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CY}	Clock Period, CLK_X, CLK_R	488			ns	$f_{CLKX} = f_{CLKR} = 2.048$ MHz
t_{CLK}	Clock Pulse Width, CLK_X, CLK_R	220			ns	
t_{DCLK}	Data Clock Pulse Width	220			ns	64 KHz $\leq f_{DCLK} \leq$ 2.048 MHz
t_{CDC}	Clock Duty Cycle, CLK_X, CLK_R	45	50	55	%	
t_r, t_f	Clock Rise and Fall Time	5		30	ns	

TRANSMIT SECTION, FIXED DATA RATE MODE(1)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DZX}	Data Enabled on TS Entry	0		145	ns	$0 < C_{LOAD} < 100$ pF
t_{DDX}	Data Delay from CLK_X	0		145	ns	$0 < C_{LOAD} < 100$ pF
t_{HZX}	Data Float on TS Exit	60		215	ns	$C_{LOAD} = 0$
t_{SON}	Timeslot X to Enable	0		145	ns	$0 < C_{LOAD} < 100$ pF
t_{SOFF}	Timeslot X is Disable	60		215	ns	$0 < C_{LOAD}$
t_{FSD}	Frame Sync Delay	100		t_{CLK}	ns	
t_{SS}	Signal Setup Time	0			ns	
t_{SH}	Signal Hold Time	0			ns	

RECEIVE SECTION, FIXED DATA RATE MODE

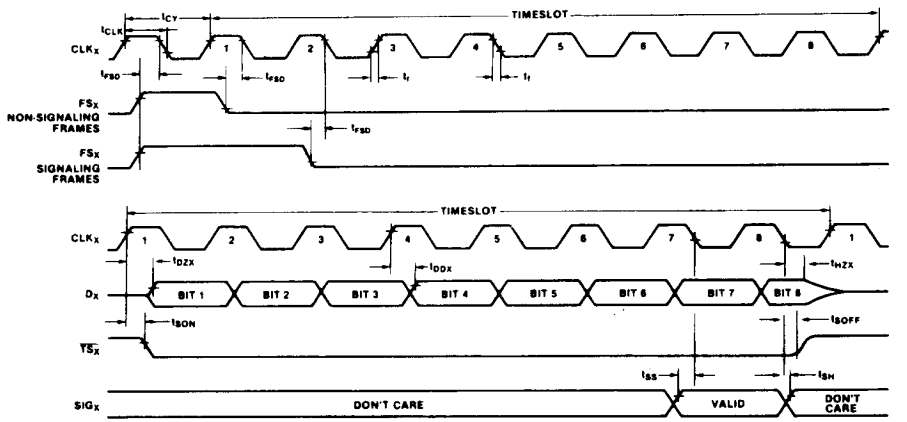
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DSR}	Receive Data Setup	10			ns	
t_{DHR}	Receive Data Hold	60			ns	
t_{FSD}	Frame Sync Delay	100		t_{CLK}	ns	
t_{SIGR}	SIG_R Update	0		2	μs	

NOTE:
1. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

WAVEFORMS

Fixed Data Rate Timing

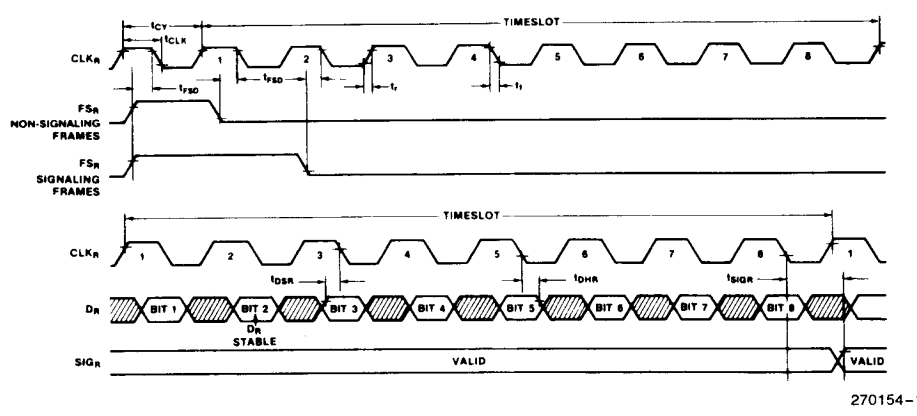
TRANSMIT TIMING



270154-13

NOTE:
All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF} and t_{HZX} which reference a high impedance state.

RECEIVE TIMING



270154-14

NOTE:
All timing parameters referenced to V_{IH} and V_{IL}.

TRANSMIT SECTION, VARIABLE DATA RATE MODE(1)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDX}	Timeslot Delay from $DCLK_X$(2)	140		$t_{DX}-140$	ns	
t_{FSD}	Frame Sync Delay	100		$t_{CY}-100$	ns	
t_{DDX}	Data Delay from $DCLK_X$	0		100	ns	$0 < C_{LOAD} < 100$ pF
t_{DON}	Timeslot to D_X Active	0		50	ns	$0 < C_{LOAD} < 100$ pF
t_{DOFF}	Timeslot to D_X Inactive	0		80	ns	$0 < C_{LOAD} < 100$ pF
t_{DX}	Data Clock Period	488		15620	ns	
t_{DFSX}	Data Delay from FS_X	0		140	ns	

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDR}	Timeslot Delay from $DCLK_R$(3)	140		$t_{DR}-140$	ns	
t_{FSD}	Frame Sync Delay	100		$t_{CY}-100$	ns	
t_{DSR}	Data Setup Time	10			ns	
t_{DHR}	Data Hold Time	60			ns	
t_{DR}	Data Clock Period	488		15620	ns	
t_{SER}	Timeslot End Receive Time	0			ns	

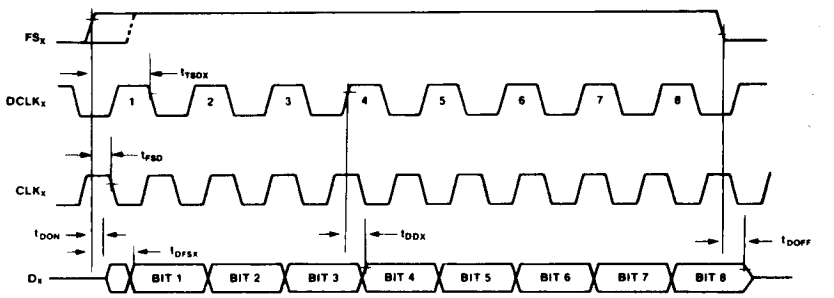
64 KB OPERATION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{FSLX}	Transmit Frame Sync Minimum Downtime	488			ns	FS_X is TTL high for remainder of frame
t_{FSLR}	Receive Frame Sync Minimum Downtime	488			ns	FS_R is TTL high for remainder of frame
t_{DCLK}	Data Clock Pulse Width			10	μs	

NOTES:
1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. t_{FSLX} minimum requirements overrides t_{TSDX} maximum spec for 64 KHz operation.
3. t_{FSLR} minimum requirements overrides t_{TSDR} maximum spec for 64 KHz operation.

VARIABLE DATA RATE TIMING

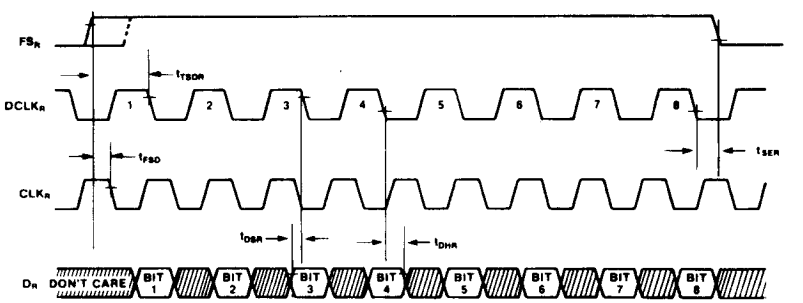
TRANSMIT TIMING



NOTE:
All timing parameters referenced to V_{IH} and V_{IL} except t_{DON} and t_{OFF} which reference a high impedance state.

270154-15

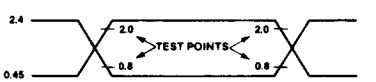
RECEIVE TIMING



NOTE:
All timing parameters referenced to V_{IH} and V_{IL} except t_{DON} and t_{OFF} which reference a high impedance state.

270154-16

A.C. TESTING INPUT, OUTPUT WAVEFORM



270154-17

A.C. Testing: Inputs Are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements Are Made at 2.0V for a Logic "1" and 0.8V for a Logic "0".