LSI/CSI

LS7501 thru LS7510

TONE ACTIVATED LINE ISOLATION DEVICE

FEATURES:

- Low power CMOS design
- On chip oscillator (32,768HZ external crystal required)
- Tone input can be low level sinusoid (as low as — 30 DBM) or fully digital.
- Mask programmable available frequencies: 11 HZ to 4095 HZ (in 1 HZ steps)
- Sample interval -4.5 seconds (Mask programmable 0.5 to 8.0 seconds).

CONNECTION DIAGRAM: TOP VIEW
STANDARD 16 PIN PLASTIC DIP

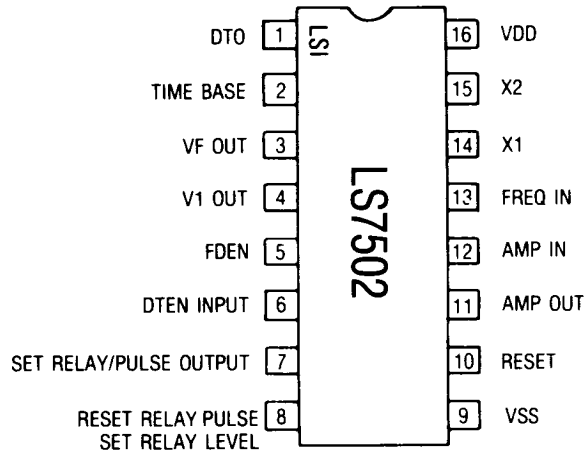


FIGURE 1

DESCRIPTION

The LS7501 — LS7510 are frequency discriminator circuits that respond to a standard frequency input if the input is maintained within ± 10HZ during a 4.5 second continuous sample interval. During this interval, the input is being sampled every 0.5 seconds. If it is valid for the sample interval, then the circuit can be used to pulse a relay that disconnects the line to be tested. After 20 seconds of disconnect time, the relay is reset and the line is restored. There are ten standard frequency versions of this circuit. These are indicated in table 1 with their associated input discriminator frequencies.

TABLE 1

PART NO.	FREQUENCY (HZ)
LS7501	2683
LS7502	2713
LS7503	2743
LS7504	2773
LS7505	2833
LS7506	2863
LS7507	2893
LS7508	2923
LS7509	2953
LS7510	2983

DETAILED DESCRIPTION

A. Input Amplifier:
The amplifier has a minimum gain of 40. The input should be a.c. coupled.

B. Frequency Discriminator:
The frequency input can be a digital source or the output of the amplifier. The input is sampled for a 1/2 second interval and if a proper frequency is present, the VF output goes high.

C. The sample interval timer is enabled when a valid frequency is detected. The purpose of the timer is to insure that the input frequency is continuous for a period of 4.5 seconds ± 125ms. If the applied input frequency is interrupted during the detection period, the timer is reset and a new detection interval is started. At the end of a valid sample period, a 125ms pulse is generated at VI.

D. Disconnect Timer:
Enabled by a positive edge on the DTEN input and clocked at a 2Hz rate, this timer determines the disconnect time. (20 ± .5 seconds). On timeout, a positive pulse is generated on DTO.

E. Clock Generator:
A 32,768 Hz crystal oscillator and a chain of binary dividers provide all the timing signals.

TABLE 2. INPUT, OUTPUT DESCRIPTION

PIN	FUNCTION	DESCRIPTION
1	DTO	Disconnect timer time out. Active high pulse generated at the end of disconnect time (20 sec); normally connected to Pin 5.
2	TIME BASE	Output clock 32,768 HZ or 8 HZ (Mask Programmable)
3	VF OUT	Valid frequency. Active high when input frequency is 2713 ± 10 HZ (LS7502).
4	VI OUT	125 MS Active high pulse output generated when an input frequency has been valid for the duration of the sample interval (4.5 seconds).
5	FDEN	Frequency detector enable (Positive edge triggered)
6	DTEN INPUT	Disconnect timer enable (Positive edge triggered) normally connected to VI out. It also disables frequency detection.
7	SET RELAY/ PULSE OUTPUT	3.9 ms active high pulse generated when a valid frequency has been present for 4.5 seconds.
8	RESET RELAY PULSE/ SET RELAY LEVEL	3.9 ms active high pulse generated when the disconnect timer times out or a high level that lasts for the duration of the 20 second time out. (Mask programmable). If the reset relay option is active, a pulse is generated on the RESET RELAY Output at power-up.
9	VSS	Ground
10	RESET	External reset. An active high pulse will reset circuit (Internal pull down).
11	AMP OUT	Amplified Tone. Usually connected to the FREQ pin.
12	AMP IN	Tone input for low level (to — 30 DBM) sinusoid.
13	FREQ IN	Digital tone input.
14	X1	Crystal
15	X2	Crystal
16	VDD	Positive Supply

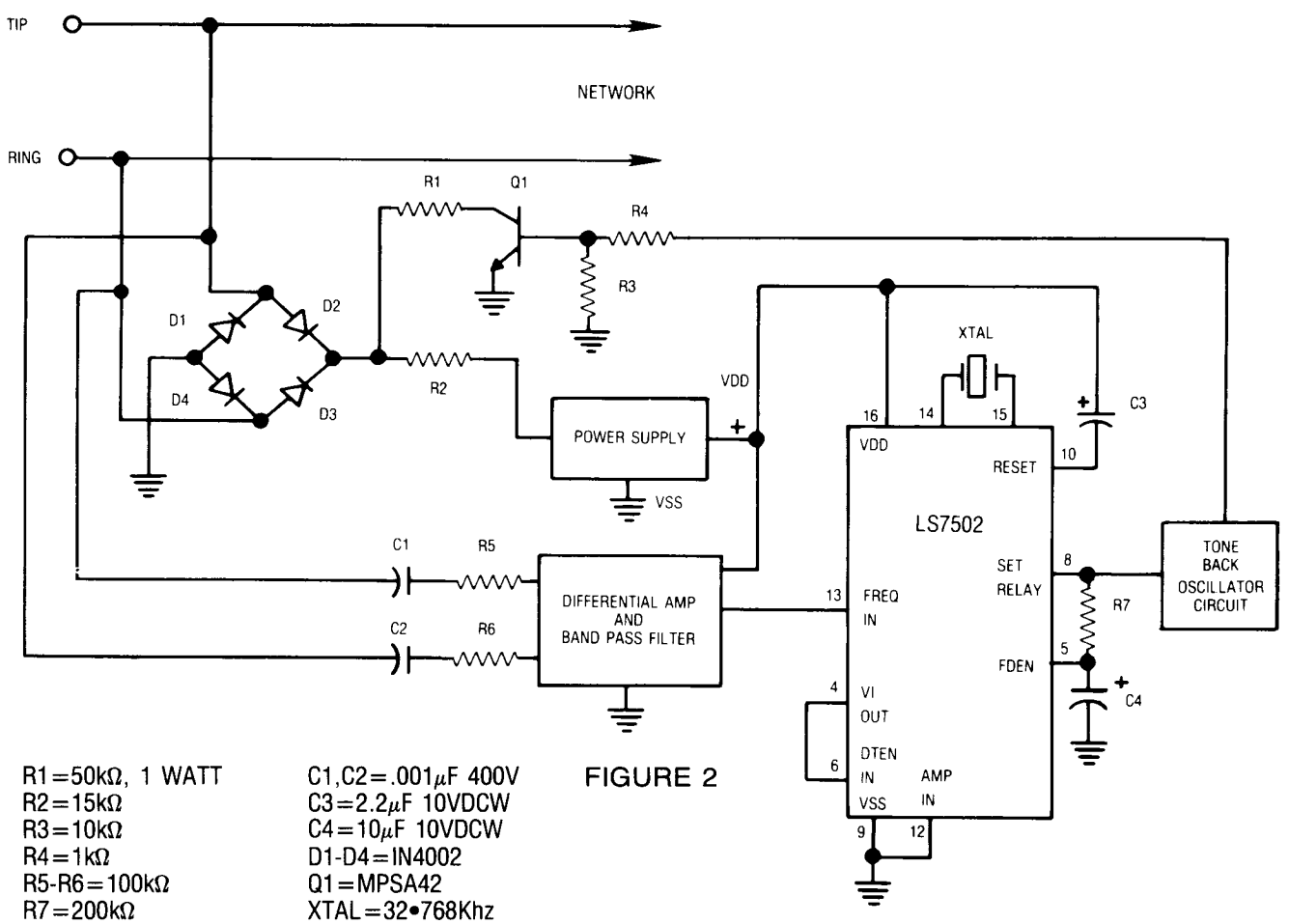
Maximum Ratings: (Voltages referenced to VSS)

RATING	SYMBOL	VALUE	UNIT
DC supply voltage	VDD	+2.5 to +6.0	Vdc
Operating temperature range	TA	-25 to +70	°C
Storage temperature range	TSTG	-65 to +150	°C

DC Electrical Characteristics:
(VSS = 0V, VDD = +2.5 to +6.0V, -25°C TA +70°C unless otherwise specified)

PARAMETER	CONDITIONS	VDD	MIN	MAX	UNITS
Output Source Current	V_0 = 0.7V	2.5V	100	—	μA
	V_0 = 0.7V	5.0V	1.0	—	ma
Output Sink Current	V_0 = 0.25V	2.5V	350	—	μA
	V_0 = 0.25V	5.0V	900		μA
Input Specifications (All Inputs)					
Vi_L (MAX)		2.5V	—	0.75	Volts
		5.0V	—	1.50	Volts
Vi_H (MIN)		2.5V	1.75	—	Volts
		5.0V	3.50	—	Volts
Noise Margins:		2.5 to 5.0V	1.0	—	Volts
Quiescent Device Current:		2.5V	—	20	μA
Note: Reset Input Contains Internal 100KΩ Pulldown.					
A.C. Specifications (All Outputs)					
T_{RISE}, T_{FALL}	CL = 50pf	5.0V	—	1.0	μsec

TELEPHONE LINE INTERROGATOR AND TONE BACK GENERATOR



R1=50kΩ, 1 WATT
R2=15kΩ
R3=10kΩ
R4=1kΩ
R5-R6=100kΩ
R7=200kΩ

C1,C2=.001μF 400V
C3=2.2μF 10VDCW
C4=10μF 10VDCW
D1-D4=IN4002
Q1=MPSA42
XTAL=32•768Khz

FIGURE 2

DESCRIPTION

This application indicates a method for interrogating a telephone line when a 2713Hz (±10Hz) tone is detected for a minimum of 4.5 seconds. (The LS7502 Circuit.)

At the end of the 4.5 second sample period, an oscillator is energized and generates a tone back signal. This signal modulates the line at a voice level of -16DB or 3.5MV peak to peak.

Typical system input activation sensitivity is -30DBM. The unit should also be operational down to 6 volts at the tip/ring network terminals.

As shown in Figure 2, the differential op-amp is connected to the telephone lines through .001μF coupling capacitors. This eliminates the D.C. component and acts as the first filter for 60Hz. The differential amplifier stage is followed by a band pass filter centered around 2713Hz. This filter should be designed for high Q's (Q=10) and yet utilize current efficient op-amps.

The band pass output is then squared up and connected to the digital tone input (Pin 13). The input signal, is sampled by the digital discrimination section of the LS7502. If 2713Hz (±10Hz) is present for 4.5 seconds, a 125 millisecond pulse at Pin 4 is applied to the DTEN input (Pin 6), causing an internal flip-flop to set an the set relay output (Pin 8) to go high, activating the tone back oscillator.

As the 10μF capacitor (C_4) builds up stored charge, it biases the FDEN input (Pin 5) through R_7 until it is sufficient to reset the internal flip-flop and bring the circuit back to its idle state and turn the tone back oscillator off. By varying the R_7-C_4 network, the time constant for the tone back duration can be varied.

CIRCUIT BLOCK DIAGRAM

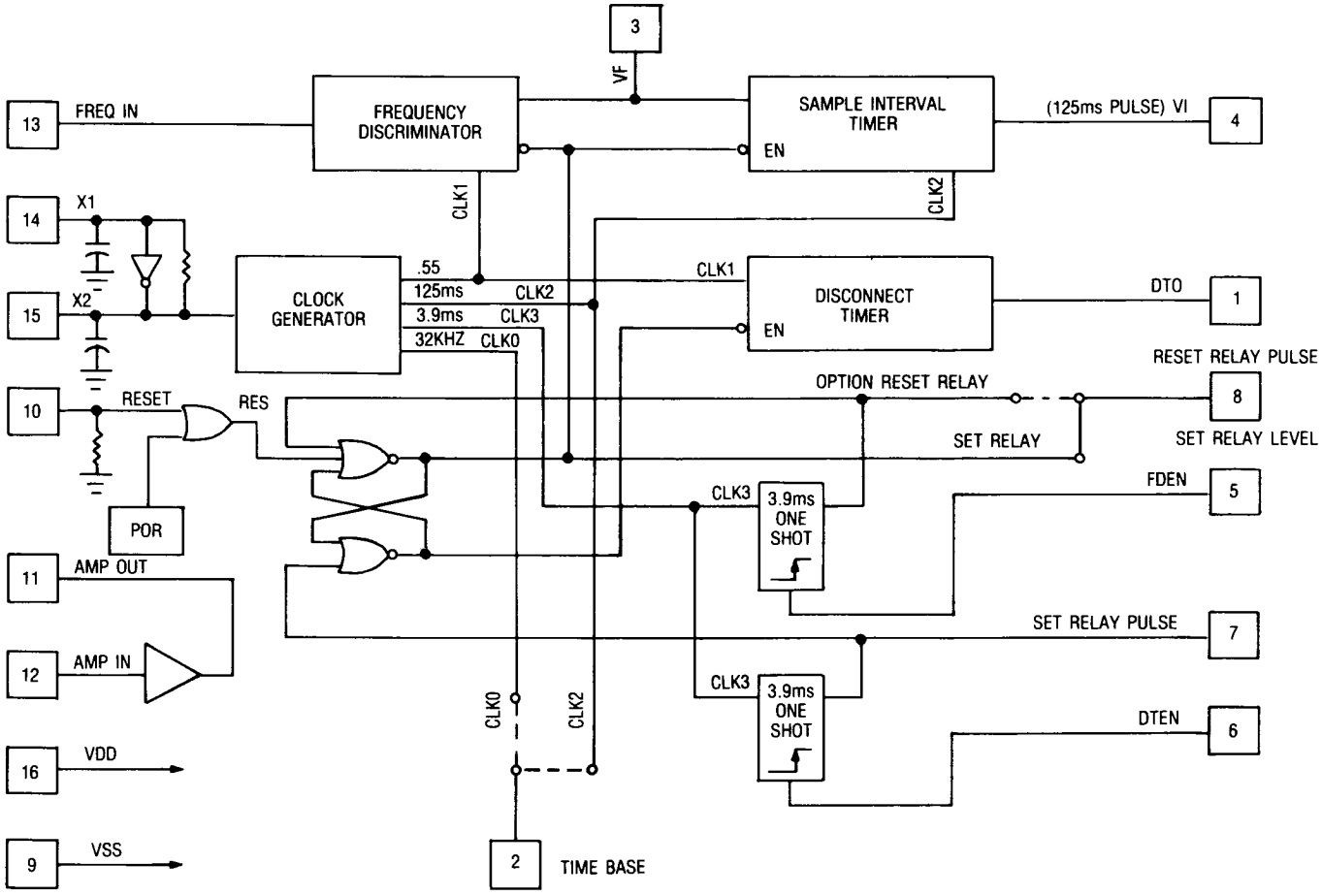


FIGURE 3

NOTE (1) All devices shown on the LS7501 through the LS7510 are configured with the set relay outpout on Pin 8. The reset option can be substituted by optional mask change.

NOTE (2) All devices shown with the exception of the LS7502 are configured with the clock-0, 32KHz output on Pin 2. The LS7502 is configured with the clock-2 time base output of 8Hz. These outputs may be changed with the same optional mask change referred to in Note 1.

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