

High Reliability Fast CMOS Gate Arrays

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FEATURES:

- Single & Dual Layer Metal
- Source/Drain Contacts Programmable
- All I/O's Guardbanded Against Latchup
- Radiation Tolerant to 1 Megarad
- Fast Toggle Rates—Fast enough to satisfy applications historically served by TTL and LSTTL.
- Low Power Consumption—Typically 20% of the power dissipated by a TTL IC
- High Packing Density
- Well Defined Logic Levels
- Wide Tolerance of Operation—Typically operate over a supply voltage range of 3 to 10 volts and from -55°C to $+125^{\circ}\text{C}$ with no change in operation except circuit delays
- Excellent Noise Immunity—45% of supply voltage
- Ease of Breadboarding
- Ease of Interface

ISO-5/ISO-3/ISO-2 GATE ARRAY DESCRIPTION

The ISO 2/3/5 series of silicon gate CMOS arrays are high performance families of eleven arrays each with complexity

ranging from 100 to 6000 equivalent gates and a maximum pin count ranging from 24 to 120.

The ISO series of gate arrays are manufactured using a proven silicon gate oxide isolated CMOS process with either a single layer or dual layer of metal interconnect and a contact layer, defining the logic function being implemented.

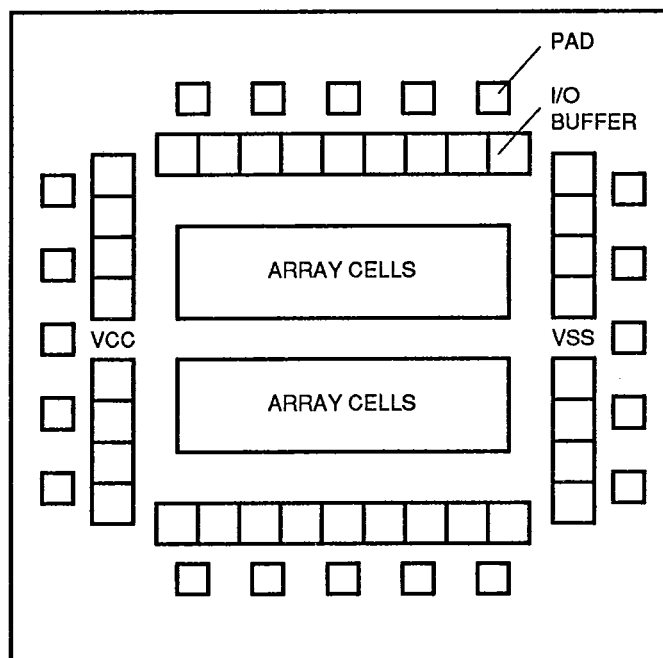
The circuits are organized as arrays of cells and I/O buffers as shown in Figure 1.

BASIC ARRAY CELL STRUCTURE

Each cell consists of three pairs of NMOS and PMOS transistors together with a poly underpass as shown in Figure 2. Note that each gate is common to adjacent N and P devices. Individual n-channel and p-channel transistors may be configured into a variety of SSI logic elements called macrocells, using predefined contacts and metal interconnections.

Note that each intersection point of the grid inside the diffusion boundary is a potential contact point for source or

FIGURE 1. CELL AND I/O ORGANIZATION





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drain which can be programmed as desired. Altogether there are six possible contact points for each source or drain and four contact options for each gate. There are fourteen possible initial routing paths per cell. Of these, two are normally taken by the power bus lines leaving 14 channels for macrocell and interconnect. Programmable contact is one of the unique features of our LSI silicon gate CMOS arrays which provides easy layout and maximum routing flexibility.

Figures 3 through 5 are some gate implementation examples.

INPUT/OUTPUT BUFFERS

The ISO series has very powerful I/O buffers designed to be direct TTL compatible, capable of sinking 6mA at 0.4V or 24mA at 2.5V ($V_{DD}=5.0V$), and sourcing 2mA at 4.6V or 10mA at 2.5V (for ISO 3 process).

There are three transistors (one single and one double) in each buffer device which can be connected as desired for any particular application. All the output devices are fully guardbanded.

FIGURE 2. BASIC CELL

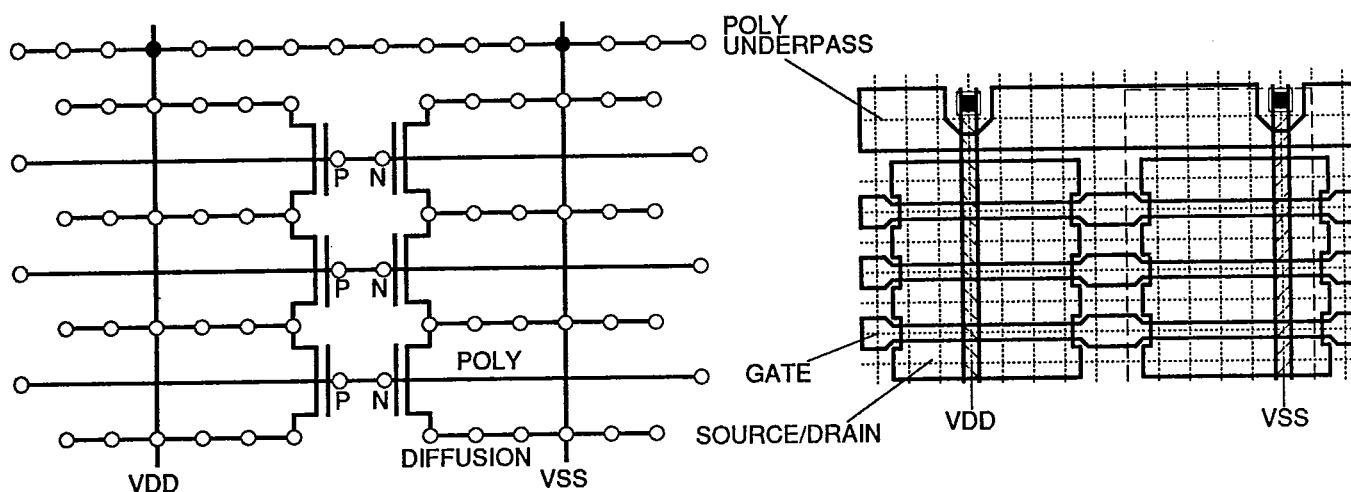
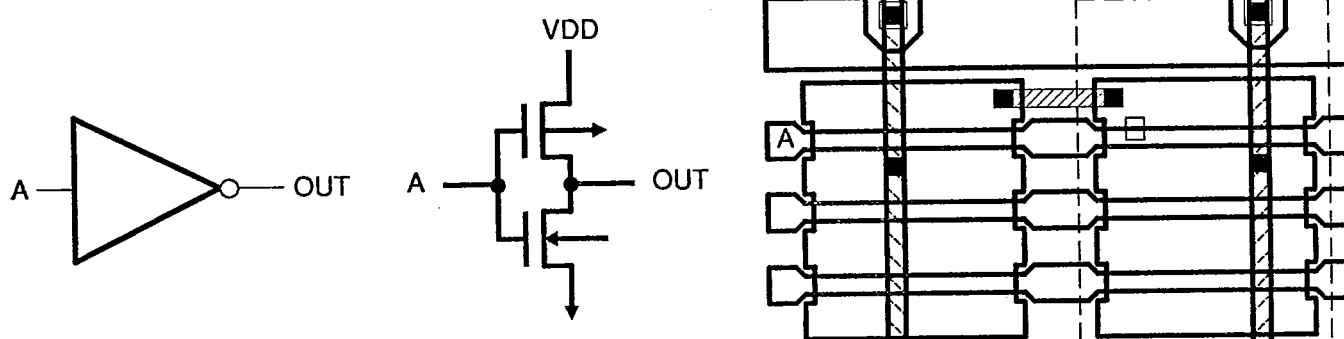


FIGURE 3. SINGLE INVERTER





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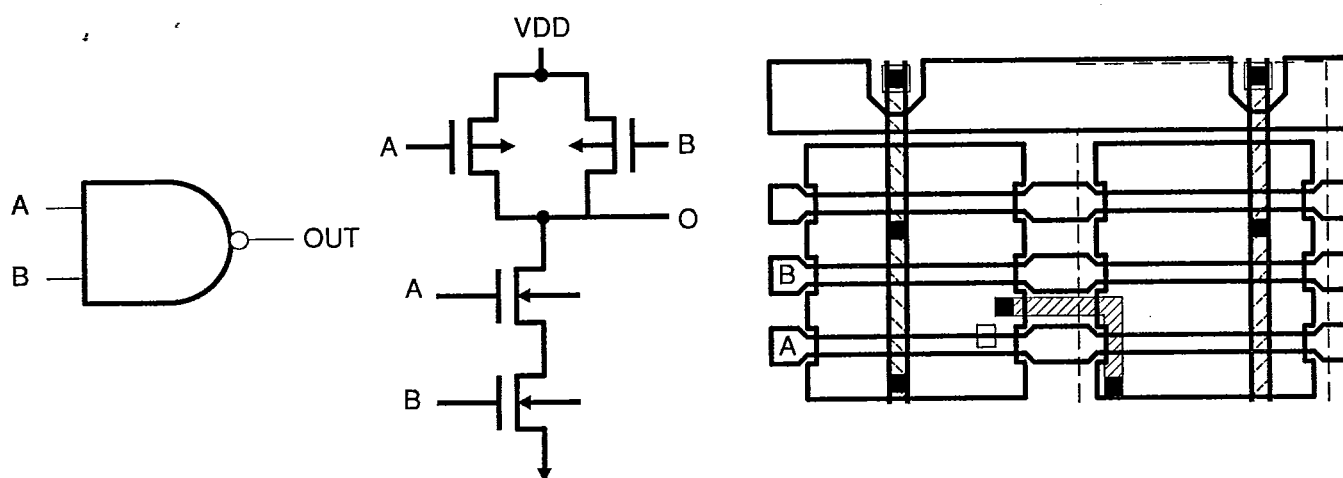
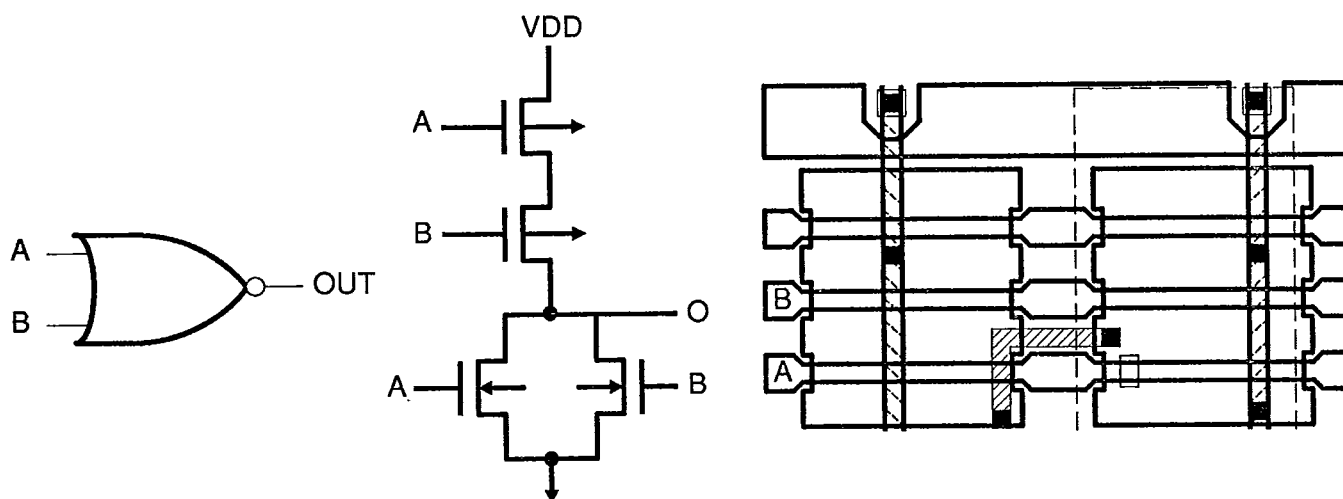
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I/O buffers can also be used as input protection devices. Figure 6 shows a typical implementation. This structure provides in excess of 2000V ESD (electrostatic discharge) protection.

The gate arrays are also protected against latch-up with over 100mA input injection current.

ISO 2/3/5 FAMILY

There are eleven ISO-CMOS arrays differing only in the size and number of cells. They are distinguished by the letters J, I, A, B, C, D, E, F, G, H and K, where J being the smallest and K being the largest and most complex. The internal arrays and peripheral devices are identical on all the circuits.

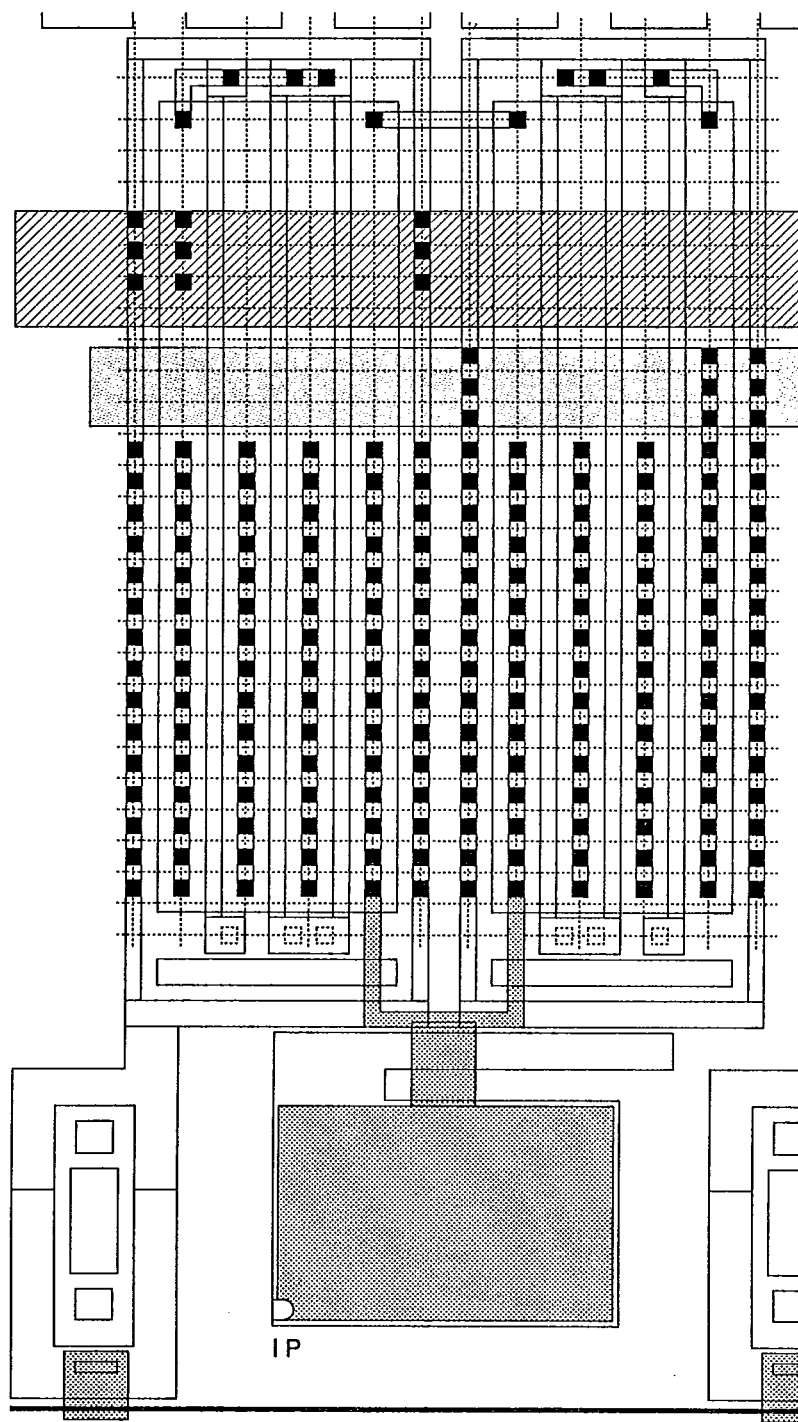
FIGURE 4. 2-INPUT NAND GATE**FIGURE 5. 2-INPUT NOR GATE**



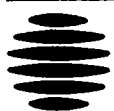
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FIGURE 6. INPUT PROTECTION DEVICE



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Every array in the family can be processed by three different technologies: ISO-5, ISO-3 and ISO-2. As the names imply, ISO-5, ISO-3 and ISO-2 designate 5, 3 and 2 micron gate length respectively.

Table 1 shows the ISO 2/3/5 family of fast Si-gate CMOS gate arrays their cell count and number of gate equivalents, pads and I/O buffers.

TABLE 1.

DESIGNATION	TOTAL CELLS	GATE EQUIVALENT	I/O BUFFER	PAD
ARRAY J	66	100	18	24
ARRAY I	120	180	36	46
ARRAY A	240	360	36	46
ARRAY B	360	540	48	58
ARRAY C	480	720	54	64
ARRAY D	640	960	62	72
ARRAY E	800	1200	68	78
ARRAY F	1000	1500	76	86
ARRAY G	1200	1800	82	92
ARRAY H	1600	2400	90	100
ARRAY K	4000	6000	110	120

DEVICE GEOMETRIES AND PARASITIC CAPACITANCE

The vital statistics of the ISO 2/3/5 active devices are given below (Tables 2, 3 and 4).

The underpasses used throughout the gate arrays are highly doped poly of varying sizes and lengths. A typical underpass (as used in the core of the array) resistance is 200 ohms and its parasitic capacitance about .12 Pf. The exact resistance and capacitance can be computed from the poly resistivity and field capacitance parameters give in Table 9. In most cases the underpasses contribute negligible delays and can be ignored.

TABLE 2. DEVICE CHANNEL CHARACTERISTICS OF ISO-5

CHANNEL TYPE	CHANNEL DIMENSION			GATE CAPACITANCE
	W _{eff}	L _{eff}	W/L	
N-channel array	53μ	3.5μ	15	.23 pf
N-channel buffer	850μ	3.5μ	243	3.70 pf
P-channel array	53μ	3.5μ	15	.23 pf
P-channel buffer	850μ	3.5μ	243	3.70 pf

TABLE 3. DEVICE CHANNEL CHARACTERISTICS OF ISO-3

CHANNEL TYPE	CHANNEL DIMENSION			GATE CAPACITANCE
	W _{eff}	L _{eff}	W/L	
N-channel array	53μ	2.0μ	22.5	.16 pf
N-channel buffer	850μ	2.0μ	425	2.50 pf
P-channel array	53μ	2.0μ	22.5	.16 pf
P-channel buffer	850μ	2.0μ	425	2.50 pf

TABLE 4. DEVICE CHANNEL CHARACTERISTICS OF ISO-2

CHANNEL TYPE	CHANNEL DIMENSION			GATE CAPACITANCE
	W _{eff}	L _{eff}	W/L	
N-channel array	53μ	1.5μ	35	.16 pf
N-channel buffer	850μ	1.5μ	566	2.50 pf
P-channel array	53μ	1.5μ	37	.16 pf
P-channel buffer	850μ	1.5μ	604	2.50 pf

CIRCUIT PERFORMANCE

Actual performance of each design will depend on the layout and normal manufacturing process variations. Our ISO-5 CMOS arrays can provide you with up to 15MHz speed and ISO-3 CMOS arrays can handle up to 30MHz and ISO-2 arrays will operate at 40 MHz.

Typical gate delays for some of the ISO 2/3/5 gates are presented in Tables 5, 6 and 7 respectively. T_r and T_f are typical output rise and fall delays. T_{pd} is the average delay.

TABLE 5.

ISO-5 FAMILY OF ARRAYS Typical Gate Delays (ns) F.O.=2			
GATE TYPE	T _r	T _f	T _{pd}
Inverter	2.7	1.7	2.2
2-Input NAND	3.2	2.4	2.8
2-Input NOR	5.6	2.7	3.7
3-Input NAND	3.7	3.6	3.6
3-Input NOR	9.4	1.9	7.8
4-Input NAND	4.2	5.2	4.7

TABLE 6.

ISO-3 FAMILY OF ARRAYS Typical Gate Delays (ns) F.O.=2			
GATE TYPE	T _r	T _f	T _{pd}
Inverter	1.4	1.1	1.2
2-Input NAND	1.6	1.6	1.6
2-Input NOR	2.2	1.2	1.7
3-Input NAND	1.7	2.3	2.0
3-Input NOR	3.6	1.3	2.5
4-Input NAND	2.0	3.1	2.5

TABLE 7.

ISO-2 FAMILY OF ARRAYS Typical Gate Delays (ns) F.O.=2			
GATE TYPE	T _r	T _f	T _{pd}
Inverter	.8	.7	.7
2-Input NAND	.9	.9	.9
2-Input NOR	1.3	.7	1.0
3-Input NAND	1.2	1.6	1.4
3-Input NOR	2.3	.8	1.6
4-Input NAND	1.4	2.2	1.8



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TABLE 8. DC CHARACTERISTICS (at $V_{DD}=5V$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{dd}	Quiescent Current		.1	10	μA	All Inputs = 0 or VDD
V_{ih}	Input High Voltage	3.5			V	CMOS Interface
		2.4			V	TTL Interface
V_{il}	Input Low Voltage			1.5	V	CMOS Interface
				0.6	V	TTL Interface
I_{in}	Input Current	- 10	.001	10	μA	$V_{in} = 0$ to VDD
V_{oh}	High Level Output Voltage (CMOS)	4.95			V	$ I_o < 1\mu A$
V_{ol}	Low Level Output Voltage (CMOS)			0.05	V	$ I_o < 1\mu A$
I_{ol}	Output Low (SINK) Current	5	8		mA	$V_o = 0.5V$ (ISO3)
		3	6		mA	$V_o = 0.5V$ (ISO5)
I_{oh}	Output High (SOURCE) Current	5	8		mA	$V_o = 2.4V$ (ISO3)
		3	6		mA	$V_o = 2.4V$ (ISO5)
I_{oz}	Three State Output Leakage Current	- 10	.001	10	μA	$V_o = 0$ or VDD
C_{in}	Any Input			7	Pf	

ABSOLUTE MAXIMUM RATINGSOperating Power Supply Range (V_{DD}):

for ISO-5: 3.0 to 15.0V

for ISO-3: 3.0 to 8.0V

for ISO-2: 3.0 to 8.0V

Operating Temperature Range -55°C to +125°C

Storage Temperature Range -55°C to +150°C

Input Voltage at any pin $V_{SS} - 0.3$ to $V_{DD} + 0.3$

Lead Temperature (soldering 10 sec) 200°C

Radiation 1×10^4 RADS*

Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

*RAD Hard Gate Array available up to 1×10^6 RADS.**PACKAGING**

Table 10 lists the typical plastic packages available for the ISO 2/3/5 family of arrays.

Ceramic packages are also available for the sizes listed above, although the cavity size may be slightly different than the leadframe pad size listed.

Other standard package options are listed below.

CATEGORY	PIN COUNT
Ceramic Leadless Chip Carrier	24 to 100
Flat Packs	24 to 84
Pin Grid Arrays	64 to 120
Chip Carriers	20 to 84

Custom Tooling is available to accommodate specialized package requirements.



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TABLE 9. ELECTRICAL PARAMETERS

PARAMETER	P-CHANNEL			N-CHANNEL			UNIT	CONDITION
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Threshold Voltage 2 Micron Process	0.6	0.9	0.6	0.6	0.9	1.2	Volts	IDS = 1 μ A W/L = 55/2
3 Micron Process	0.6	0.9	1.2	0.6	0.9	1.2		IDS = 1 μ A W/L = 55/3
5 Micron Process	0.7	1.0	1.4	0.6	0.9	1.2		IDS = 1 μ A W/L = 55/5
Conduction Factor K' = μ Co Non-Saturation	12	15	18	25	30	35	μ A/Volt ²	VDS = 0.1V
Polysilicon Over Field Oxide Threshold Voltage	15			15			Volts	ID = 1 μ A VB = 0V
Junction Breakdown Voltage	12 15			12 15			Volts	2 μ /3 μ Process 5 μ Process
Gate Oxide Capacitance		6.2×10^{-4}			6.2×10^{-4}		pf/ μ m ²	550 Å
Polysilicon Over Intermediate Field Oxide Capacitance		4.2×10^{-5}			4.2×10^{-5}		pf/ μ m ²	8000 Å Field Oxide
Al Over Field Oxide Capacitance		2.3×10^{-5}			2.3×10^{-5}		pf/ μ m ²	15000 Å Field Oxide
Sidways Field		1			1		μ m	
Substrate Resistivity P-Well Sheet Resistance		4 (5 μ)			—		ohm-cm	Substrate
		0.7 (3 μ)			—		ohm-sq	Substrate
		—			3000		ohm-sq	Well Region
Diffusion Sheet Resistance	25	50	90	10	15	25	ohm/sq	5 μ Process
	25	50	90	15	20	40	ohm/sq	3 μ Process
Polysilicon Sheet Resistance	10	20	30	10	20	30	ohm/sq	Same for Poly 1 & Poly 2
Junction Depth		0.5			0.4		μ m	2 μ Process
		0.8			1.0			3 μ Process
		1.0			1.5			5 μ Process
P-Well Depth		—			5.5		μ m	
Al Sheet Resistance		.02			.02		ohm/sq	
Junction Capacitance		3.0×10^{-4}			5×10^{-4}		pf/ μ m ²	2 μ Process
		2.6×10^{-4}			3.2×10^{-4}			3 μ Process
		1.2×10^{-4}			3.2×10^{-4}			5 μ Process

NOTE: All numbers are expressed as absolute values.



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TABLE 10.

NO. PINS	PACKAGE TYPE	PACKAGE WIDTH	LEADFRAME PAD PAD SIZE (mils)	100 J	180 I	360 A	540 B	720 C	960 D	1200 E	1500 F	1800 G	2400 H	6000 K
16	DUAL IN-LINE	300	150 x 200	yes	yes	no	no	no	no	no	no	no	no	no
18	DUAL IN-LINE	300	150 x 200	yes	yes	no	no	no	no	no	no	no	no	no
20	DUAL IN-LINE	300	160 x 230	yes	yes	no	no	no	no	no	no	no	no	no
22	DUAL IN-LINE	400	220 x 230	yes	yes	yes	yes	no	no	no	no	no	no	no
24	DUAL IN-LINE	300 600	160 x 210 180 x 220 250 x 270	yes	yes	yes yes	yes yes	yes		yes	yes	yes	yes	no
28	DUAL IN-LINE	600	200 x 220 260 x 260	no	yes	yes	yes	yes		yes	yes	yes	yes	no
40	DUAL IN-LINE	600	180 x 180 210 x 230 260 x 266	no	no	yes	yes	yes		yes	yes	yes	yes	no
48	DUAL IN-LINE	600	250 x 250 310 x 310	no	no	yes	yes	yes	yes	yes	yes	yes	yes	no
68	DUAL IN-LINE	900	310 x 310 410 x 410	no	no	no	no	yes	yes	yes	yes	yes	yes	no
28	QUAD	490	180 x 180	yes	yes	yes	yes	yes	no	no	no	no	no	no
44	QUAD	690	260 x 260	no	no	yes	yes	yes	yes	yes	yes	yes	no	no
68	QUAD	990	300 x 300 410 x 410	no	no	no	no	no	yes	yes	yes	yes	yes	no
84	QUAD	1190	390 x 390	no	no	no	no	no	yes	yes	yes	yes	yes	yes



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