

DESCRIPTION

The HY51V18164B is the new generation and fast dynamic RAM organized 1,048,576 × 16-bit. The HY51V18164B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY51V18164B to be packaged in standard 42/42 pin plastic SOJ, 44/50 pin TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 3.3V±10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
Max. CMOS standby 1.1mW (SL-part)
3.6mW
Max. TTL standby 7.2mW
Max. operating

Speed	Power
60	540mW
70	468mW
80	432mW

- Single power supply of 3.3V±10%
- TTL compatible inputs and outputs
- Fast access and cycle time

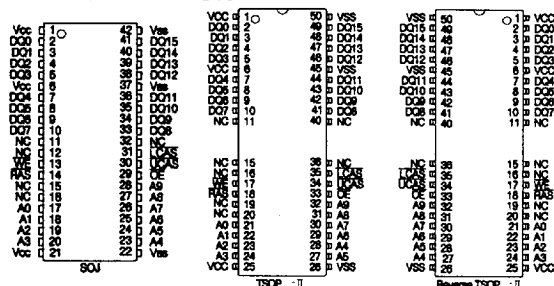
Speed	t _{RAC}	t _{CAC}	t _{HPC}
60	60ns	17ns	25ns
70	70ns	20ns	30ns
80	80ns	20ns	35ns

- Extended Data Out operation
- 2CAS Inputs for upper and lower byte control
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self refresh capability
- 1024 refresh cycles /256ms (SL-part)
- 1024 refresh cycles /16ms

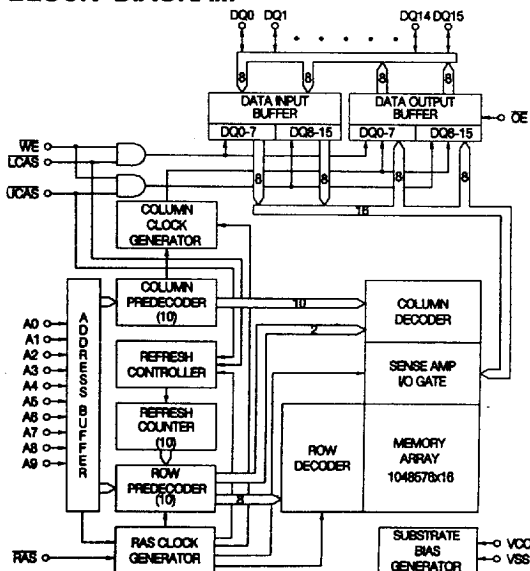
PIN DESCRIPTION

RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0 - A9	Address Input
DQ0 - DQ15	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 4.6	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 4.6	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	0.70	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	3.0	3.3	3.6	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.0	-	Vcc+0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

NOTE: All Voltage are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=3.3V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ VCC+1.0, All other pins not under test = VSS		-10	10	μA	
ILO	Output Leakage Current (High impedance State)	VSS ≤ VOUT ≤ VCC RAS & CAS at VIH		-10	10	μA	
ICC1	Vcc Supply Current, Operating	trc = trc (min.)	60 70 80	- - -	170 150 130	mA	1,2,3
ICC2	Vcc Supply Current, TTL Standby	RAS & CAS at VIH (min.), other Inputs ≥ VSS	SL-part	-	2 1	mA	
ICC3	Vcc Supply Current, RAS-only refresh	trc = trc (min.)	60 70 80	- - -	170 150 130	mA	1,3
ICC4	Vcc Supply Current, EDO mode	thpc = thpc (min.)	60 70 80	- - -	140 120 100	mA	1,2,3
ICC5	Vcc Supply Current, CMOS Standby	RAS & CAS ≥ Vcc-0.2V	SL-part	-	1 200	mA μA	5
ICC6	Vcc Supply Current, CAS-before- RAS refresh	trc = trc (min.)	60 70 80	- - -	170 150 130	mA	1
ICC7	Vcc Supply Current, Battery Back up (SL-part only)	trc = 250μs, CAS = CBR cycling or 0.2V OE & WE = Vcc-0.2V or 0.2V, A0-A9 = Vcc-0.2V or 0.2V, DQ0-DQ15 = -0.2V, VCC-0.2V or open	trAS ≤ 300ns trAS ≤ 1μs	- - -	350 450	μA	4,5
ICC8	Vcc Supply Current, Self Refresh (SL-Part only)	RAS & CAS ≤ 0.2V other pins same as ICC7		-	350	μA	5
VOL	Output Low Voltage	IOL = 2.0mA		-	0.4	V	
VOH	Output High Voltage	IOH = -2.0mA		2.4	-	V	

NOTE:

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
2. ICC1, ICC3, ICC4 and ICC6 are depend on output loading. Specified values are obtained with the output open.
3. ICC is specified as an average current. ICC1, ICC3, ICC6, Address can be changed maximum two times while RAS=VIL. ICC4, Address can be changed maximum once while CAS=VIH.
4. Only trAS(max.)=1μs is applied to refresh of battery backup but trAS(max.)=10μs is applied to normal functional operation.
5. ICC5(max.)=200μA, ICC7 and ICC8 are applied to SL-parts only.

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER		HY51V18164BJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
				-60		-70		-80			
				MIN	MAX	MIN	MAX	MIN	MAX		
1	tRC	Random Read or Write Cycle Time		105	-	125	-	145	-	ns	
2	tRWC	Read-Modify-Write Cycle Time		142	-	167	-	187	-	ns	
3	tHPC	EDO Mode Cycle Time		25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time		73	-	85	-	100	-	ns	
5	tRAC	Access Time from RAS		-	60	-	70	-	80	ns	8,9,10
6	tCAC	Access Time from CAS		-	17	-	20	-	20	ns	8,9
7	tAA	Access Time from Column Address		-	30	-	35	-	40	ns	8,10
8	tCPA	Access Time from CAS Precharge		-	35	-	35	-	40	ns	8,15
9	tCLZ	CAS to Output Low Impedance		0	-	0	-	0	-	ns	8
10	tOFF	Output Buffer Turn-off Delay from CAS		0	15	0	15	0	15	ns	11
11	tT	Transition Time (Rise and Fall)		2.5	50	2.5	50	2.5	50	ns	6
12	tRP	RAS Precharge Time		40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width		60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (EDO Mode)		60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time		13	-	15	-	20	-	ns	
16	tCSH	CAS Hold Time		40	-	50	-	60	-	ns	
17	tCAS	CAS Pulse width		13	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay		20	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time		15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time		5	-	5	-	5	-	ns	15
21	tCP	CAS Precharge Time		7	-	10	-	10	-	ns	20
22	tASR	Row Address Set-up Time		0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold time		10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time		0	-	0	-	0	-	ns	15
25	tCAH	Column Address Hold Time		15	-	15	-	15	-	ns	15
26	tRAL	Column Address to RAS Lead Time		30	-	35	-	40	-	ns	
27	tRCS	Read Command Set-up Time		0	-	0	-	0	-	ns	15
28	tRCH	Read Command Hold Time Referenced to CAS		0	-	0	-	0	-	ns	13,15
29	tRRH	Read Command Hold Time Referenced to RAS		0	-	0	-	0	-	ns	15
30	tWCH	Write Command Hold Time		10	-	15	-	15	-	ns	15
31	tWP	Write Command Pulse Width		10	-	10	-	10	-	ns	
32	tRWL	Write Command to RAS Lead Time		15	-	15	-	15	-	ns	
33	tCWL	Write Command to CAS Lead Time		13	-	15	-	20	-	ns	22
34	tDS	Data-in Set-up Time		0	-	0	-	0	-	ns	15,25
35	tDH	Data-in Hold Time		10	-	15	-	15	-	ns	15,25
36	tREF	Refresh Period (1024)		-	16	-	16	-	16	ms	18
		SL-Part		-	256	-	256	-	256	ms	
37	tWCS	Write Command Set-up Time		0	-	0	-	0	-	ns	15,16
38	tCWD	CAS to WE Delay Time		37	-	45	-	45	-	ns	16,21
39	tRWD	RAS to WE Delay Time		80	-	95	-	105	-	ns	16
40	tAWD	Column Address to WE Delay Time		50	-	60	-	65	-	ns	16

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY51V18164BJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-60		-70		-80			
			MIN	MAX	MIN	MAX	MIN	MAX		
41	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	15,23
42	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15,24
43	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	15
44	tCPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	20
45	tROH	RAS Hold Time Referenced to OE	10	-	10	-	10	-	ns	
46	tOEA	OE Access Time	-	17	-	20	-	20	ns	
47	tOED	OE to Data Delay	15	-	20	-	20	-	ns	
48	tOEZ	Output Buffer Turn Off Delay Time	0	15	0	15	0	15	ns	11
49	tOEH	OE Command Hold Time	15	-	20	-	20	-	ns	
50	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	16
51	tRHCP	RAS Hold Time from CAS Precharge	40	-	40	-	50	-	ns	
52	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
53	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
54	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	μs	
55	tRPS	RAS Precharge Time (Self Refresh Cycle)	110	-	130	-	150	-	ns	
56	tCHS	CAS Hold Time (Self Refresh Cycle)	50	-	50	-	50	-	ns	
57	tDOH	Output Data Hold Time	3	-	3	-	3	-	ns	
58	tREZ	Output Buffer Turn Off Delay Time from RAS	0	15	0	15	0	15	ns	
59	tWEZ	Output Buffer Turn Off Delay Time from WE	0	15	0	15	0	15	ns	
60	tWED	WE to Data Delay Time	15	-	15	-	15	-	ns	
61	tOEP	OE High Pulse Width	10	-	10	-	10	-	ns	
62	tWPE	WE Pulse Width (EDO Cycle)	10	-	10	-	10	-	ns	
63	tOCH	OE to CAS Hold Time	0	-	0	-	0	-	ns	
64	tCHO	CAS Hold Time to OE	5	-	5	-	5	-	ns	

NOTE:

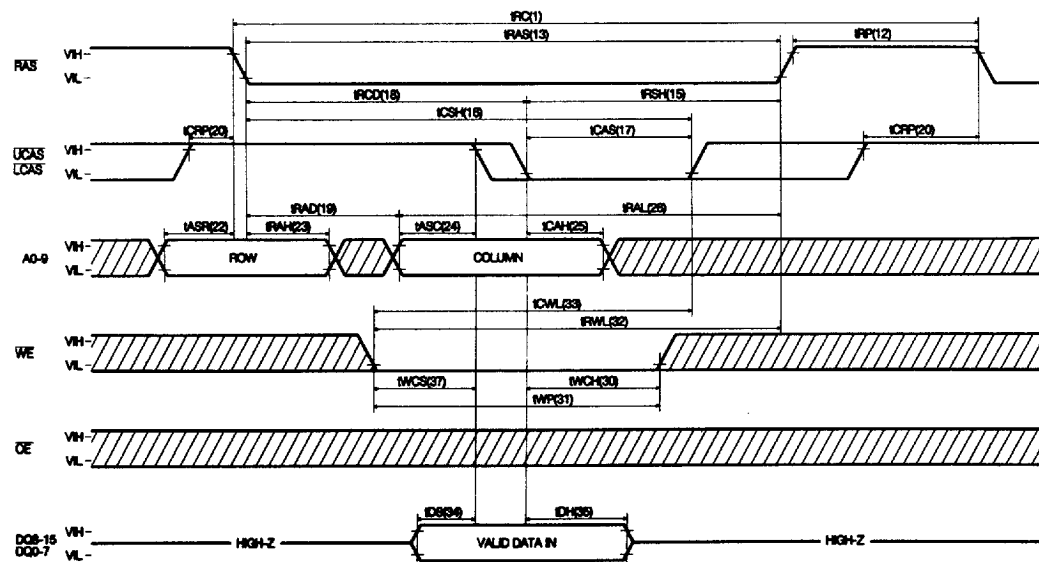
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages referenced to Vss.
3. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles are required.
4. Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$. In case of changed once or less during a EDO mode cycle (thPC).
5. AC measurements assume $t_r 2.5\text{ns}$.
6. $\text{VIH}(\text{min.})$ and $\text{VIL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL .
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_A = 0$ to 70°C) is assured.
8. Measured at $\text{VOH}=2.0\text{V}$ and $\text{VOL}=0.8\text{V}$ with a load equivalent to 1TTL load and 100pF.
9. Operation within the $\text{trCD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met.
 $\text{trCD}(\text{max.})$ is specified as a reference point only. If trCD is greater than the specified $\text{trCD}(\text{max.})$ limit, then access time is controlled by tCAC .
10. Operation within the $\text{trAD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met.
 $\text{trAD}(\text{max.})$ is specified as a reference point only. If trAD is greater than the specified $\text{trAD}(\text{max.})$ limit, then access time is controlled by tAA .
11. $\text{tOFF}(\text{max.})$, $\text{tREZ}(\text{max.})$, $\text{tWEZ}(\text{max.})$ and $\text{tOEZ}(\text{max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. The tCRP requirement should be applicable for $\overline{\text{RAS}} / \overline{\text{CAS}}$ cycles preceded by any cycle.
13. Either trCH or trRH must be satisfied for a read cycle.
14. Parameter tWP is applicable for a late write cycle. For early write cycle, tWCH must be met.
15. These parameters are referenced to $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
16. twCS , trWD , tcWD , tAWD , and tcpWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $\text{twCS} \geq \text{twCS}(\text{min.})$, the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) through the entire cycle. If $\text{trWD} \geq \text{trWD}(\text{min.})$, $\text{tcWD} \geq \text{tcWD}(\text{min.})$, $\text{tAWD} \geq \text{tAWD}(\text{min.})$, and $\text{tcpWD} \geq \text{tcpWD}(\text{min.})$ (Hyper Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of condition of the data out (at access time) is interminated.
17. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
18. 1024 cycles of Burst Refresh must be executed within 16ms after exiting Self Refresh.
19. tASC , tCAH are reference to the earlier $\overline{\text{CAS}}$ falling edge.
20. tCP and tCPT are measured when both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ are high state.
21. tcWD is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
22. tcWL must be satisfied by both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ for 16-bits access cycles.
23. tCSR is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
24. tCHR is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.
25. tDS , tDH is independently specified for lower byte $\text{DQ}(0-7)$, upper byte $\text{DQ}(8-15)$.

CAPACITANCE

(TA=25°C, Vcc=3.3V $\pm$ 10%, Vss=0V, f=1MHz, unless otherwise noted.)

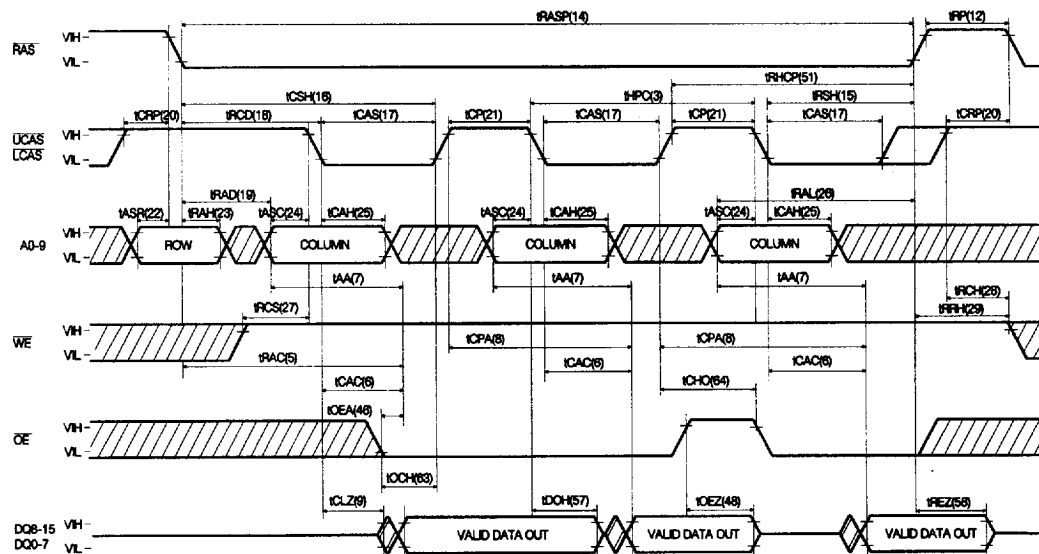
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	5	pF
CIN2	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ15)	-	7	pF

READ CYCLE

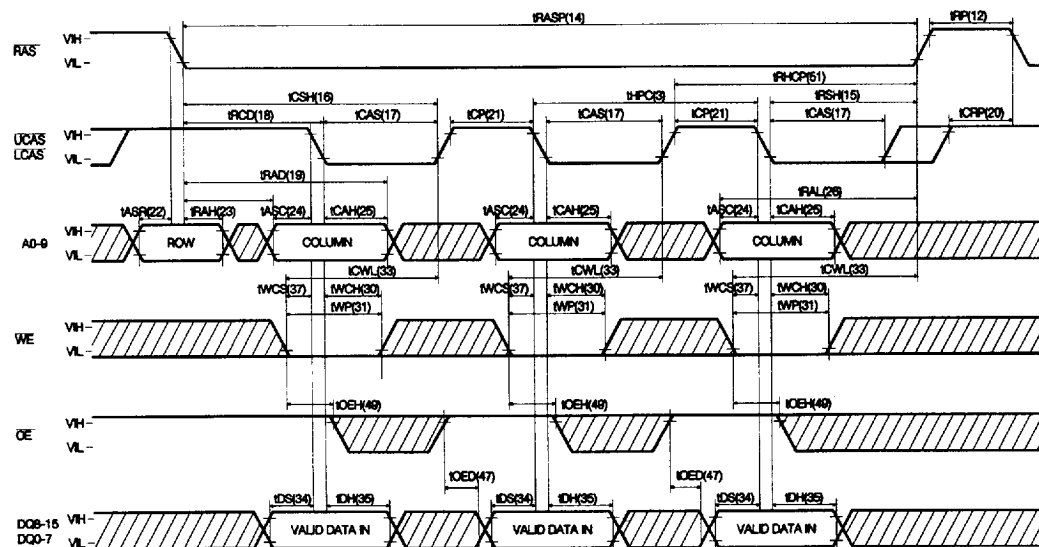


The timing diagram illustrates the sequence of signals for the 64160 device. The signals shown are RAS, UCAS, AD[9], WE, OE, and DOB[15:DOO[7]. The diagram includes various timing parameters such as t_{RAS} , t_{RCD} , t_{RSH} , t_{ICP} , t_{RAD} , t_{IAR} , t_{IAS} , t_{ICAH} , t_{FAL} , t_{ICSD} , t_{ICWD} , t_{ICWL} , t_{IAC} , t_{ICLZ} , t_{IOED} , t_{IOE2} , t_{IS3} , and t_{IDH} . The diagram also shows the valid data out and valid data in periods.

EDO MODE READ CYCLE



EDO MODE EARLY WRITE CYCLE



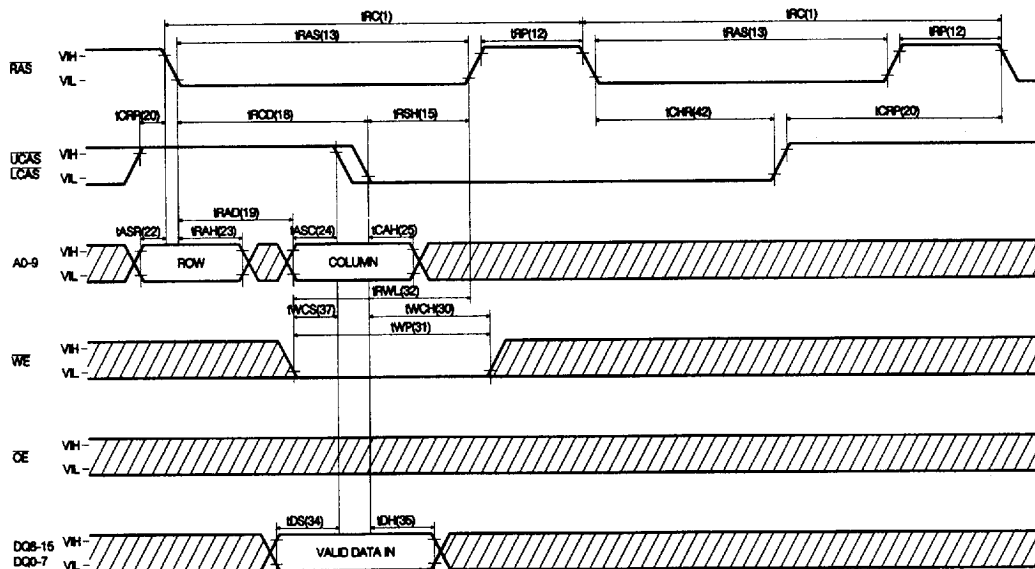
[illegible]

Timing diagram for the 74VHC04-10. The diagram shows the relationship between RAS, UCAS, WE, and DOB-15/DOB-7 signals. RAS has a high pulse with timing parameters $t_{PR}(12)$, $t_{RAS}(13)$, $t_{PO}(1)$, and $t_{RP}(12)$. UCAS has a high pulse with timing parameters $t_{PC}(13)$, $t_{CPR}(41)$, and $t_{CHP}(42)$. WE is a high pulse with timing parameter $t_{CEZ}(10)$. DOB-15 and DOB-7 are shown as a single signal with a high pulse. A note indicates that AO-9 and OE are 'H' or 'L'.

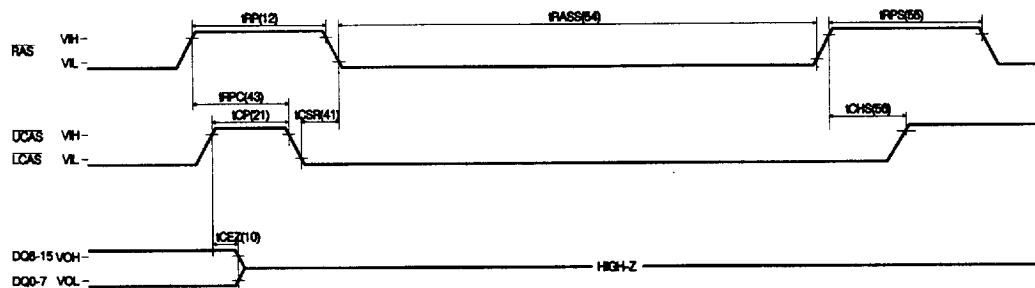
The timing diagram illustrates the relationship between various control and data signals for the 64160 device. The signals and their timing parameters are as follows:

- RAS:** Row Address Strobe. Timing parameters include $t_{RAS}(13)$, $t_{RC}(1)$, $t_{RP}(12)$, $t_{RAS}(13)$, and $t_{RP}(12)$.
- UCAS/LCAS:** Column Address Strobe/Latch Enable. Timing parameters include $t_{ICPP}(20)$, $t_{ICD}(18)$, $t_{RSH}(15)$, $t_{ICHR}(42)$, and $t_{ICPP}(20)$.
- A0-9:** Address lines. Timing parameters include $t_{ASR}(22)$, $t_{RAD}(19)$, $t_{RAH}(23)$, $t_{ASQ}(24)$, $t_{RAL}(26)$, and $t_{CAH}(29)$.
- WE:** Write Enable. Timing parameters include $t_{RCS}(27)$, $t_{RRH}(29)$, and $t_{AA}(7)$.
- OE:** Output Enable. Timing parameters include $t_{CAC}(8)$, $t_{IOEA}(48)$, $t_{RAC}(5)$, $t_{ICLZ}(9)$, $t_{IOEZ}(51)$, and $t_{IOFF}(19)$.
- Data Bus:** Signals D08-15 (VOH) and D00-7 (VOL). The diagram shows a period of **VALID DATA OUT** and a transition to **HIGH-Z**.

HIDDEN REFRESH CYCLE (WRITE)

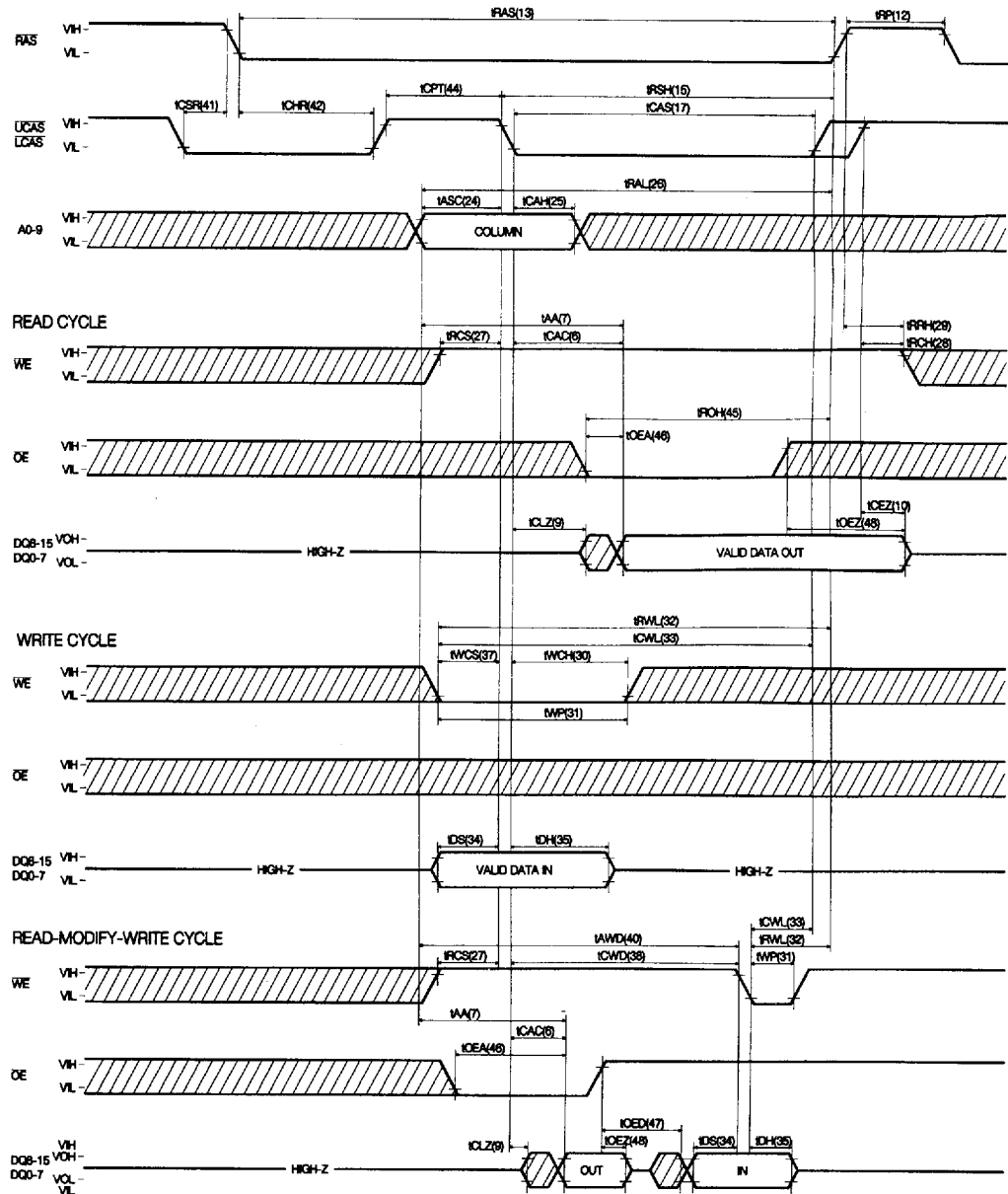


CAS-BEFORE-RAS SELF REFRESH CYCLE



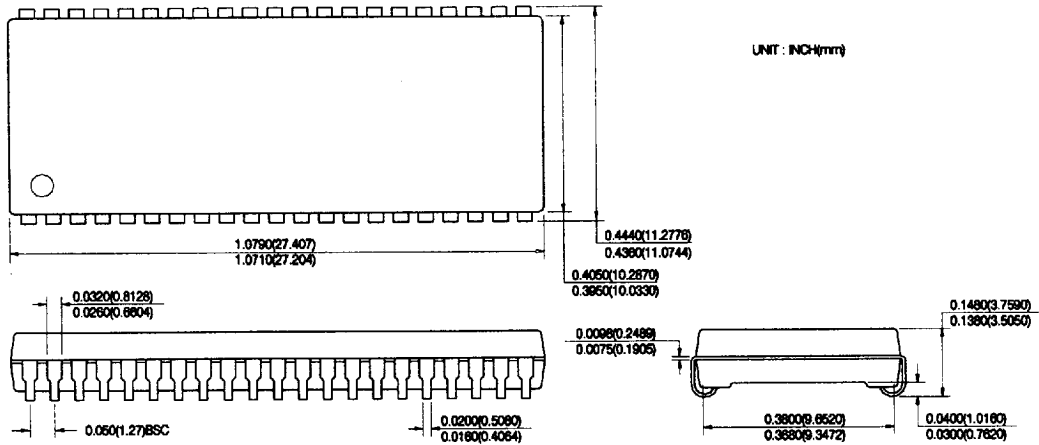
NOTE: A0-9, OE and WE = "H" or "L"

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

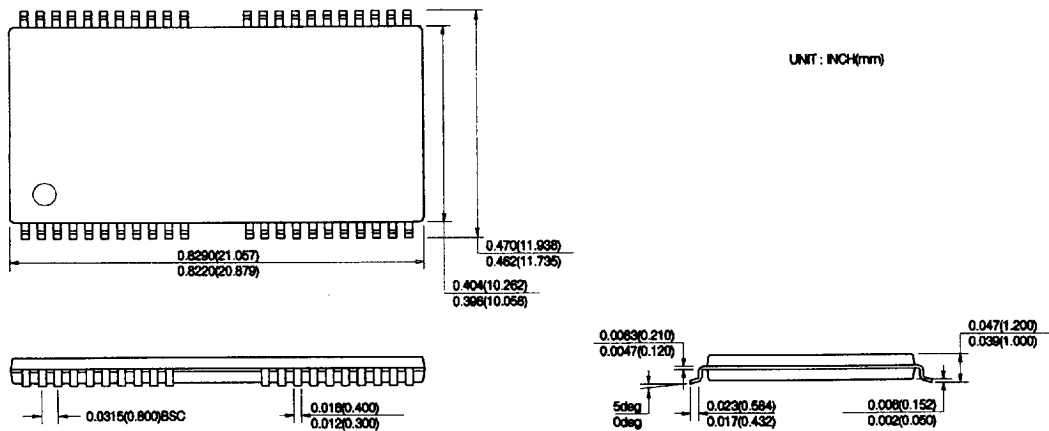


PACKAGE INFORMATION

400 mil 42/42 pin Small Outline J-form Package (JC)



400 mil 44/50 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NO	SOEED	POWER	PACKAGE
HY51V18164BJC	60/70/80		SOJ
HY51V18164BSLJC	60/70/80	SL-part	SOJ
HY51V18164BTC	60/70/80		TSOP-II
HY51V18164BSLTC	60/70/80	SL-part	TSOP-II
HY51V18164BRC	60/70/80		TSOP-II(R)
HY51V18164BSLRC	60/70/80	SL-part	TSOP-II(R)