NEC

# Application Note

# USAGE OF μPC1663, DC to VHF WIDEBAND DIFFERENTIAL INPUT AND OUTPUT AMPLIFIER IC

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**The information in this document will be updated without notice.**

This document outlines a typical application of this product, that is, provides an example for designing concept of an external circuit directly required for this product. NEC only assures the quality and characteristics of this product specified in the Data Sheet, and is not responsible for any user's product designs or application sets.

The peripheral circuit shown in this document is just an example prepared for evaluating the operations of this product, and does not imply that the circuit configurations or constants are recommended values or regulations. In addition, these circuits are not intended for any mass-produced application sets. This is because the analog characteristics vary depending on the external parts used, mounting patterns, and other conditions.

For this reason, customers are responsible for designing external circuits according to user-designed system requirements by referring this document, and should also confirm the characteristics of their application circuit before use.



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## CONTENTS

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## 1. GENERAL

The μPC1663 is a differential input, differential output wideband amplifier IC that uses a high-frequency ($f_T$ = 6 GHz) silicon bipolar process (called NESAT™ 1). This process improves bandwidth, phase characteristics, input noise voltage characteristics, and low power consumption compared to conventional HF-band differential amplifier ICs.

These features make this device suitable as a wideband amplifier in high-definition TVs, high-resolution monitors, broadcasting satellite receivers, and video cameras, as a sense amplifier in high-density CCD and optical pick-up products, or as a pulse amplifier for optical data links.

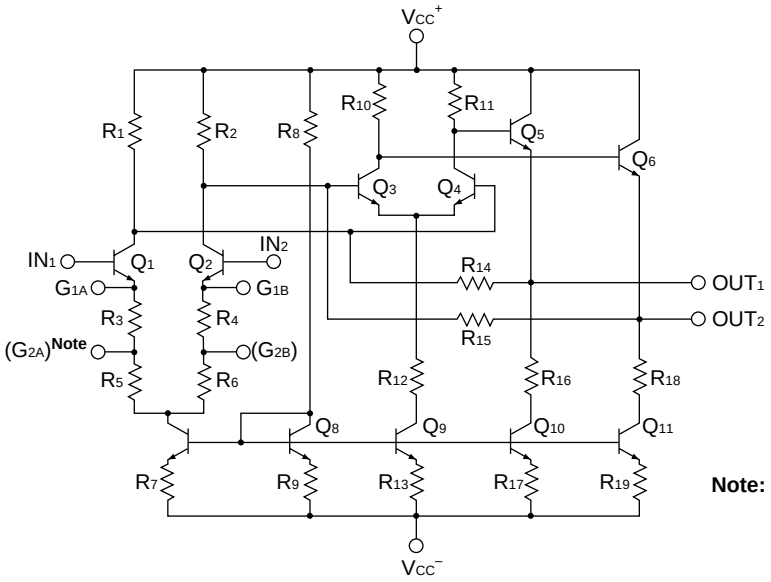
Note, however, that this device's wide frequency range means that extra caution is required with regard to factors such as oscillation.

This application note describes how to use the μPC1663 and its application circuits.

## 2. BASIC OPERATIONS

### 2.1 Outline of Operations

**Figure 1. Internal Equivalent Circuit**




| | | | |
|---|---|---|---|
| $R_1$ | 2.4 kΩ | $R_{11}$ | 1.1 kΩ |
| $R_2$ | 2.4 kΩ | $R_{12}$ | 750 Ω |
| $R_3$ | 50 Ω | $R_{13}$ | 300 Ω |
| $R_4$ | 50 Ω | $R_{14}$ | 7 kΩ |
| $R_5$ | 590 Ω | $R_{15}$ | 7 kΩ |
| $R_6$ | 590 Ω | $R_{16}$ | 1.2 kΩ |
| $R_7$ | 600 Ω | $R_{17}$ | 400 Ω |
| $R_8$ | 10 kΩ | $R_{18}$ | 1.2 kΩ |
| $R_9$ | 1.4 kΩ | $R_{19}$ | 400 Ω |
| $R_{10}$ | 1.1 kΩ | | |

**Note:** The μPC1664, which included $G_{2A}$ and $G_{2B}$ pins, has been discontinued.

Figure 1 shows an internal equivalent circuit diagram of the μPC1663. It is a DC direct-coupled amplifier in which two emitter-followers for transistors $Q_5$ and $Q_6$ are added to the two-stage differential configuration and in which feedback is propagated from the output via $R_{14}$ and $R_{15}$.

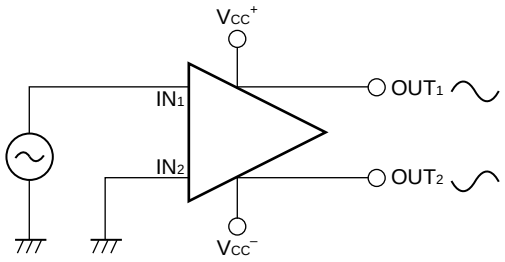
Since $OUT_1$ and $OUT_2$ are differential outputs, the output voltage changes to the reverse direction at precisely double the gain (single-end) of differential voltage $\Delta V_{DIF}$ added between the differential inputs $IN_1$ and $IN_2$. $OUT_1$ operates in phase with $IN_1$ and $OUT_2$ operates in phase with $IN_2$, so that, for example:

When $IN_1 > IN_2$, $OUT_1$ changes to positive and $OUT_2$ changes to negative

When $IN_1 < IN_2$, $OUT_1$ changes to negative and $OUT_2$ changes to positive

Accordingly, as is shown in Figure 2, if a sine wave is input to $IN_1$ when $IN_2$ is used as a ground, a sine wave having the same phase as the $IN_1$ input is output via $OUT_1$ and a sine wave having a 180° inverted phase is output via $OUT_2$.

**Figure 2. Response to Sine Wave Input**




**Remark** For purposes of simplification, the bypass capacitor and gain select pin have been omitted in some figures, such as Figure 2.

## 2.2 Determination of Gain

Given $r_{e1}$ and $r_{e2}$ as the resistance values corresponding to the input differential transistors $Q_1$ and $Q_2$, the gain can be approximated via the following equations.

Gain $A_{VD1}$ for $IN_1$ and $OUT_1$

$$A_{VD1} \doteqdot \frac{R_{14}}{r_{e1} + R_3 + R_5} \quad \text{.....(1)}$$

Gain $A_{VD2}$ for $IN_2$ and $OUT_2$

$$A_{VD2} \doteqdot \frac{R_{15}}{r_{e2} + R_4 + R_6} \quad \text{.....(2)}$$

Consequently, assuming that $\Delta V_{DIF} = V_{IN1} - V_{IN2}$ as the differential voltage between $IN_1$ and $IN_2$, the output voltage can be calculated as follows.

$$|\Delta OUT_1| = \frac{|\Delta V_{DIF}|}{2} \bullet A_{VD1} \text{.....(3)}$$

$$|\Delta OUT_2| = \frac{|\Delta V_{DIF}|}{2} \bullet A_{VD2} \text{.....(4)}$$

Since $A_{VD1} = A_{VD2}$, we can add equations (3) and (4) to obtain the following.

$$A_{VD1} = \frac{|\Delta OUT_1| + |\Delta OUT_2|}{|\Delta V_{DIF}|} \text{.....(5)}$$

In equations (3), (4), and (5), $A_{VD1}$ ($A_{VD2}$) represents the differential output gain corresponding to the differential input voltage. Therefore, the differential voltage gain and $A_{VD1}/2$ ($A_{VD2}/2$) are defined as single-end voltage gain since it represents only one-sided output corresponding to the differential input voltage.

## 2.3 Gain Adjustments

The gain values shown in equations (1) and (2) in section 2.2 above are determined according to the resistance applied to the emitter side of input differential transistors $Q_1$ and $Q_2$.

Accordingly, in the equivalent circuit shown in Figure 1, a short between gain select pins $G_{1A}$ and $G_{1B}$ or insertion of an adjusting resistor can be used to adjust the gain in steps.

Setting a short between $G_{1A}$ and $G_{1B}$ sets maximum gain, with a typical value of 320 times the differential gain. Setting an open connection between $G_{1A}$ and $G_{1B}$ sets minimum gain, with a typical value of 10 times the differential gain. The electrical characteristics for the two gain select pin conditions, when Gain 1 is the maximum gain and Gain 2 is the minimum gain, are shown in Table 3.

If a gain adjusting resistor is inserted between $G_{1A}$ and $G_{1B}$ (as shown in Figure 4), any desired gain level can be obtained. Depending on the application circuit, if the Rs value is changed, the input voltage amplitude appears like it fluctuates due to changes in the interstage impedance, but the gain of the IC itself does not vary.

**Figure 3. Pin Configuration of μPC1663 (Top View)**

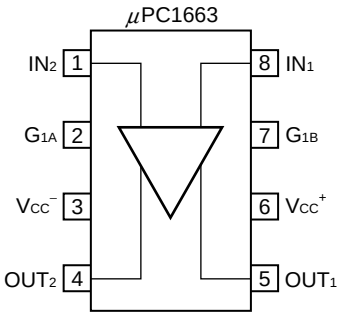
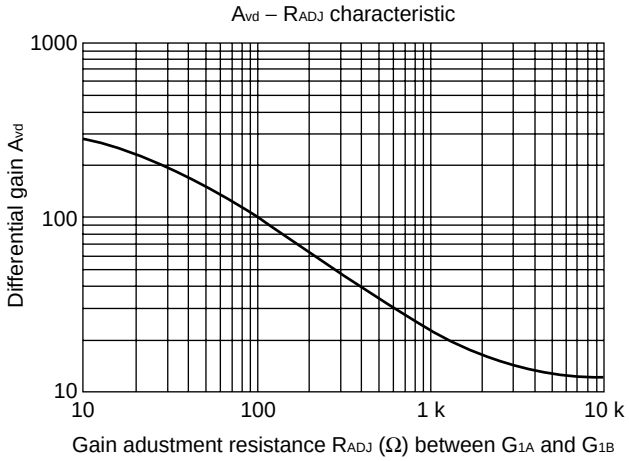



**Figure 4. Differential Voltage Gain vs. Gain Adjustment Resistance Characteristics**




## 3. ELECTRICAL CHARACTERISTICS

The absolute maximum ratings are listed in Table 1, recommended operating conditions in Table 2, and electrical characteristics in Table 3. Due to limitations that depend on the package, the supply voltage and temperature range differ slightly. The electrical characteristics are identical, however, because the same chip is employed.

**Table 1. Absolute Maximum Ratings**

| Parameter | Symbol | Condition | μPC1663C | μPC1663G | μPC1663GV | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}^{\pm}$ | $T_A$ = +25°C | ±8 | ±7 | ±7 | V |
| Total dissipation | $P_D$ | **Note** | 500 ($T_A$ = +85°C) | 280 ($T_A$ = +75°C) | 280 ($T_A$ = +75°C) | mW |
| Differential input voltage | $V_{ID}$ | $T_A$ = +25°C | ±5 | ±5 | ±5 | V |
| Common mode input voltage | $V_{ICM}$ | $T_A$ = +25°C, within $V_{CC}^-$ to $V_{CC}^+$ range | ±6 | ±6 | ±6 | V |
| Output current | $I_O$ | $T_A$ = +25°C | 35 | 35 | 35 | mA |
| Operating ambient temperature | $T_A$ | | −45 to +85 | −45 to +75 | −45 to +75 | °C |
| Storage temperature | $T_{stg}$ | | −55 to +150 | −55 to +150 | −55 to +150 | °C |

**Note** When mounted on a double sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB

**Table 2. Recommended Operating Conditions**

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}^{\pm}$ ($\mu$PC1663C) | ±2 | ±6 | ±7 | V |
| Power supply voltage | $V_{CC}^{\pm}$ ($\mu$PC1663G, $\mu$PC1663GV) | ±2 | ±6 | ±6.5 | V |
| Output source current | $I_{O\ source}$ | | | 20 | mA |
| Output sink current | $I_{O\ sink}$ | | | 2.5 | mA |
| Operating frequency range | $f_{opt}$ | DC | | 200 | MHz |

**Table 3. Electrical Characteristics ($T_A$ = +25°C, $V_{CC}^{\pm}$ = ±6 V)**

| Parameter | | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Differential voltage gain | Gain 1 | $A_{vd}$ | f = 10 MHz (Note 1) | 200 | 320 | 500 | — |
| | Gain 2 | | f = 10 MHz (Note 2) | 8 | 10 | 12 | |
| Bandwidth | Gain 1 | BW | $R_S$ = 50 Ω | — | 120 | — | MHz |
| | Gain 2 | | (3 dB down point) | — | 700 | — | |
| Rise time | Gain 1 | $t_r$ | $R_S$ = 50 Ω, $V_{out}$ = 1 $V_{P-P}$ | — | 2.9 | — | ns |
| | Gain 2 | | | — | 2.7 | — | |
| Propagation delay | Gain 1 | $t_{pd}$ | $R_S$ = 50 Ω, $V_{out}$ = 1 $V_{P-P}$ | — | 2 | — | ns |
| | Gain 2 | | | — | 1.2 | — | |
| Input resistance | Gain 1 | $R_{in}$ | | — | 4.0 | — | kΩ |
| | Gain 2 | | | 50 | 180 | — | |
| Input capacitance | | $C_{in}$ | | — | 2 | — | pF |
| Input offset current | | $I_{IO}$ | | — | 0.4 | 5.0 | $\mu$A |
| Input bias current | | $I_R$ | | — | 20 | 40 | $\mu$A |
| Input noise voltage | | $V_n$ | $R_S$ = 50 Ω, 10 k to 10 MHz | — | 3 | — | $\mu V_{r.m.s}$ |
| Input voltage range | | $V_I$ | | ±1.0 | — | — | V |
| Common mode rejection ratio | Gain 2 | CMR | $V_{cm}$ = ±1 V, f ≤ 100 kHz | 53 | 94 | — | dB |
| Supply voltage rejection ratio | | SVR | $\Delta V$ = ±0.5 V | 50 | 70 | — | dB |
| Output offset voltage | Gain 1 | $V_{O(off)}$ | $V_{O(off)}$ = \|$OUT_1$ – $OUT_2$\| | — | 0.3 | 1.5 | V |
| | Gain 2 | | | — | 0.1 | 1.0 | |
| Output common mode voltage | | $V_{O(CM)}$ | | 2.4 | 2.9 | 3.4 | V |
| Output voltage swing | | $V_{Op-p}$ | Single end | 3.0 | 4.0 | — | $V_{P-P}$ |
| Output sink current | | $I_{sink}$ | | 2.5 | 3.6 | — | mA |
| Power supply current | | $I_{CC}$ | | — | 13 | 20 | mÁ |

**Notes 1.** Gain 1 is when gain select pins $G_{1A}$ and $G_{1B}$ are connected

**2.** Gain 2 is when none of the gain select pins are connected

**Remark** The detailed specifications and package drawings should be referred to the data sheet (G11024E).

The electrical characteristics are defined as follows.

### 3.1 Differential Voltage Gain ($A_{VD}$)

As was described in section 2.2, this indicates the ratio between the differential input and differential output voltage.

$$A_{VD} = \frac{|\Delta OUT_1| + |\Delta OUT_2|}{|\Delta V_{DIF}|} \quad \text{or} \quad \frac{\Delta|OUT_1 - \Delta OUT_2|}{|\Delta V_{DIF}|}$$

The single-end gain ($A_{VS}$) for single-side output is expressed as one half of $A_{VD}$ shown below.

$$A_{VS} = \frac{|\Delta OUT_1|}{|\Delta V_{DIF}|} \quad \text{or} \quad \frac{|\Delta OUT_2|}{|\Delta V_{DIF}|}$$

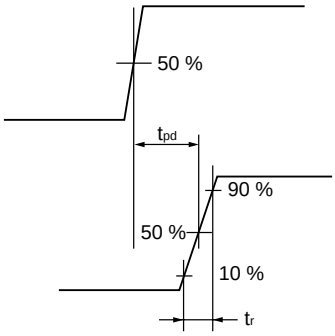
### 3.2 Bandwidth (BW)

This is defined as the bandwidth when there is a 3-dB down gain ($1 / \sqrt{2}$) in relation to the DC gain.

### 3.3 Rise Time ($t_r$) and Propagation Delay Time ($t_{pd}$)

These are defined as shown below for this IC.

**Figure 5. Measurement Conditions for $t_{pd}$ and $t_r$**




### 3.4 Input Resistance ($R_{in}$)

This indicates the ratio of the change in the input bias voltage ($\Delta I_B$) to the change in the input voltage ($\Delta V_{IN}$).

$R_{IN} = \Delta V_{IN} / \Delta I_B$

The input resistance is defined as the product of the input transistor's current gain $\beta$ and the emitter resistance. Therefore, this value is reduced in relation to higher gain values.

### 3.5 Input Capacitance ($C_{in}$)

This indicates the capacitance between the input and the GND.

### 3.6 Input Offset Current ($I_{IO}$)

This is the offset current of the dual input bias current.

$I_{IO} = |IB_1 - IB_2|$

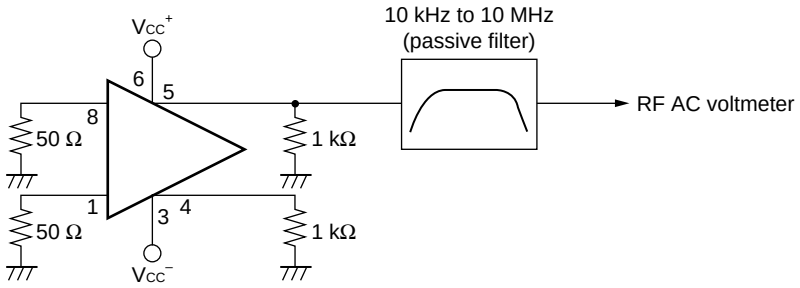
### 3.7 Input Bias Current ($I_B$)

This indicates the base current at input transistors $Q_1$ and $Q_2$.

### 3.8 Input Noise Voltage ($V_n$)

In Figure 6, the value measured by an RF AC voltmeter is divided by the single-end gain value.

**Figure 6. Input Noise Voltage Measurement Circuit**

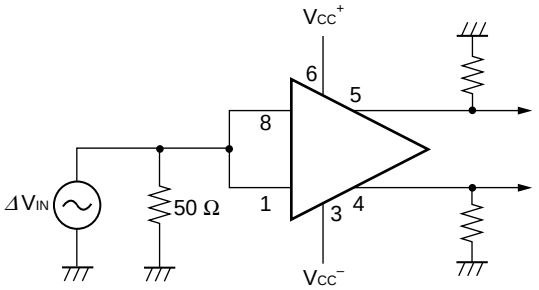



### 3.9 Input Voltage Range ($V_I$)

This indicates the input voltage range for normal operation, during which input signals must be within this range. With the intermediate potential between $V_{CC}^+$ and $V_{CC}^-$ as the center, the input voltage range is guaranteed within ±1 V (when $V_{CC}^+ - V_{CC}^- = 12$ V).

### 3.10 Common Mode Rejection Ratio (CMR)

**Figure 7. Common Mode Rejection Ratio Measurement Circuit**




This indicates the rate of variation in the input conversion offset relative to the common mode input signal. This can be expressed as follows, based on the circuit shown in Figure 7.

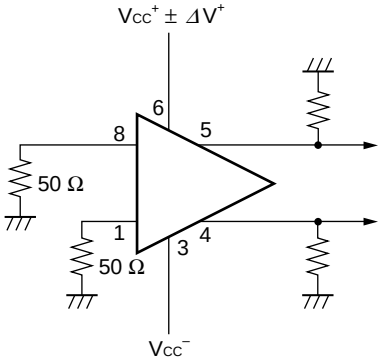
$$CMR = 20 \log \frac{\Delta V_{IN}}{\Delta V_O} \bullet A_{VD}$$

### 3.11 Supply Voltage Rejection Ratio (SVR)

This indicates the rate of variation in the input conversion offset relative to the supply voltage.
This can be expressed as follows, based on the circuit shown in Figure 8.

$$SVR = 20 \log \frac{\Delta V^{+}}{\Delta V_O} \bullet A_{VD}$$

**Figure 8. Supply Voltage Rejection Ratio Measurement Circuit ($V^+$ side)**




$\Delta V_O = |\Delta OUT_1| + |\Delta OUT_2|$

### 3.12 Output Offset Voltage ($V_{O(off)}$)

This indicates the DC voltage difference between both outputs when both of the differential inputs voltage is not applied.

$$V_{O(off)} = |OUT_1 - OUT_2|$$

### 3.13 Output Common Mode Voltage ($V_{O(CM)}$)

This indicates the average value from both output's DC voltages when both of the differential inputs voltage is not applied.

$$V_{O(CM)} = \frac{OUT_1 + OUT_2}{2}$$

### 3.14 Output Voltage Swing ($V_{Op-p}$)

This indicates the maximum amplitude (swing) that occurs without distortion, mainly in the output common mode voltage.

### 3.15 Output Sink Current

This indicates the sink current capacity of transistors $Q_{10}$ and $Q_{11}$. If a current that exceeds this value is accepted, the output voltage swing is greatly reduced.

### 3.16 Power Supply Current

This indicates the circuit current and does not include the output load current.

## 4. PRECAUTIONS FOR DESIGN IN

### 4.1 Cautions on Layout and Wiring

In high-frequency circuits, the PCB design can considerably influence circuit performance.

When using this device with an especially high gain, you must note that oscillation might occur even when there is only a slight amount of external feedback.

The following cautions concern the device mounting layout.

- Form as wide an area as possible for the ground pattern so as to prevent feedback due to conductor inductance (a double sided copper clad epoxy glass PWB is recommended).
- Make the leads from external components and the link wiring between front and rear components as short as possible.
- Use a single ground as the ground for input/output circuit and the power supply.
- Form the ground pattern to shield the input and output wiring so as to prevent feedback due to stray capacitance.
- Lay out the output signal current path at a distance from the input wiring.
- The power supply is bypassed very near to the IC's power supply pin by a small-inductance, high-frequency capacitor. If the power supply wiring is long, insert a small resistance (up to 10 Ω) in series.
- The ground for the bypass capacitor should be laid out in order to form a loop only with the power supply line so as to prevent the high-frequency current that runs throughout the PCB from entering the input.

### 4.2 Cautions on External Circuit

This IC features greatly improved phase characteristics, such that the characteristics inherent to this IC make it one of the more stable wideband amplifier ICs. However, the following cautions should be noted when this IC is used in application circuits.

- Whenever possible, the signal source resistance values should be the same for the two inputs. Signal source resistance values should be minimized, with 1 kΩ maximum (If the signal source impedance is too large, the input amplitude becomes large and the output will become saturated).
- Whenever possible, the load resistance values should be the same for the two outputs.

  * For this IC, it is essential that a balance be maintained between the two lines ($IN_1$ to $OUT_1$ and $IN_2$ to $OUT_2$) in the application circuit.

### 4.3 Other Caution Points

- Use of single (power) supply

  This IC can be used with a single supply if the input voltage is biased at the intermediate between $V_{CC}^+$ and $V_{CC}^-$, as is shown in the application circuit example in the data sheet. More detailed circuit examples and their characteristics are shown in Figure 9 and Tables 4 and 5.

  Note, however, that in this case the load current along $R_L$ is more than twice as great as when the load is connected with ± power supply to a ground (recommended: max. 20 mA, $I_O = \frac{V_{O(CM)}}{R_L}$ ).

**Figure 9. Example Using Single Power Supply**

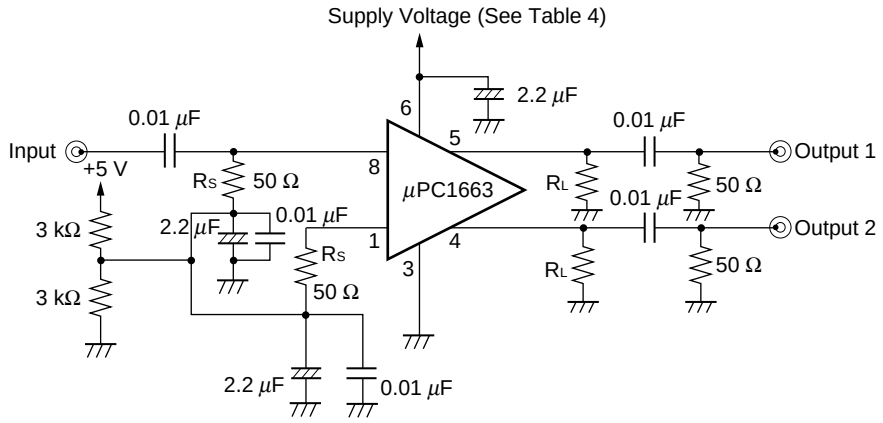



**Table 4. Reference Usage Range**

| Parameter | Symbol | Condition | μPC1663C | μPC1663G | μPC1663GV | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}^{+} - V_{CC}^{-}$ | Single power supply | –0.3 to +16 | –0.3 to +14 | –0.3 to +14 | V |

**Table 5. +5 V Single Power Supply Operation Performance (Based on Figure 9)**

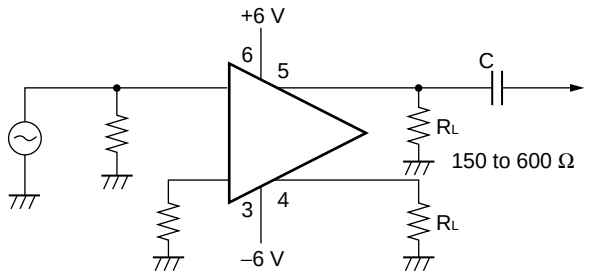
| Parameter | | Condition | Characteristics | Unit |
|---|---|---|---|---|
| Gain | Gain 1 | 15 MHz | 35 | dB |
| | Gain 2 | | 11 | |
| Bandwidth | Gain 1 | 3 dB down point | 106 | MHz |
| | Gain 2 | | 115 | |
| Rise time | Gain 1 | $R_S$ = 50 Ω, $V_{OUT}$ = 80 $mV_{P-P}$ | 2.2 | ns |
| Propagation delay time | Gain 1 | $R_S$ = 50 Ω, $V_{OUT}$ = 80 $mV_{P-P}$ | 2.8 | ns |
| | Gain 2 | $R_S$ = 50 Ω, $V_{OUT}$ = 60 $mV_{P-P}$ | 1.8 | |
| Phase | Gain 1 | 100 MHz | –123 | degree |
| | Gain 2 | | –93 | |
| Output, Max. | $R_L$ = 240 Ω | $R_L$ = 50 Ω | 5.0 | dBm |
| | $R_L$ = 910 Ω | 15 MHz | 0 | |
| | $R_L$ = 80 Ω | | –11.5 | |

- Driving a low-impedance line

  As was described in section 3.15 above, the sink current of the IC itself is only 3.6 mA (TYP.), which is inadequate for driving a low-impedance line such as a video line. As is shown in Figure 10, it is possible to drive a low-impedance line if a bypass resistor rated between 150 and 600 Ω is connected and a capacitor coupling is used to link the increased drive capacity of the output-level emitter-follower.

  In this case, the output current ($I_O$ = ($V_{O(CM)}$ / $R_L$) generated based on the $R_L$ value should not be more than 20 mA.

**Figure 10. Driving a Low Impedance Line**




## 5. APPLICATION CIRCUIT EXAMPLES

### 5.1 Video Line Driver Circuit Example

**Figure 11. Video Line Driver Circuit Example**

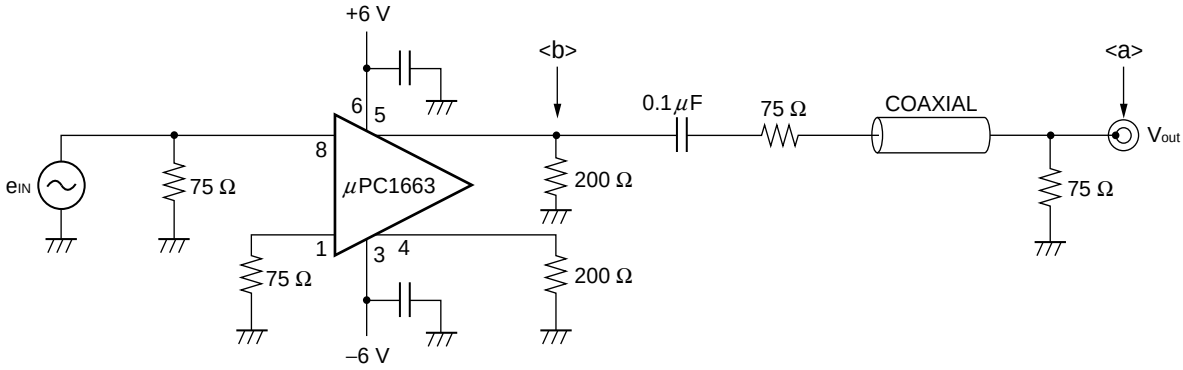
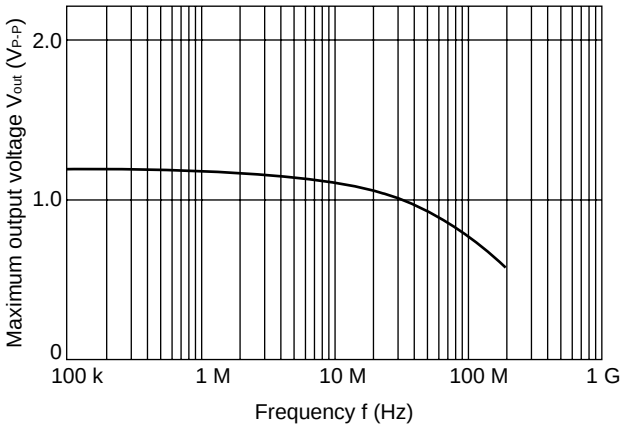
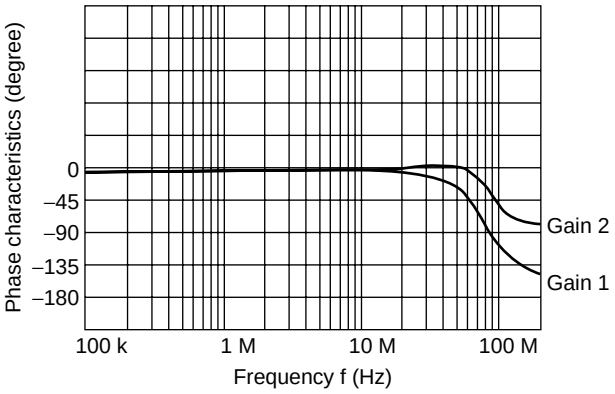



**Figure 12. $V_{out}$ vs. f Characteristics (Video Line, Single End)**



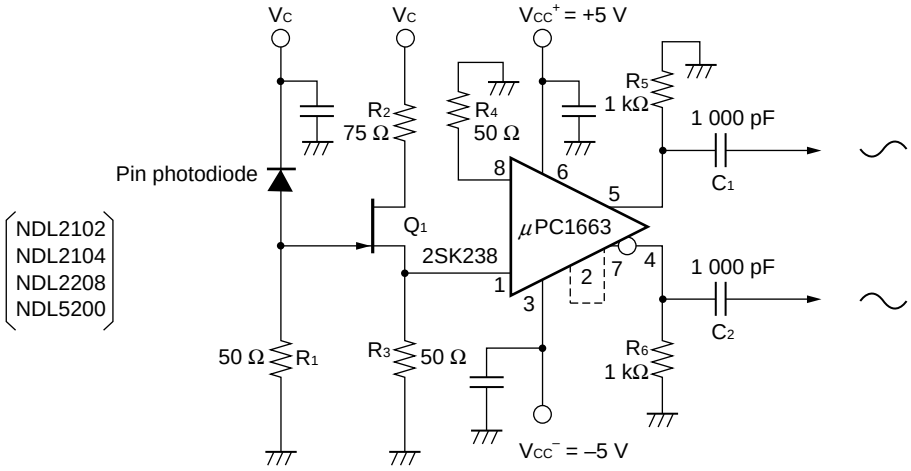

**Remark** The measurement results in Figure 12 are the values of point <a> in Figure 11 of the application circuit. The values for the μPC1663 are those of point <b>, therefore when converted, they are equivalent to approximately twice the value of $V_{out}$ at point <a>. Because the measured values at point <a> are single-end, in the case of differential I/O, the values of points <a> and <b> are twice the value of the single-end values.

**Figure 13. Phase Characteristics vs. Frequency Characteristics**




## 5.2 Optical Signal Detection Circuit Example

**Figure 14. Optical Signal Detection Circuit Example**



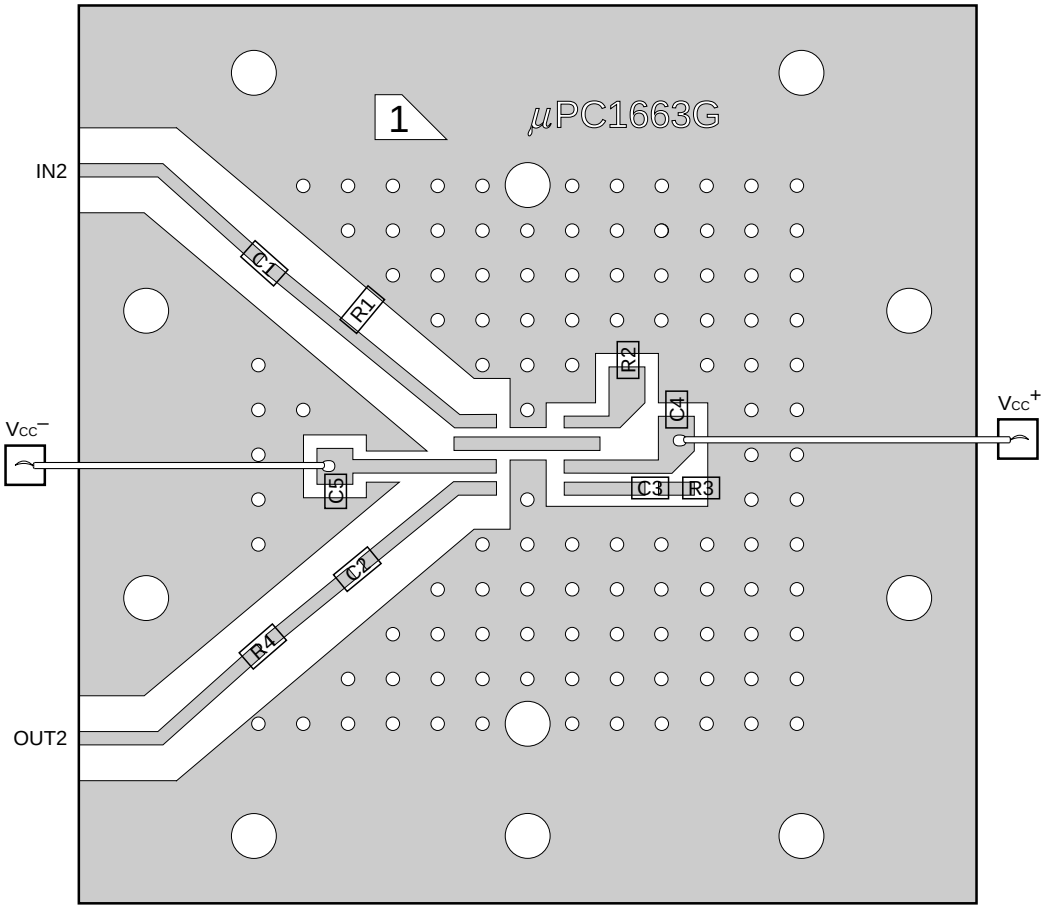

Since a high gain value may lower the IC's input impedance, stable operation can be ensured by including an FET buffer (source follower), as is shown in Figure 14. This FET buffer also shifts the level of the input voltage from the diode. For detail on the FET and PIN photodiode, see the data sheet for each product.

## 6. EXAMPLE OF MOUNTING MEASURING CIRCUIT ON PRINTED BOARD

### 6.1 Example of Mounting μPC1663G on Printed Board

Figure 15 shows an example of mounting of 8-pin SOP 225-mil type product on a PCB for use in the test circuit described in the μPC1663 data sheet. The evaluation board in Figure 15 is designed for single-end test circuit of IN2 input and OUT2 output.

**Figure 15. Example of assembled test Circuit on Evaluation Board**




**Parts Table**

| No. | Value |
|---|---|
| C1 to 3 | 0.1 μF |
| C4 to 5 | 1000 pF |
| R1 to 2 | 50 Ω |
| R3 | 1 kΩ |
| R4 | 950 Ω* |

**Notes on Printed Board**

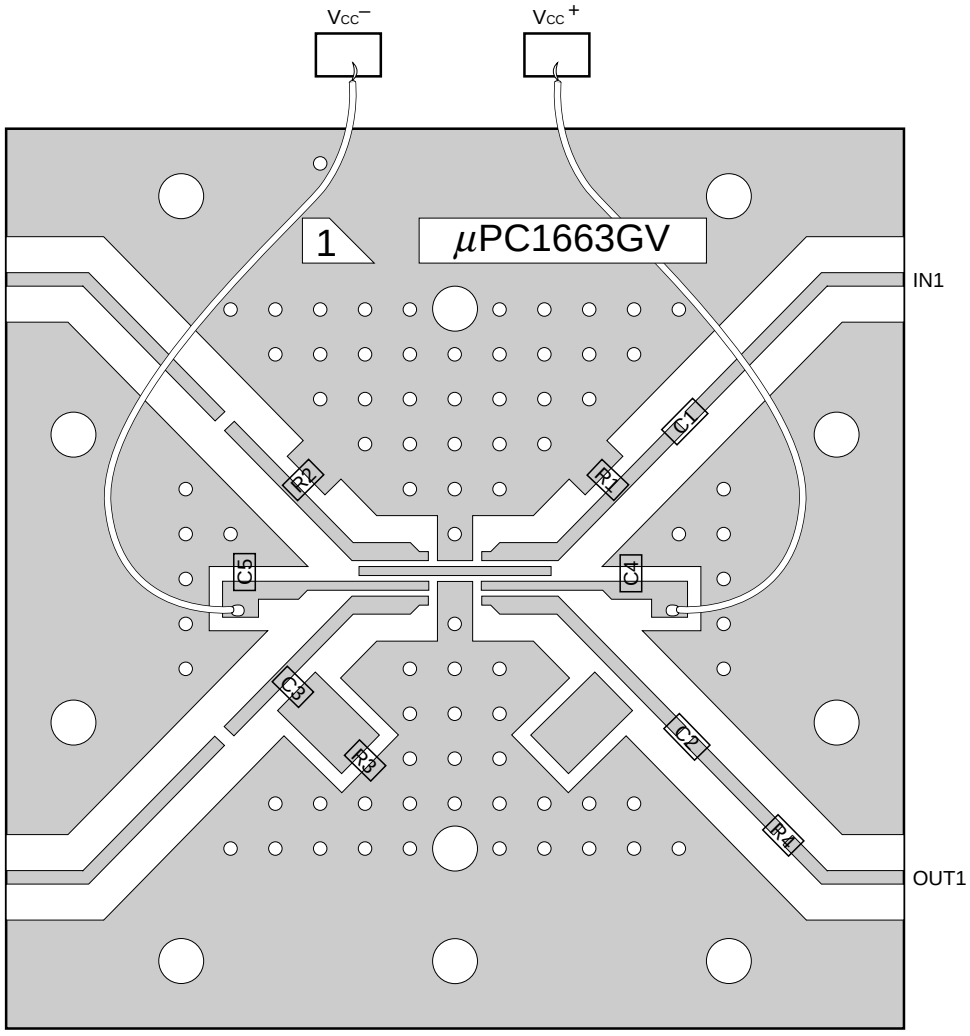
(*1) 35-μm copper patterning on both sides of 50 × 50 × 0.4-mm polyimide board
(*2) Rear side ground pattern
(*3) Solder plating of patterning side
(*4) ○ O is through-hole.
(*5) To mount C2, pattern should be cut.

***** R4 is the value obtained by subtracting the impedance of the measuring instrument from R3.

## 6.2 Example of Mounting μPC1663GV on Printed Board

Figure 16 shows an example of mounting of 8-pin SSOP 175-mil type product on a PCB for use in the test circuit described in the μPC1663 data sheet. This evaluation board can be used either for a single-end or differential amplifier. The assembled example in Figure 16 is for a single-end amplifier and provides one IN1 and one OUT1 pins.

**Figure 16. Example of assembled test Circuit on Evaluation Board**




**Parts Table**

| No. | Value |
|---|---|
| C1 to 3 | 0.1 μF |
| C4 to 5 | 1000 pF |
| R1 to 2 | 50 Ω |
| R3 | 1 kΩ |
| R4 | 950 Ω* |

**Notes on Printed Board**

(*1) 35-μm copper patterning on both sides of 50 × 50 × 0.4-mm polyimide board
(*2) Rear side ground pattern
(*3) Solder plating of patterning side
(*4) ○ O is through-hole.
(*5) To mount R4, pattern should be cut.

***** R4 is the value obtained by subtracting the impedance of the measuring instrument from R3.

## 7. CONCLUSION

The usage of the μPC1663 DC to VHF wideband differential input and output amplifier IC has been described above.

Another product that uses a high-frequency process, the μPC2726T, is also offered as an L-band differential input and differential output wideband amplifier IC that operates up to 1.6 GHz.

**Reference Materials**

μPC1663 Data Sheet (Document No. G11024E)

μPC2726T Data Sheet (Document No. P10873E)

**[MEMO]**

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