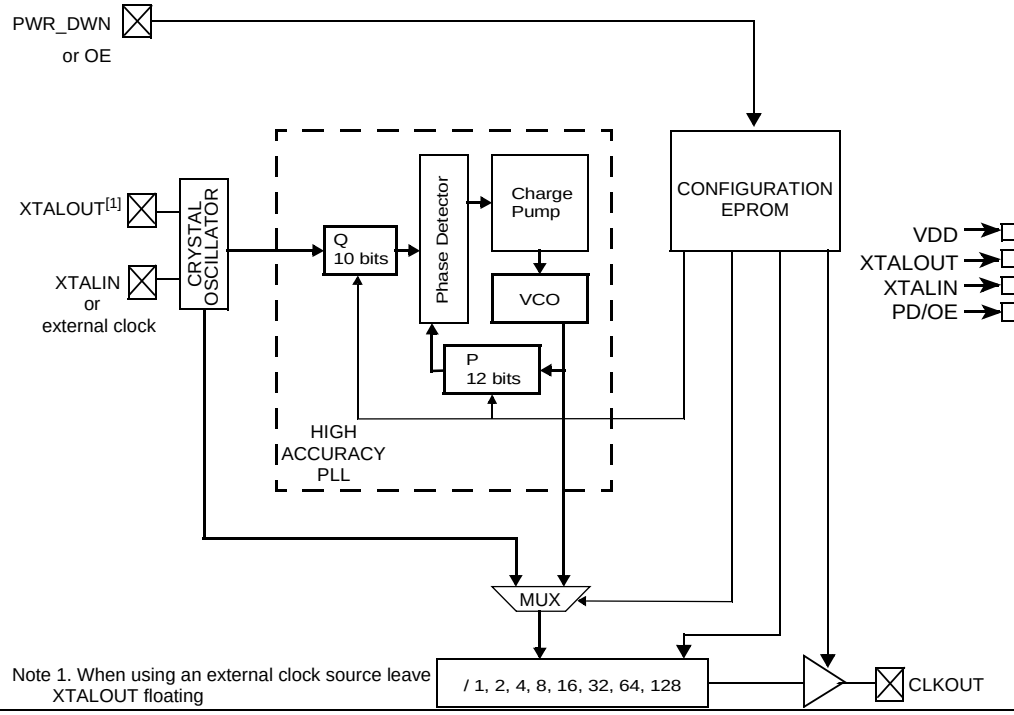
# CY2077

# High Accuracy EPROM Programmable Single-PLL Clock Generator

| Features | Benefits |
|---|---|
| • **High accuracy PLL with 12-bit multiplier and 10-bit divider** | Enables synthesis of highly accurate and stable output clock frequencies with zero PPM |
| • **EPROM-programmability** | Enables quick turnaround of custom frequencies |
| • **3.3V or 5V operation** | Supports industry standard design platforms |
| • **Operating frequency**<br>**— 390 kHz–133 MHz at 5V**<br>**— 390 kHz–100 MHz at 3.3V** | Services most PC, networking, and consumer applications |
| • **Reference input from either a 10-30 MHz fundamental toned crystal or a 1-75 MHz external clock** | Lowers cost of oscillator as PLL can be programmed to a high frequency using either a low-frequency, low-cost crystal, or an existing system clock |
| • **EPROM-selectable TTL or CMOS duty cycle levels** | Duty cycle centered at 1.5V or $V_{DD}/2$<br>Provides flexibility to service most TTL or CMOS applications |
| • **Sixteen selectable post-divide options, using either PLL or reference oscillator/external clock** | Provides flexibility in output configurations and testing |
| • **Programmable PWR_DWN or OE pin, with asynchronous or synchronous modes** | Enables low-power operation or output enable function and flexibility for system applications, through selectable instantaneous or synchronous change in outputs |
| • **Low Jitter outputs typically**<br>**— 80 ps at 3.3V/5V** | Suitable for most PC, consumer, and networking applications |
| • **Controlled rise and fall times and output slew rate** | Has lower EMI than oscillators |
| • **Available in both commercial and industrial temperature** | Suitable to fit most applications |
| • **Factory-programmable device options** | Easy customization and fast turnaround. |

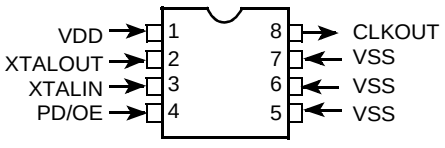
## CY2077 Logic Block Diagram




Note 1. When using an external clock source leave XTALOUT floating

## Pin Configuration

**8-Pin Top View**



## Functional Description

The CY2077 is an EPROM-programmable, high-accuracy, general purpose, PLL-based design for use in applications such as modems, disk drives, CD-ROM drives, video CD players, DVD players, games, set-top boxes, and data/telecommunications.

The CY2077 can generate a clock output up to 133 MHz at 5V or 100 MHz at 3.3V. It has been designed to give the customer a very accurate and stable clock frequency with little to zero PPM error. The CY2077 contains a 12-bit feedback counter divider and 10-bit reference counter divider to obtain a very high resolution to meet the needs of stringent design specifications. Further more, there are 8 output divide options of /1, /2, /4, /8, /16, /32, /64, and /128. The output divider can select between the PLL and crystal oscillator output/external clock, providing a total of 16 different options. To add more flexibility in designs. TTL or CMOS duty cycles can be selected.

Power management with the CY2077 is also very flexible. The user may choose either a PWR_DWN or an OE feature with which both have integrated pull-up resistors. PWR_DWN and OE signals can be programmed to have asynchronous and synchronous timing with respect to the output siginal. There is a weak pull-down on the output that will pull CLKOUT low when either the PWR_DWN or OE siginal is active. This weak pull-down can easily be overridden by another clock signal in designs where multiple clock signals share a signal path.

Multiple options for output selection, better power distribution layout, and controlled rise and fall times enable the CY2077 to be used in applications which require low jitter and accurate reference frequencies.

## EPROM Configuration Block

*Table 1* summarizes the features which are configurable by EPROM

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**Table 1. EPROM Adjustable Features**

| EPROM Adjustable Features | |
|---|---|
| Adjust Freq. | Feedback counter value (P) |
| | Reference counter value (Q) |
| | Output divider selection |
| Duty cycle levels (TTL or CMOS) | |
| Power management mode (OE or PWR_DWN) | |
| Power management timing (synchronous or asynchronous) | |

## PLL Output Frequency

The CY2077 contains a high resolution PLL with 12 bit multiplier and 10 bit divider.The output frequency of the PLL is determined by the following formula:

$$F_{PLL} = \frac{2 \bullet (P + 5)}{(Q + 2)} \bullet F_{REF}$$

where P is the feedback counter value and Q is the reference counter value. P and Q are EPROM programmable values.

The calculation of P and Q values for a given PLL output frequency is handled by the CyClocks software. Refer to the “Custom Configuration Request Procedure” section for details.

## Power Management Features

PWR_DWN and OE options are configurable by EPROM programming for the CY2077. In PWR_DWN mode, all active circuits are powered down when the control pin is set to LOW. When the control pin is set back to HIGH, both the PLL and oscillator circuit must re-lock. In the case of OE, the output is three-stated and weakly pulled down when the control pin is set to LOW. The oscillator and PLL are still active in this state, which leads to a quick clock output return when the control pin is set back to HIGH.

Additionally, PWR_DWN and OE can be configured to occur asynchronously or synchronously with respect to CLKOUT. In asynchronous mode, PWR_DWN or OE disables CLKOUT immediately (allowing for logic delays), without respect to the current state of CLKOUT. Synchronous mode will prevent output glitches by waiting for the next falling edge of CLKOUT after PWR_DWN or OE becomes asserted. In either asynchronous or synchronous setting, the output is always enabled synchronously by waiting for the next falling edge of CLKOUT.

## Pin Summary

| Name | Pin | Description |
|---|---|---|
| $V_{DD}$ | 1 | Voltage supply. |
| $V_{SS}$ | 5,6,7 | Ground (all the pins have to be grounded). |
| $X_D$ | 2 | Crystal output (leave this pin floating when external reference is used.). |
| $X_G$ | 3 | Crystal input or external input reference. |
| PWR_DWN / OE | 4 | EPROM programmable power down or output enable pin. Weak pull-up. |
| CLKOUT | 8 | Clock output. Weak pull-down. |

## Device Functionality: Output Frequencies

| Symbol | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Fo | Output frequency | $V_{DD}$ = 4.5–5.5V | 0.39 | 133 | MHz |
| | | $V_{DD}$ = 3.0–3.6V | 0.39 | 100 | MHz |

## Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .....–0.5 to +7.0V

Input Voltage .....–0.5V to $V_{DD}$+0.5V

Storage Temperature (Non-Condensing) ... –55°C to +150°C

Junction Temperature ..... 150°C

Static Discharge Voltage ..... ≥2000V (per MIL-STD-883, Method 3015)

## Operating Conditions for Commercial Temperature Device

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.0 | 5.5 | V |
| $T_A$ | Operating Temperature, Ambient | 0 | +70 | °C |
| $C_{TTL}$ | Max. Capacitive Load on outputs for TTL levels<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 1–40 MHz<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 40–125 MHz<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 125–133 MHz | | <br>50<br>25<br>15 | <br>pF<br>pF<br>pF |
| $C_{CMOS}$ | Max. Capacitive Load on outputs for CMOS levels<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 1–40 MHz<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 40–125 MHz<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 125–133 MHz<br>$V_{DD}$ = 3.0–3.6V, Output frequency = 1–40 MHz<br>$V_{DD}$ = 3.0–3.6V, Output frequency = 40–100 MHz | | <br>50<br>25<br>15<br>30<br>15 | <br>pF<br>pF<br>pF<br>pF<br>pF |
| $X_{REF}$ | Reference Frequency, input crystal with $C_{load}$ = 10 pF | 10 | 30 | MHz |
| | Reference Frequency, external clock source | 1 | 75 | MHz |

## Electrical Characteristics $T_A$ = 0°C to +70°C

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level Input Voltage | $V_{DD}$ = 4.5–5.5V<br>$V_{DD}$ = 3.0–3.6V | | | 0.8<br>0.2$V_{DD}$ | V<br>V |
| $V_{IH}$ | High-level Input Voltage | $V_{DD}$ = 4.5–5.5V<br>$V_{DD}$ = 3.0–3.6V | 2.0<br>0.7$V_{DD}$ | | | V<br>V |
| $V_{OL}$ | Low-level Output Voltage | $V_{DD}$ = 4.5–5.5V, $I_{OL}$= 16 mA<br>$V_{DD}$ = 3.0–3.6V, $I_{OL}$= 8 mA | | | 0.4<br>0.4 | V<br>V |
| $V_{OHCMOS}$ | High-level Output Voltage, CMOS levels | $V_{DD}$ = 4.5–5.5V, $I_{OH}$= –16 mA<br>$V_{DD}$ = 3.0–3.6V, $I_{OH}$= –8 mA | $V_{DD}$–0.4<br>$V_{DD}$–0.4 | | | V<br>V |
| $V_{OHTTL}$ | High-level Output Voltage, TTL levels | $V_{DD}$ = 4.5–5.5V, $I_{OH}$= –8 mA | 2.4 | | | V |
| $I_{IL}$ | Input Low Current | $V_{IN}$ = 0V | | | 10 | µA |
| $I_{IH}$ | Input High Current | $V_{IN}$ = $V_{DD}$ | | | 5 | µA |
| $I_{DD}$ | Power Supply Current, Unloaded | $V_{DD}$ = 4.5–5.5V, Output frequency <= 133 MHz<br>$V_{DD}$ = 3.0–3.6V, Output frequency <= 100 MHz | | | 45<br>25 | mA<br>mA |
| $I_{DDS}$ | Stand-by current (PD = 0) | $V_{DD}$ = 4.5-5.5V<br>$V_{DD}$ = 3.0-3.6V | | 25<br>10 | 100<br>50 | µA |
| $R_{UP}$ | Input Pull-Up Resistor | $V_{DD}$ = 4.5–5.5V, $V_{IN}$ = 0V<br>$V_{DD}$ = 4.5–5.5V, $V_{IN}$ = 0.7$V_{DD}$ | 1.1<br>50 | 3.0<br>100 | 8.0<br>200 | MΩ<br>kΩ |
| $I_{OE\_CLKOUT}$ | CLKOUT Pulldown current | $V_{DD}$=5.0 | | 20 | | µA |

**Note:**

1. When using CyClocks, please note that the PLL frequency range is from 50 MHz to 250 MHz for 5V $V_{DD}$ supply, and 50 MHz to 180 MHz for 3V $V_{DD}$ supply. The output frequency is determined by the selected output divider.

## Output Clock Switching Characteristics Commercial Over the Operating Range[2]

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{1w}$ | Output Duty Cycle at 1.4V, $V_{DD}$ = 4.5–5.5V $t_{1w} = t_{1A} \div t_{1B}$ | 1–40 MHz, $C_L$ <= 50 pF<br>40–125 MHz, $C_L$ <= 25 pF<br>125–133 MHz, $C_L$ <= 15 pF | 45<br>45<br>45 | | 55<br>55<br>55 | %<br>%<br>% |
| $t_{1x}$ | Output Duty Cycle at $V_{DD}/2$, $V_{DD}$ = 4.5–5.5V $t_{1x} = t_{1A} \div t_{1B}$ | 1–40 MHz, $C_L$ <= 50 pF<br>40–125 MHz, $C_L$ <= 25 pF<br>125–133 MHz, $C_L$ <= 15 pF | 45<br>45<br>45 | | 55<br>55<br>55 | %<br>%<br>% |
| $t_{1y}$ | Output Duty Cycle at $V_{DD}/2$, $V_{DD}$ = 3.0–3.6V $t_{1y} = t_{1A} \div t_{1B}$ | 1–40 MHz, $C_L$ <= 30 pF<br>40–100 MHz, $C_L$ <= 15 pF | 45<br>40 | | 55<br>60 | %<br>% |
| $t_2$ | Output Clock Rise Time | Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 50 pF<br>Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 25 pF<br>Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 15 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 4.5V–5.5V, $C_L$ = 50 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 3.0V–3.6V, $C_L$ = 30 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 3.0V–3.6V, $C_L$ = 15 pF | | | 1.8<br>1.2<br>0.9<br>3.4<br>4.0<br>2.4 | ns<br>ns<br>ns<br>ns<br>ns<br>ns |
| $t_3$ | Output Clock Fall Time | Between 0.8V–2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 50 pF<br>Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 25 pF<br>Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 15 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 4.5V-5.5V, $C_L$ = 50 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 3.0V–3.6V, $C_L$ = 30 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 3.0V–3.6V, $C_L$ = 15 pF | | | 1.8<br>1.2<br>0.9<br>3.4<br>4.0<br>2.4 | ns<br>ns<br>ns<br>ns<br>ns<br>ns |
| $t_4$ | Start-Up Time Out of Power-Down | PWR_DWN pin LOW to HIGH[3] | | 1 | 2 | ms |
| $t_{5a}$ | Power Down Delay Time (synchronous setting) | PWR_DWN pin LOW to output LOW (T=period of output clk) | | T/2 | T+10 | ns |
| $t_{5b}$ | Power Down Delay Time (asynchronous setting) | PWR_DWN pin LOW to output LOW | | 10 | 15 | ns |
| $t_6$ | Power Up Time | From power-on[1] | | 1 | 2 | ms |
| $t_{7a}$ | Output Disable Time (synchronous setting) | OE pin LOW to output Hi-Z (T=period of output clk) | | T/2 | T+10 | ns |
| $t_{7b}$ | Output Disable Time (asynchronous setting) | OE pin LOW to output Hi-Z | | 10 | 15 | ns |
| $t_8$ | Output Enable Time (always synchronous enable) | OE pin LOW to HIGH (T=period of output clk) | | T | 1.5T +25ns | ns |
| $t_9$ | Peak-to-Peak Period Jitter | $V_{DD}$=3.0V–3.6V, 4.5V–5.5V, Fo>33 MHz, VCO>100 MHz<br>$V_{DD}$= 3.0V–5.5V, Fo <33 MHz | | 80<br>0.3 % | 150<br>1% | ps<br>% of $F_O$ |

**Notes:**

2. Not all parameters measured in production testing.
3. Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70Ω.

## Operating Conditions for Industrial Temperature Device

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.0 | 5.5 | V |
| $T_A$ | Operating Temperature, Ambient | –40 | +85 | °C |
| $C_{TTL}$ | Max. Capacitive Load on outputs for TTL levels<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 1–40 MHz<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 40–125 MHz<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 125–133 MHz | | <br>35<br>15<br>10 | <br>pF<br>pF<br>pF |
| $C_{CMOS}$ | Max. Capacitive Load on outputs for CMOS levels<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 1–40 MHz<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 40–125 MHz<br>$V_{DD}$ = 4.5–5.5V, Output frequency = 125–133 MHz<br>$V_{DD}$ = 3.0–3.6V, Output frequency = 1–40 MHz<br>$V_{DD}$ = 3.0–3.6V, Output frequency = 40–100 MHz | | <br>35<br>15<br>10<br>20<br>10 | <br>pF<br>pF<br>pF<br>pF<br>pF |
| $X_{REF}$ | Reference Frequency, input crystal with $C_{load}$ = 10 pF | 10 | 30 | MHz |
| | Reference Frequency, external clock source | 1 | 75 | MHz |

## Electrical Characteristics $T_A$ = –40°C to +85°C

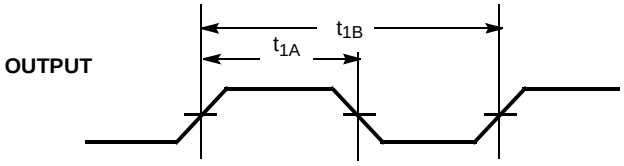
| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level Input Voltage | $V_{DD}$ = 4.5–5.5V<br>$V_{DD}$ = 3.0–3.6V | | | 0.8<br>$0.2V_{DD}$ | V<br>V |
| $V_{IH}$ | High-level Input Voltage | $V_{DD}$ = 4.5–5.5V<br>$V_{DD}$ = 3.0–3.6V | 2.0<br>$0.7V_{DD}$ | | | V<br>V |
| $V_{OL}$ | Low-level Output Voltage | $V_{DD}$ = 4.5–5.5V, $I_{OL}$= 16 mA<br>$V_{DD}$ = 3.0–3.6V, $I_{OL}$= 8 mA | | | 0.4<br>0.4 | V<br>V |
| $V_{OHCMOS}$ | High-level Output Voltage, CMOS levels | $V_{DD}$ = 4.5–5.5V, $I_{OH}$= –16 mA<br>$V_{DD}$ = 3.0–3.6V, $I_{OH}$= –8 mA | $V_{DD}$–0.4<br>$V_{DD}$–0.4 | | | V<br>V |
| $V_{OHTTL}$ | High-level Output Voltage, TTL levels | $V_{DD}$ = 4.5–5.5V, $I_{OH}$= –8 mA | 2.4 | | | V |
| $I_{IL}$ | Input Low Current | $V_{IN}$ = 0V | | | 10 | µA |
| $I_{IH}$ | Input High Current | $V_{IN}$ = $V_{DD}$ | | | 5 | µA |
| $I_{DD}$ | Power Supply Current, Unloaded | $V_{DD}$ = 4.5–5.5V, Output frequency <= 133 MHz<br>$V_{DD}$ = 3.0–3.6V, Output frequency <= 100 MHz | | | 45<br>25 | mA<br>mA |
| $I_{DDS}$ | Stand-by current (PD = 0) | $V_{DD}$ = 4.5-5.5V<br>$V_{DD}$ = 3.0-3.6V | | 25<br>10 | 100<br>50 | µA |
| $R_{UP}$ | Input Pull-Up Resistor | $V_{DD}$ = 4.5–5.5V, $V_{IN}$ = 0V<br>$V_{DD}$ = 4.5–5.5V, $V_{IN}$ = $0.7V_{DD}$ | 1.1<br>50 | 3.0<br>100 | 8.0<br>200 | MΩ<br>kΩ |
| $I_{OE\_CLKOUT}$ | CLKOUT Pulldown current | $V_{DD}$=5.0 | | 20 | | µA |

## Output Clock Switching Characteristics Industrial Over the Operating Range[3]

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{1w}$ | Output Duty Cycle at 1.4V, $V_{DD}$ = 4.5–5.5V $t_{1w} = t_{1A} \div t_{1B}$ | 1–40 MHz, $C_L$ <= 35 pF<br>40–125 MHz, $C_L$ <= 15 pF<br>125–133 MHz, $C_L$ <= 10 pF | 45<br>45<br>45 | | 55<br>55<br>55 | %<br>%<br>% |
| $t_{1x}$ | Output Duty Cycle at $V_{DD}/2$, $V_{DD}$ = 4.5–5.5V $t_{1x} = t_{1A} \div t_{1B}$ | 1–40 MHz, $C_L$ <= 35 pF<br>40–125 MHz, $C_L$ <= 15 pF<br>125–133 MHz, $C_L$ <= 10 pF | 45<br>45<br>45 | | 55<br>55<br>55 | %<br>%<br>% |
| $t_{1y}$ | Output Duty Cycle at $V_{DD}/2$, $V_{DD}$ = 3.0–3.6V $t_{1y} = t_{1A} \div t_{1B}$ | 1–40 MHz, $C_L$ <= 20 pF<br>40–100 MHz, $C_L$ <= 10 pF | 45<br>40 | | 55<br>60 | %<br>% |
| $t_2$ | Output Clock Rise Time | Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 35 pF<br>Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 15 pF<br>Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 10 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 4.5V–5.5V, $C_L$ = 35 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 3.0V–3.6V, $C_L$ = 20 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 3.0V–3.6V, $C_L$ = 10 pF | | | 1.8<br>1.2<br>0.9<br>3.4<br>4.0<br>2.4 | ns<br>ns<br>ns<br>ns<br>ns<br>ns |
| $t_3$ | Output Clock Fall Time | Between 0.8V–2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 35 pF<br>Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 15 pF<br>Between 0.8 –2.0V, $V_{DD}$ = 4.5V–5.5V, $C_L$ = 10 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 4.5V-5.5V, $C_L$ = 35 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 3.0V–3.6V, $C_L$ = 20 pF<br>Between $0.2V_{DD}$– $0.8V_{DD}$, $V_{DD}$= 3.0V–3.6V, $C_L$ = 10 pF | | | 1.8<br>1.2<br>0.9<br>3.4<br>4.0<br>2.4 | ns<br>ns<br>ns<br>ns<br>ns<br>ns |
| $t_4$ | Start-Up Time Out of Power-Down | PWR_DWN pin LOW to HIGH[1] | | 1 | 2 | ms |
| $t_{5a}$ | Power Down Delay Time (synchronous setting) | PWR_DWN pin LOW to output LOW (T=period of output clk) | | T/2 | T+10 | ns |
| $t_{5b}$ | Power Down Delay Time (asynchronous setting) | PWR_DWN pin LOW to output LOW | | 10 | 15 | ns |
| $t_6$ | Power Up Time | From power on[1] | | 1 | 2 | ms |
| $t_{7a}$ | Output Disable Time (synchronous setting) | OE pin LOW to output Hi-Z (T=period of output clk) | | T/2 | T+10 | ns |
| $t_{7b}$ | Output Disable Time (asynchronous setting) | OE pin LOW to output Hi-Z | | 10 | 15 | ns |
| $t_8$ | Output Enable Time (always synchronous enable) | OE pin LOW to HIGH (T=period of output clk) | | T | 1.5T+ 25ns | ns |
| $t_9$ | Peak-to-Peak Period Jitter | $V_{DD}$=3.0V–3.6V, 4.5V–5.5V, Fo>33 MHz, VCO>100 MHz<br>$V_{DD}$= 3.0V–5.5V, Fo <33 MHz | | 80<br>0.3 % | 150<br>1% | ps<br>% of $F_O$ |

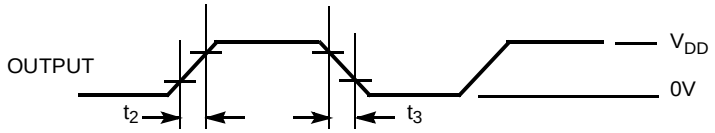
## Switching Waveforms

**Duty Cycle Timing** ($t_{1w}$, $t_{1x}$, $t_{1y}$)

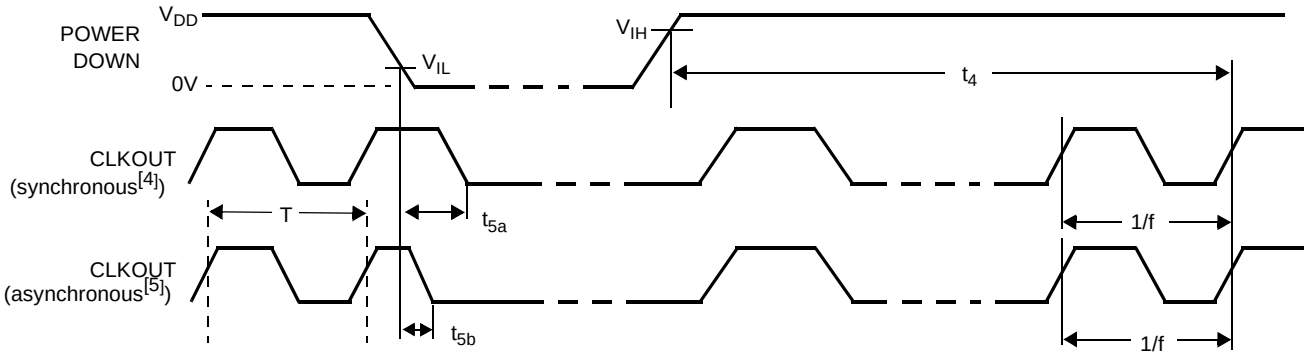


## Switching Waveforms (continued)

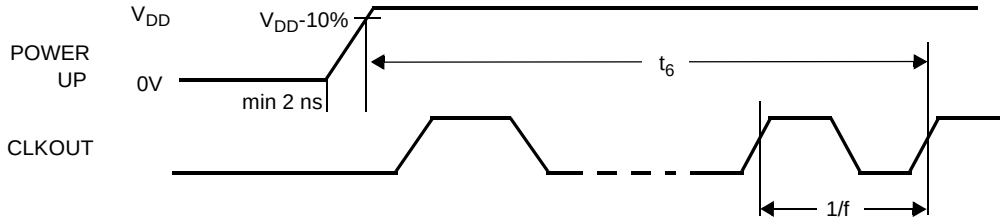
### Output Rise/Fall Time



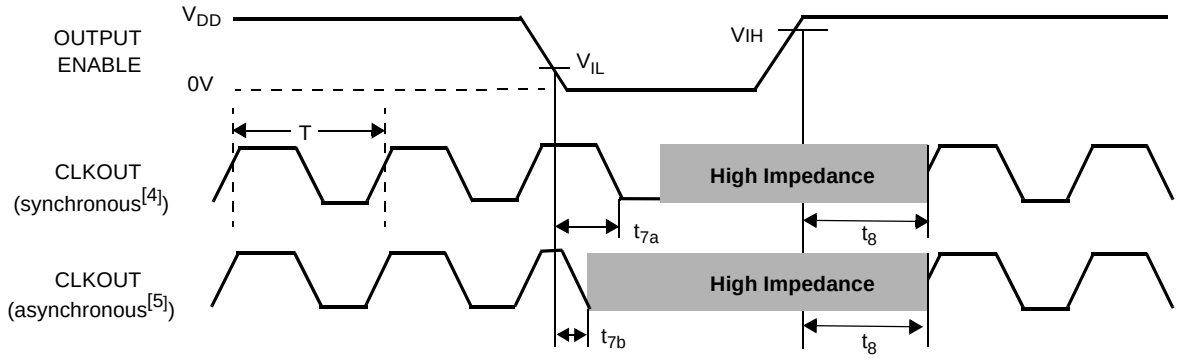

### Power Down Timing (synchronous and asynchronous modes)




### Power Up Timing




### Output Enable Timing (synchronous and asynchronous modes)




**Notes:**

4. In synchronous mode the power-down or output three-state is not initiated until the next falling edge of the output clock.
5. In asynchronous mode the power-down or output three-state occurs within 25 ns irrespective of position in the ouput clock cycle.

## Ordering Information

| Ordering Code | Type | Operating Range |
|---|---|---|
| CY2077SC-XXX | SOIC | Commercial |
| CY2077ZC-XXX | TSSOP | Commercial |
| CY2077SI-XXX | SOIC | Industrial |
| CY2077ZI-XXX | TSSOP | Industrial |

## Custom Configuration Request Procedure

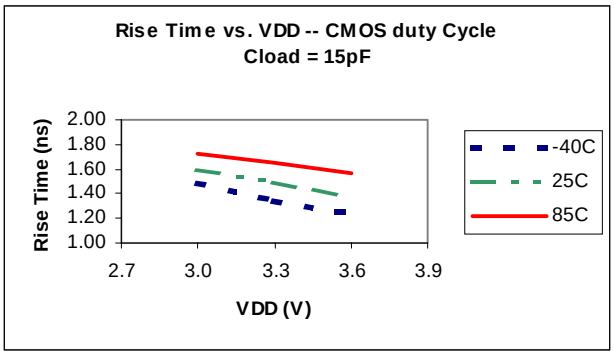
The CY2077 is an EPROM-programmable device that is configured in the factory. The output frequencies requested will be matched as closely as the internal PLL divider and multiplier options allow. All custom requests must be submitted to your local Cypress Field Application Engineer (FAE) or sales representative. The method to use to request custom configurations is:

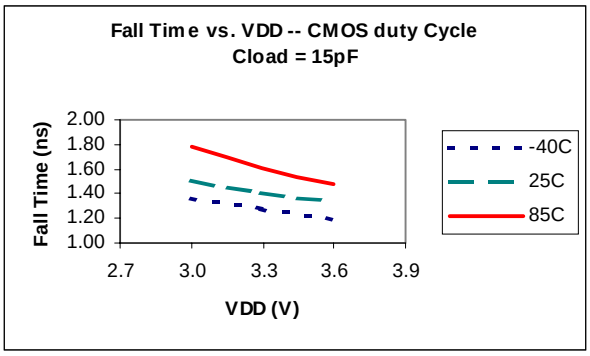
Use CyClocks™ software of version 3.65 or greater. This software automatically calculates the output frequencies that can be generated by the CY2077 devices and provides a print-out of final pinout which can be submitted (in electronic or print format) to your local FAE or sales representative. The CyClocks software is available free of charge from the Cypress website (http://www.cypress.com) or from your local sales representative.

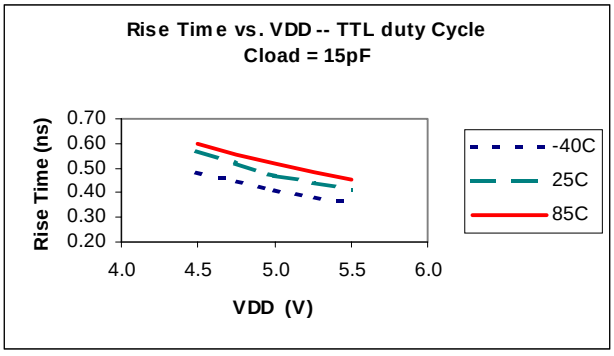
Once the custom request has been processed you will receive a part number with a 3-digit extension (e.g., CY2077SC-103) specific to the frequencies and pinout of your device. This will be the part number used for samples requests and production orders.

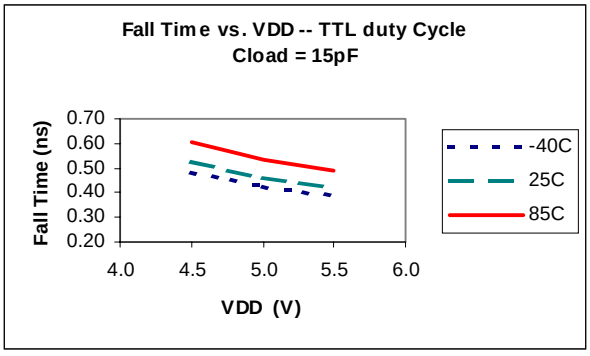
## Typical Rise Time[6] and Fall Time[6] Trends for CY2077

Rise/Fall time vs. $V_{DD}$ over Temperatures

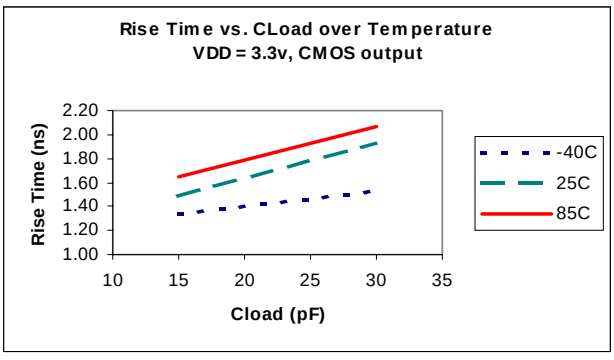


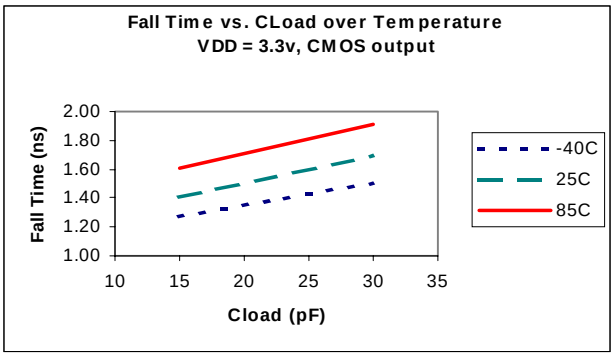




Rise/Fall time vs. Output Loads over Temperatures



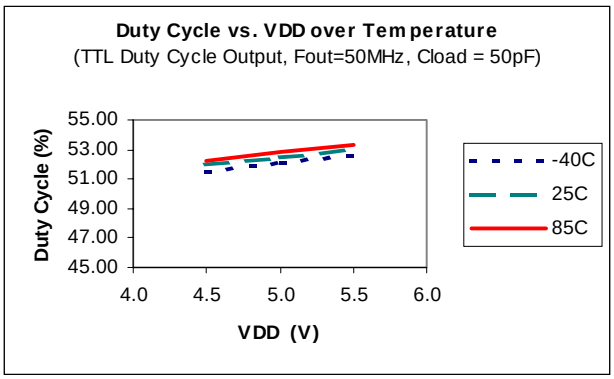



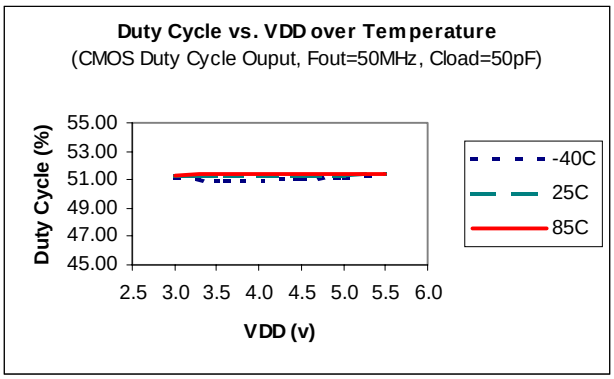

**Note:**

6. Rise/Fall Time for CMOS output is measured between 1.2 $V_{DD}$ and 0.8 $V_{DD}$. Rise/Fall Time for TTL output is measured between 0.8V and 2.0V.

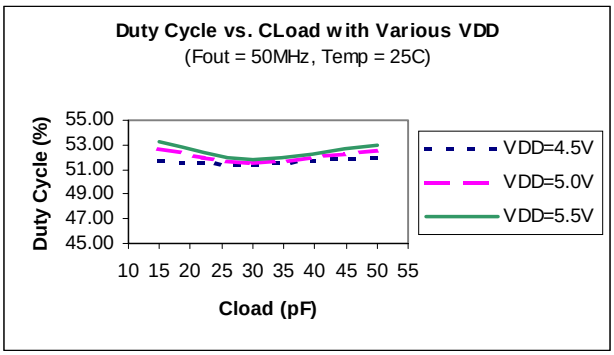
## Typical Duty Cycle[7] Trends for CY2077

Duty Cycle vs. $V_{DD}$ over Temperatures

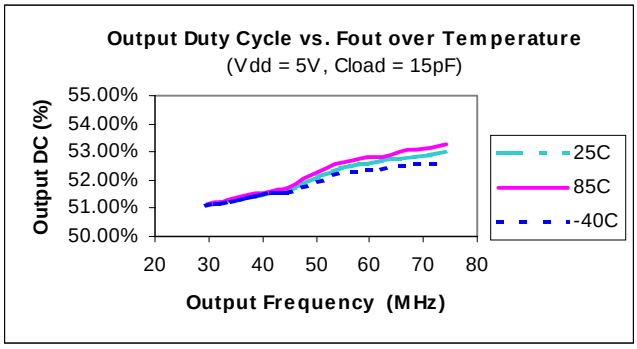



Duty Cycle vs. Output Load




Duty Cycle vs. Output Frequency over Temperatures

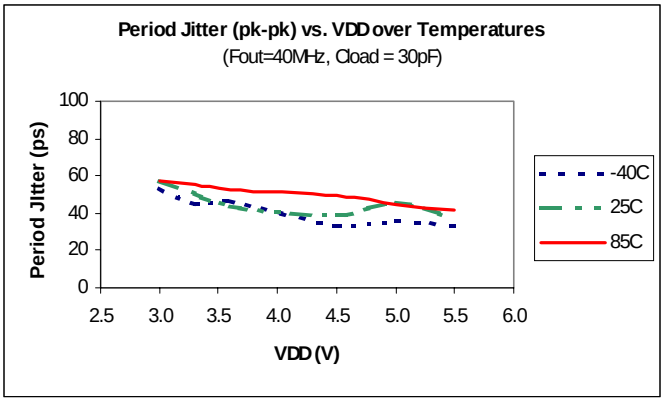



**Note:**

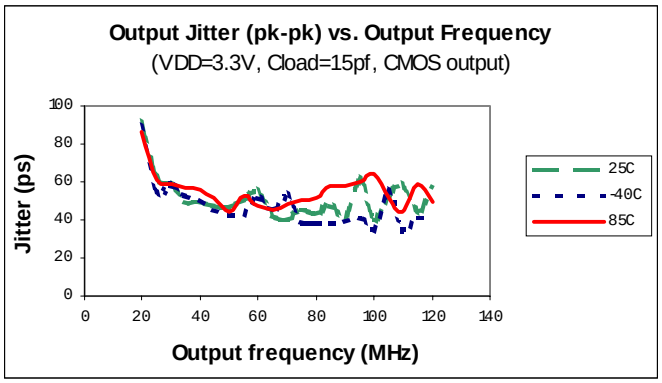
7. Duty Cycle is measured at 1.4V for TTL output and 0.5 $V_{DD}$ for CMOS output.

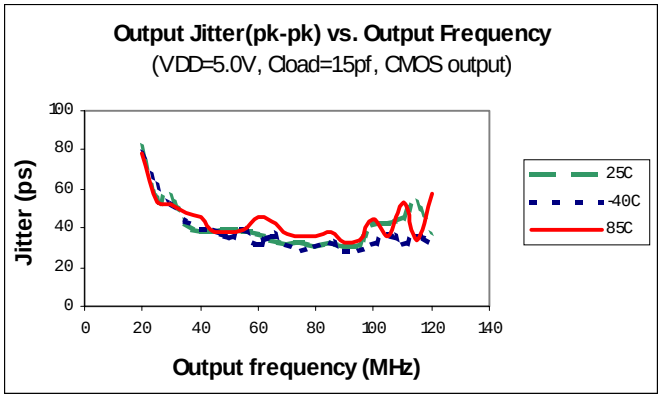
## Typical Jitter Trends for CY2077

Period Jitter (pk-pk) vs. $V_{DD}$ over Temperatures



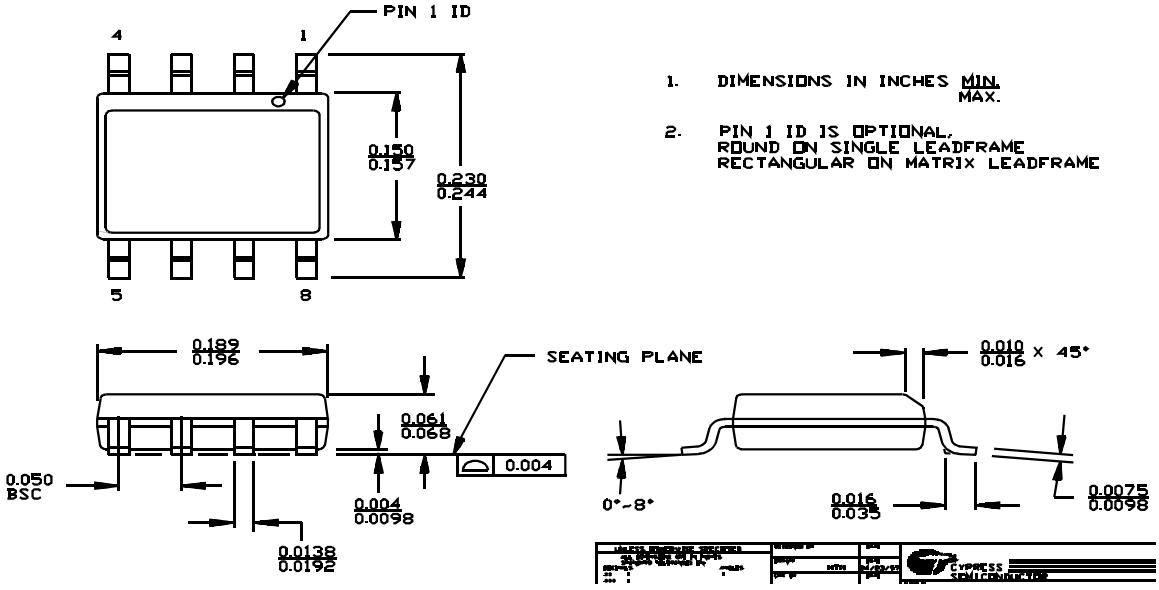

Period Jitter (pk-pk) vs. Output Frequency over Temperatures



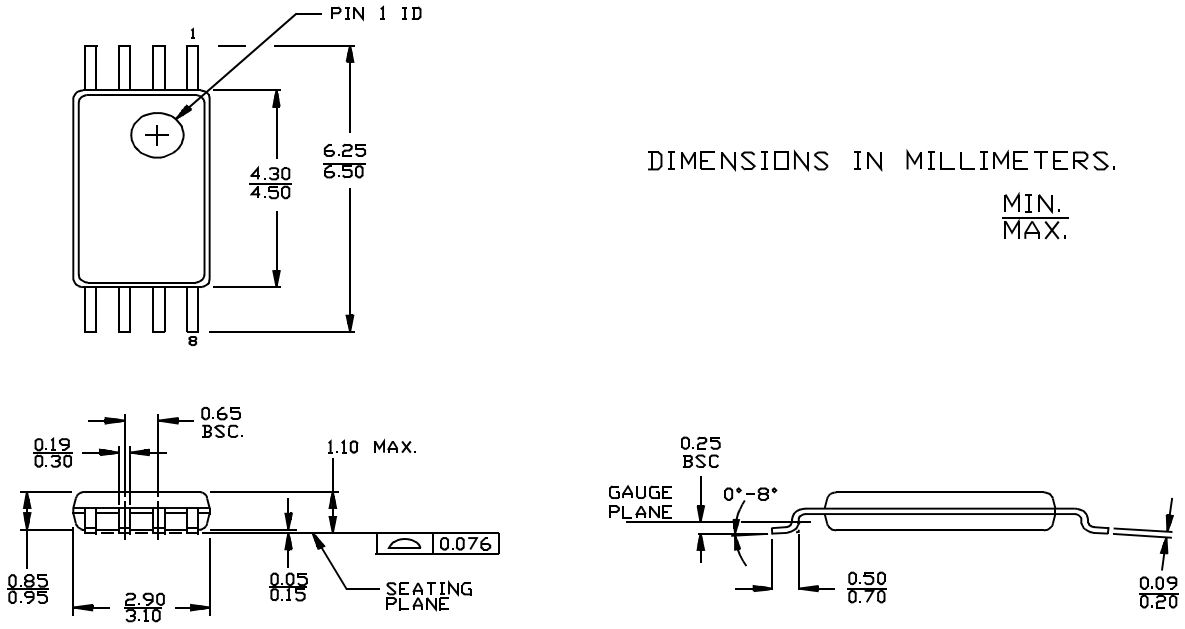



## Package Diagrams

**8-Lead (150-Mil) SOIC S8**




**8-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z8**

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