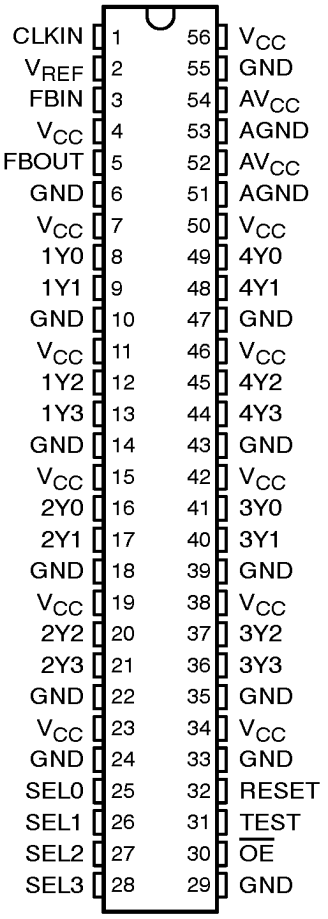
- **Low-Output Skew and Jitter for Clock Distribution and Synchronization**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to 16 Outputs**
- **Four Select Inputs Configure Output Frequency**
- **Internal Loop Filter Eliminates the Need for External RC Network**
- **Dedicated External Feedback Output and Input for Phase Synchronization With the Clock Input**
- **Applications for Synchronous DRAM, High-Speed Microprocessors, and SSTL_3 Applications**
- **LVTTL- or SSTL_3-Compatible Inputs and Outputs**
- **Distributed V_{CC} and GND Pin Configuration Minimize High-Speed Switching Noise**
- **Meets SSTL_3 Class 1 and 2 Specifications**
- **Packaged in 56-Pin Plastic Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The CDC2587 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. The CDC2587 operates at 3.3-V V_{CC} and provides LVTTL- or SSTL_3-compatible inputs and outputs. The CDC2587 operates at frequencies from 16.67 MHz to 150 MHz, and is ideally suited for high-speed microprocessor and synchronous DRAM applications. The CDC2587 provides integrated 25-Ω series damping resistors to improve signal integrity.

A dedicated feedback output (FBOUT) is used to synchronize the output clocks in frequency and phase to the CLKIN reference. Four banks of four outputs (1Yn, 2Yn, 3Yn, 4Yn) are configured to operate at specified ratios of the input frequency by four select (SELn) inputs . Selectable ratios of the input frequency are 1X, 2X, 3X, 1/2X, and 1/3X.

description (continued)

The output-enable ($\overline{OE}$) input provides control for the Y output banks. When $\overline{OE}$ is high, the outputs are in a high-impedance state. When $\overline{OE}$ is low, the outputs switch in accordance with the select inputs. RESET provides a master reset for the CDC2587 counter circuitry. This allows the outputs to be reset to a known state. TEST provides a bypass of the integrated PLL and divider circuitry. When TEST is high, CLKIN bypasses the PLL and is buffered directly to the outputs.

The loop filter components of the PLL are integrated on the CDC2587. This reduces the need for external loop components and provides an easily implemented PLL circuit. FBOUT should be connected to the feedback input (FBIN) for normal operation of the PLL.

The voltage-controlled oscillator (VCO) of the integrated PLL has an operating range of 100 MHz to 300 MHz. The VCO is designed to operate at two to twelve times the CLKIN frequency. This allows the CDC2587 to achieve output frequencies from 16.67 MHz to 150 MHz, with a duty cycle of 50% ± 5% ensured.

Independent analog V_{CC} (AV_{CC}) and ground (AGND) connections are provided for VCO stability.

CLKIN and FBIN can be configured to switch at SSTL_3 input levels by connecting V_{REF} to a nominal reference voltage of 1.5 V. If V_{REF} is strapped to GND, CLKIN and FBIN switch at normal TTL input thresholds.

Because the CDC2587 is based on PLL technology, it requires a stabilization time to achieve phase lock of the feedback signal to the CLKIN reference. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN. In addition, a stabilization time may be required, following changes to the SELn inputs, TEST inputs, or a change in frequency of CLKIN.

FUNCTION TABLE
(PLL enabled)

INPUTS							OUTPUTS				
$\overline{OE}$	SEL3	SEL2	SEL1	SEL0	F_{IN}min	F_{IN}max	FBOUT	1Y(0:3)	2Y(0:3)	3Y(0:3)	4Y(0:3)
H	X	X	X	X	Note 1	Note 1	Note 1	Hi Z	Hi Z	Hi Z	Hi Z
L	L	L	L	L	50 MHz	150 MHz	VCO/2	1X	1X	1X	1X
L	L	L	L	H	25 MHz	75 MHz	VCO/4	1X	1X	1X	2X
L	L	L	H	L	25 MHz	75 MHz	VCO/4	1X	1X	2X	2X
L	L	L	H	H	25 MHz	75 MHz	VCO/4	1X	2X	2X	2X
L	L	H	L	L	25 MHz	75 MHz	VCO/4	2X	2X	2X	2X
L	L	H	L	H	16.67 MHz	50 MHz	VCO/6	1X	1X	1X	3X
L	L	H	H	L	16.67 MHz	50 MHz	VCO/6	1X	1X	3X	3X
L	L	H	H	H	16.67 MHz	50 MHz	VCO/6	1X	3X	3X	3X
L	H	L	L	L	16.67 MHz	50 MHz	VCO/6	3X	3X	3X	3X
L	H	L	L	H	50 MHz	150 MHz	VCO/2	1X	1X	1X	1/2X
L	H	L	H	L	50 MHz	150 MHz	VCO/2	1X	1X	1/2X	1/2X
L	H	L	H	H	50 MHz	150 MHz	VCO/2	1X	1/2X	1/2X	1/2X
L	H	H	L	L	50 MHz	150 MHz	VCO/2	1/2X	1/2X	1/2X	1/2X
L	H	H	L	H	50 MHz	150 MHz	VCO/2	1X	1X	1X	1/3X
L	H	H	H	L	50 MHz	150 MHz	VCO/2	1X	1X	1/3X	1/3X
L	H	H	H	H	50 MHz	150 MHz	VCO/2	1X	1/3X	1/3X	1/3X

NOTE 1: Minimum and maximum input frequency and FBOUT frequency depend on the configuration of the SELn inputs.

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TEXAS INSTRUMENTS
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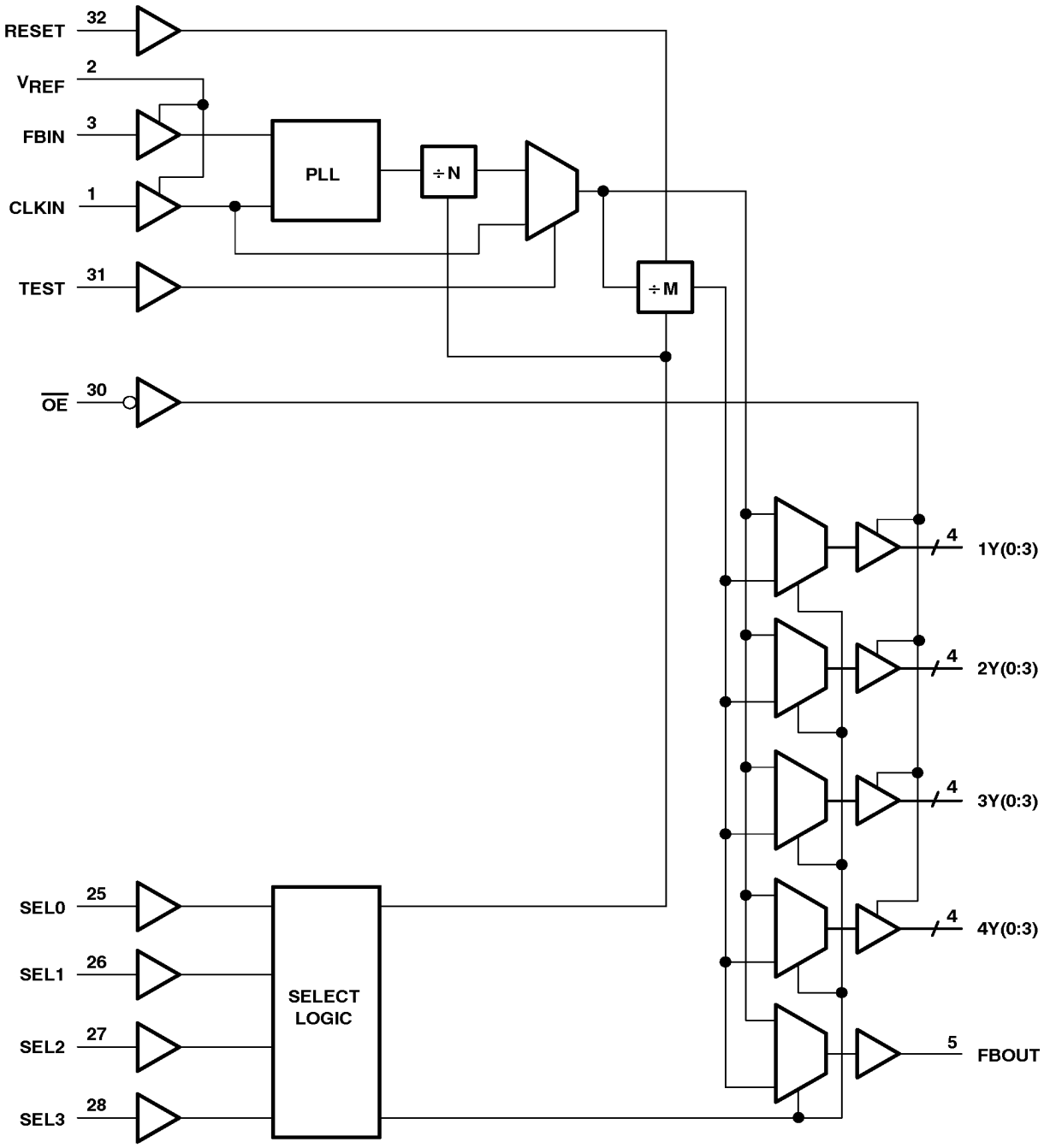
functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDC2587 clock-driver circuit. CLKIN is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	3	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN should be wired to FBOUT. The integrated PLL adjusts the output clocks to obtain zero phase delay between the FBIN and CLKIN inputs.
V_{REF}	2	I	Voltage reference. V_{REF} is the reference voltage required for SSTL operation. A nominal voltage of 1.5 V should be applied when SSTL operation of the CLKIN and FBIN signals is required. If V_{REF} is strapped to GND, CLKIN and FBIN operate at TTL switching levels.
$\overline{OE}$	30	I	Output enable. $\overline{OE}$ is the output enable for all of the Y outputs. When $\overline{OE}$ is low, all Y outputs are enabled. When $\overline{OE}$ is high, all Y outputs are in the high-impedance state. FBOUT is not disabled by $\overline{OE}$, therefore the PLL is not disrupted when placing the Y outputs into the high-impedance state.
TEST	31	I	Test input. TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the device is placed in a test mode that bypasses the PLL circuitry.
RESET	32	I	Reset input. RESET is used to reset the counter circuit that divides the VCO output frequency. Y outputs configured as fractional frequencies of the input signal may be reset to a known state. RESET is a negative-edge-triggered signal. When a high-to-low edge occurs at RESET, the counter that divides the VCO output signal is asynchronously cleared to a low level.
SEL(0:3)	28–25	I	Select inputs. SEL(0:3) configure the frequency of the Y outputs in banks of four.
1Y(0:3) 2Y(0:3) 3Y(0:3) 4Y(0:3)	8, 9, 12, 13 16, 17, 20, 21 36, 37, 40, 41 44, 45, 48, 49	O	Clock outputs. These output pins are configured by SEL(0:3) to transmit a multiple or fraction of the input frequency. The relationship between the CLKIN frequency and the output frequency is dependent on the select inputs. Due to normal operation of the PLL, the duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of CLKIN. All outputs provide integrated 25-Ω series-damping resistors to improve signal integrity at the load.
FBOUT	5	O	Feedback output. FBOUT is synchronized in phase and frequency to the input clock. FBOUT is not a 3-state output and is not disabled when $\overline{OE}$ is asserted low. A stabilization time is required on power up and the application of a fixed frequency, fixed-phase signal at CLKIN. In addition, the stabilization time may be required when changes occur to the input signal or the states of the SEL(0:3) control inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 2) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state
or power-off state, V_O (see Note 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 24 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) . . . . . 1.2 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book,* literature number SCBD002.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_{REF}	SSTL reference voltage		1.3	1.5	1.7	V
V_I	Input voltage		0		5.5	V
V_{IH}	High-level input voltage	CLKIN, FBIN	V_{REF}+100 mV			V
		CLKIN, FBIN (V_{REF} = GND)	2			
		Other inputs	2			
V_{IL}	Low-level input voltage	CLKIN, FBIN			V_{REF}–100 mV	V
		CLKIN, FBIN (V_{REF} = GND)			0.8	
		Other inputs			0.8	
I_{OH}	High-level output current				–12	mA
I_{OL}	Low-level output current				12	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V
	V_{CC} = 3 V,	I_{OH} = – 12 mA		2.4			
V_{OL}	V_{CC} = 3 V	I_{OL} = 100 µA				0.2	V
		I_{OL} = 12 mA				0.4	
I_I	V_{CC} = 0 or MAX‡,	V_I = 3.6 V,	V_{REF} = GND			±10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND,	V_{REF} = GND			±1	
		V_I = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0				–10	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0,	V_I = V_{CC} or GND,	V_{REF} = GND			1	mA
		V_I = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			1	
C_i	V_I = V_{CC} or GND,	V_{REF} = GND			3		pF
	V_I = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			3		
C_o	V_O = 3 V or 0,	V_{REF} = GND			6		pF
	V_O = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			6		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

			MIN	MAX	UNIT
fclock	Input clock frequency	VCO is operating at six times the CLKIN frequency	16.67	50	MHz
		VCO is operating at four times the CLKIN frequency	25	75	
		VCO is operating at two times the CLKIN frequency	50	150	
	Input clock duty cycle		40%	60%	
	Stabilization time†	After $\overline{OE}$↓		5	μs
		After SELn		5	
		After power up and CLKIN		5	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

NOTE 5: Preliminary specifications are based on SPICE analysis.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Note 6 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}					150	MHz
$t_{phase\ error}$	CLKIN↑	FBIN↑	–300		+300	ps
$t_{sk(o)}$ same frequency		Y			250	ps
$t_{sk(o)}$ different frequency					500	
Jitter (peak to peak)	CLKIN↑	Y↑	–75		+75	ps
Duty cycle		Y	45%		55%	
t_r						ns
t_f						ns

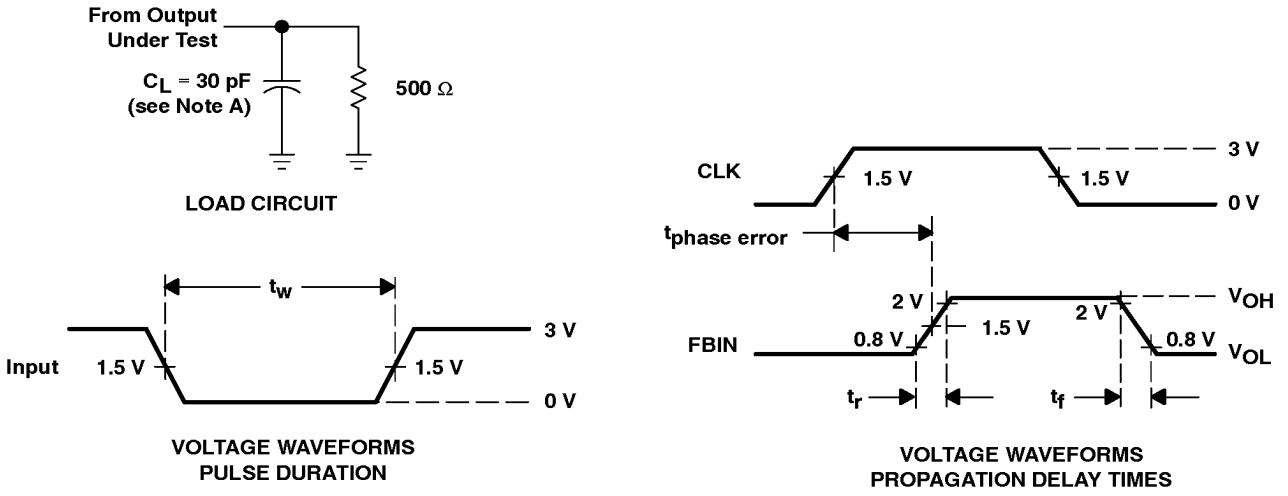
NOTE 6: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{REF} = V_{TT} = V_{CC} \times 0.45$, C_L = 30 pF (see Note 6 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}			150			MHz
$t_{phase\ error}$	CLKIN↑	FBIN↑	–300		+300	ps
$t_{sk(o)}$ same frequency		Y			250	ps
$t_{sk(o)}$ different frequency					500	
Jitter (peak to peak)	CLKIN↑	Y↑	–75		+75	ps
Duty cycle		Y	45%		55%	
t_r						ns
t_f						ns

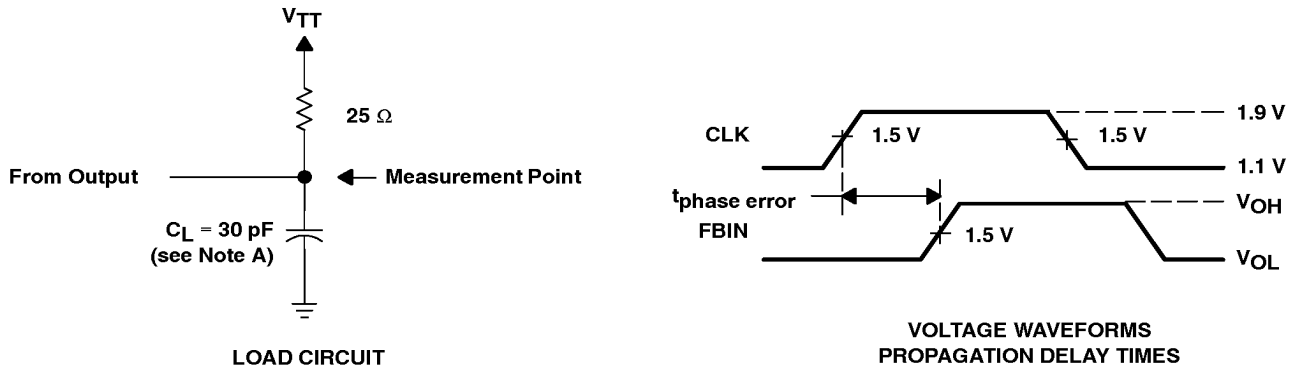
NOTE 6: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 150 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 150 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.
D. $V_{TT} = V_{REF} = V_{CC} \times 0.4$

Figure 2. Load Circuit and Voltage Waveforms for SSTL_3 Class 1

PRODUCT PREVIEW