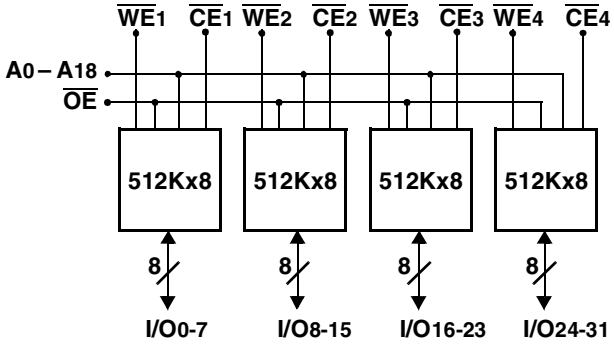
ACT–S512K32 High Speed
16 Megabit SRAM Multichip Module

Features

- 4 Low Power CMOS 512K x 8 SRAMs in one MCM
- Factory configured as 512K x 32; User configurable as 1M x 16 or 2M x 8
- Input and Output TTL & CMOS Compatible Design
- Fast 17,20,25,35,45,55ns Access Times
- Full Commercial, Industrial and Military (-55°C to +125°C) Temperature Range
- MIL-PRF-38534 Compliant MCMs Available
- +5 V Power Supply
- Available in two Surface Mount Packages, and two PGA Type Package
  - 68–Lead, Low Profile CQFP(F1), 1.56"SQ x .140"max
  - 68–Lead, Dual-Cavity CQFP(F2), 0.88"SQ x .20"max (.18 max thickness available, contact factory for details) *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
  - 68–Lead, Single-Cavity CQFP (F18), .94"SQ x .140"max *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
  - 66 Pin, 1.38" x 1.38" x .245" PGA Type, Aeroflex code# "P1"
  - 66 Pin, 1.09" x 1.09" x .185" PGA Type, With Shoulder, Aeroflex code# "P7"
- Internal Decoupling Capacitors
- DESC SMD# 5962–94611 Released (F1,F2,F18,P1,P7)

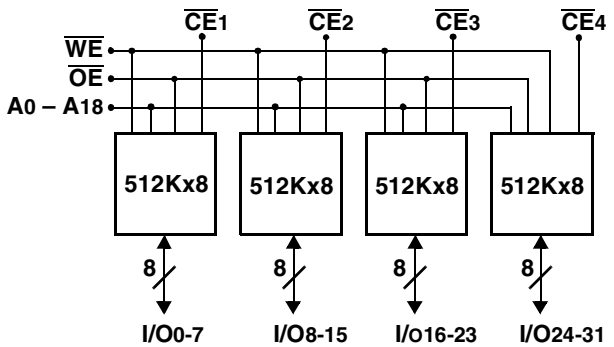
Block Diagram – PGA Type Package (P1,P7) & CQFP (F2,F18)



Pin Description

I/O0-31	Data I/O
A0–18	Address Inputs
WE1–4	Write Enables
CE1–4	Chip Enables
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

Block Diagram – CQFP(F1)



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General Description

The ACT–S512K32 is a High Speed, 16 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range industrial, military, or space, mass memory and fast cache applications.

The MCM can be organized as a 512K x 32 bit, 1M x 16 bit or 2M x 8 bit device and is input and output TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low and output enable ($\overline{OE}$) input is high. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are both low. Access time grades of 17ns, 20ns, 25ns, 35ns, 45ns and 55ns maximum are standard high speed versions.

The +5 Volt power supply version is standard and +3.3 Volt lower power model is a future optional product.

The products are designed for operation over the temperature range of -55°C to +125°C and under the full military environment. DESC Standard Military Drawing (SMD) numbers are released.

The ACT-S512K32 is manufactured in Aeroflex's 80,000 square foot MIL-PRF-38534 certified facility in Plainview, N.Y.

Absolute Maximum Ratings

Symbol	Rating	Range	Units
Tc	Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum Package Power Dissipation	3.0	W
$Ø_{J-C}$	Hottest Die, Max Thermal Resistance - Junction to Case	5	°C/W
V_G	Maximum Signal Voltage to Ground	-0.5 to +7	V
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V

Capacitance

(V_{IN} = 0V, f = 1MHz, Tc = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A_0 – A_{18} Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{WE}	CQFP (F1) Package	50	pF
	PGA (P1 & P7) and CQFP (F2 & F18) Packages	20	pF
C_{CE}	Chip Enable Capacitance	20	pF
$C_{I/O}$	I/O_0 – I/O_{31} Capacitance	20	pF

This parameter is guaranteed by design but not tested

DC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, Tc = -55°C to +125°C, unless otherwise indicated)

Parameter	Sym	Conditions	ALL Speeds Min	ALL Speeds Max	Units
Input Leakage Current	I_{LI}	V_{CC} = +5.5V, V_{IN} = 0 or V_{CC}	-	10	µA
Output Leakage Current	I_{LO}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = 0 to V_{CC}	-	10	µA
Operating Supply Current 32 Bit Mode	I_{CC1}x32	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{CC} = +5.5V f = 5 MHz CMOS Compatible	-	600	mA
Standby Current	I_{SB1}	$\overline{CE}$ = V_{CC}, $\overline{OE}$ = V_{IH}, V_{CC} = +5.5V f = 5 MHz CMOS Compatible	-	80	mA
Operating Supply Current 32 Bit Mode	I_{CC2}x32	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{CC} = +5.5V f = 50 MHz CMOS Compatible	-	700	mA
Standby Current	I_{SB2}	$\overline{CE}$ = V_{CC}, $\overline{OE}$ = V_{IH}, V_{CC} = +5.5V f = 50 MHz CMOS Compatible	-	280	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = +4.5V	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA, V_{CC} = +4.5V	2.4	-	V

AC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, Tc = -55°C to +125°C)

Read Cycle

Parameter	Sym	–017		–020		–025		–035		–045		–055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17	-	20	-	25		35	-	45	-	55	-	ns
Address Access Time	t_{AA}	-	17	-	20	-	25	-	35	-	45	-	55	ns
Chip Enable Access Time	t_{ACE}	-	17	-	20	-	25	-	35	-	45	-	55	ns
Output Hold from Address Change	t_{OH}	0	-	0		0	-	0		0	-	0	-	ns
Output Enable to Output Valid	t_{OE}	-	9	-	10	-	12		25	-	25		25	ns
Chip Enable to Output in Low Z *	t_{CLZ}	2	-	2		2	-	4		4	-	4	-	ns
Output Enable to Output in Low Z *	t_{OLZ}	0	-	0		0	-	0		0	-	0	-	ns
Chip Deselect to Output in High Z *	t_{CHZ}	-	12	-	12	-	12	-	15	-	20	-	20	ns
Output Disable to Output in High Z *	t_{OHZ}	-	12	-	12	-	12	-	15	-	20	-	20	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Sym	–017		–020		–025		–035		–045		–055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17	-	20	-	25	-	35	-	45	-	55	-	ns
Chip Enable to End of Write	t_{CW}	15	-	15	-	17	-	25	-	35	-	50	-	ns
Address Valid to End of Write	t_{AW}	15	-	15	-	17	-	25	-	35	-	50	-	ns
Data Valid to End of Write	t_{DW}	11	-	12	-	13	-	20	-	25	-	25	-	ns
Write Pulse Width	t_{WP}	15	-	15	-	17	-	25	-	35	-	40	-	ns
Address Setup Time	t_{AS}	2	-	2	-	2	-	2	-	2	-	2	-	ns
Output Active from End of Write *	t_{OW}	2	-	3	-	4	-	4	-	5	-	5	-	ns
Write to Output in High Z *	t_{WHZ}	-	9		11		13		15		20	-	20	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	0	-	0	-	ns
Address Hold Time	t_{AH}	0	-	0	-	0	-	0	-	5	-	5	-	ns

* Parameters guaranteed by design but not tested

Data Retention Electrical Characteristics (Special Order Only)

(Tc = -55°C to +125°C)

Parameter	Sym	Test Conditions	All Speeds		Units
			Min	Max	
V_{CC} for Data Retention	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2	5.5	**V**
Data Retention Current	I_{CCDR1}	V_{CC} = 3V	-	28	mA

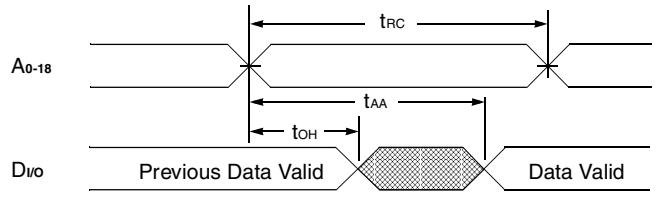
Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Output Disable	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

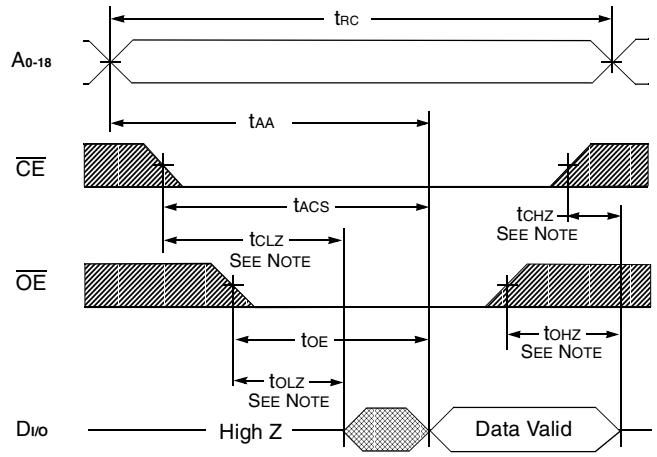
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

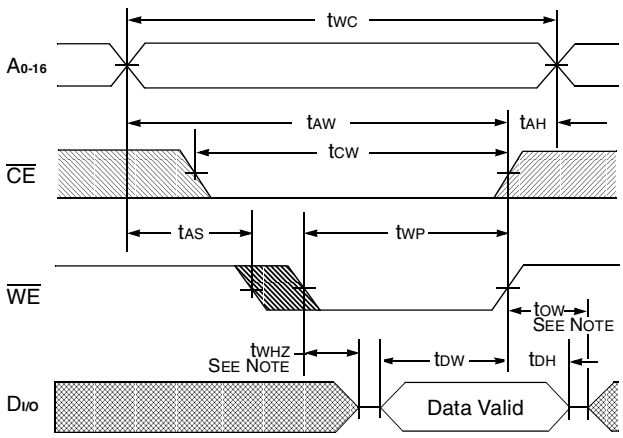


Read Cycle 2 ($\overline{WE}$ = V_{IH})

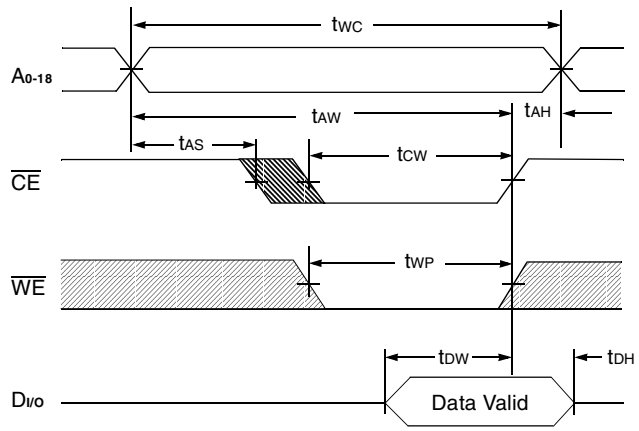


Write Cycle Timing Diagrams

Write Cycle 1 ($\overline{WE}$ Controlled, $\overline{OE}$ = V_{IL})

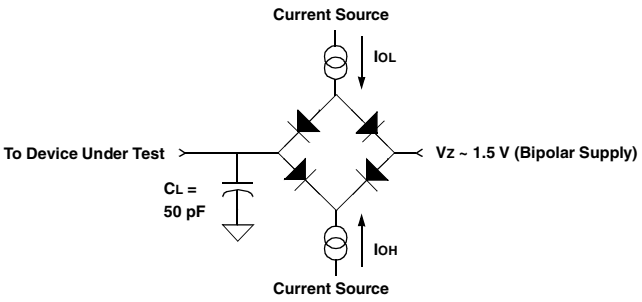


Write Cycle 2 ($\overline{CE}$ Controlled, $\overline{OE}$ = V_{IH})



Note: Guaranteed by design, but not tested.

AC Test Circuit



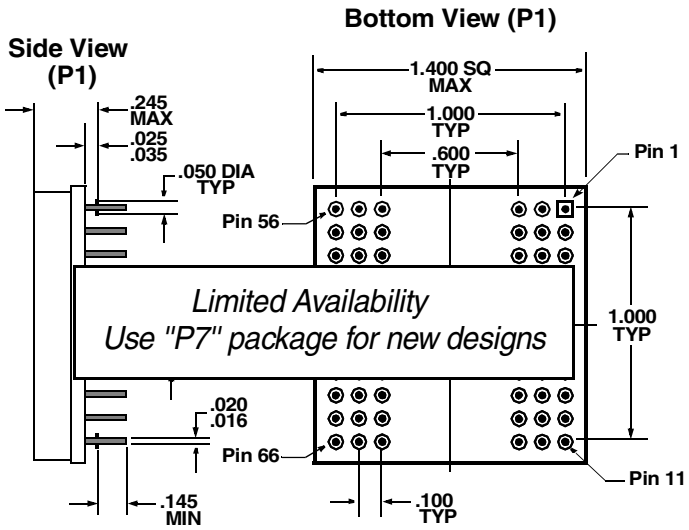
Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

Notes:
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance Z_O = 75Ω. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

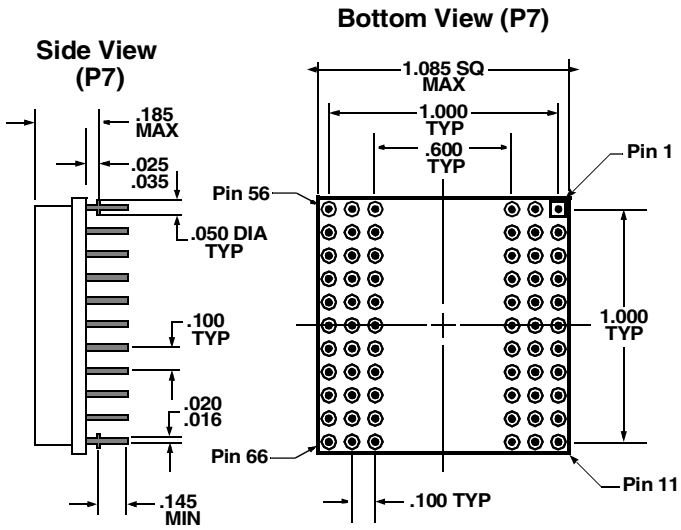
Pin Numbers & Functions

66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O_8	18	A_{12}	35	I/O_{25}	52	$\overline{WE}_3$
2	I/O_9	19	Vcc	36	I/O_{26}	53	$\overline{CE}_3$
3	I/O_{10}	20	$\overline{CE}_1$	37	A_6	54	GND
4	A_{13}	21	NC	38	A_7	55	I/O_{19}
5	A_{14}	22	I/O_3	39	NC	56	I/O_{31}
6	A_{15}	23	I/O_{15}	40	A_8	57	I/O_{30}
7	A_{16}	24	I/O_{14}	41	A_9	58	I/O_{29}
8	A_{17}	25	I/O_{13}	42	I/O_{16}	59	I/O_{28}
9	I/O_0	26	I/O_{12}	43	I/O_{17}	60	A_0
10	I/O_1	27	$\overline{OE}$	44	I/O_{18}	61	A_1
11	I/O_2	28	A_{18}	45	V_{CC}	62	A_2
12	$\overline{WE}_2$	29	$\overline{WE}_1$	46	$\overline{CE}_4$	63	I/O_{23}
13	$\overline{CE}_2$	30	I/O_7	47	$\overline{WE}_4$	64	I/O_{22}
14	GND	31	I/O_6	48	I/O_{27}	65	I/O_{21}
15	I/O_{11}	32	I/O_5	49	A_3	66	I/O_{20}
16	A_{10}	33	I/O_4	50	A_4		
17	A_{11}	34	I/O_{24}	51	A_5		

Package Outline — PGA-Type "P1"



Package Outline — PGA-Type "P7"

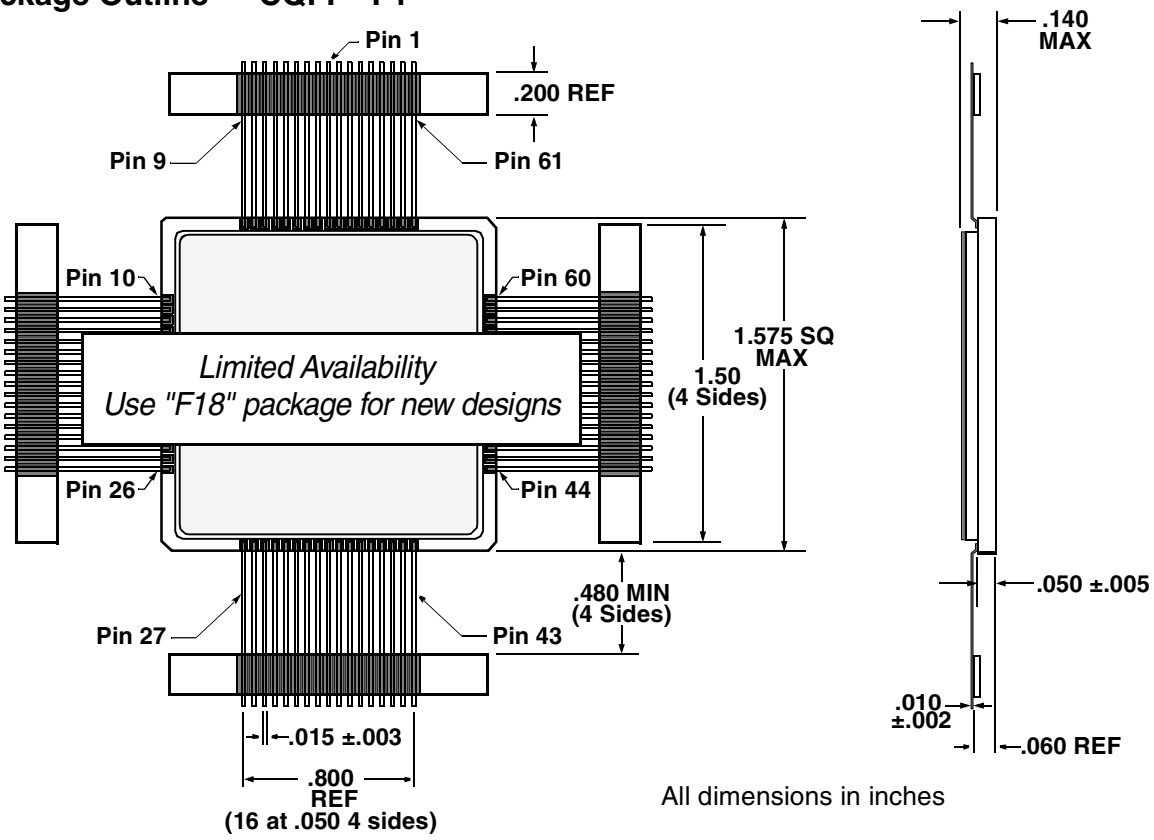


All dimensions in inches

Pin Numbers & Functions

68 Pins — CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_1$	19	I/O_8	36	$\overline{CE}_4$	53	I/O_{23}
3	A_5	20	I/O_9	37	A_{17}	54	I/O_{22}
4	A_4	21	I/O_{10}	38	A_{18}	55	I/O_{21}
5	A_3	22	I/O_{11}	39	NC	56	I/O_{20}
6	A_2	23	I/O_{12}	40	NC	57	I/O_{19}
7	A_1	24	I/O_{13}	41	NC	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE}$
17	I/O_7	34	$\overline{CE}_2$	51	I/O_{24}	68	$\overline{CE}_3$

Package Outline — CQFP "F1"



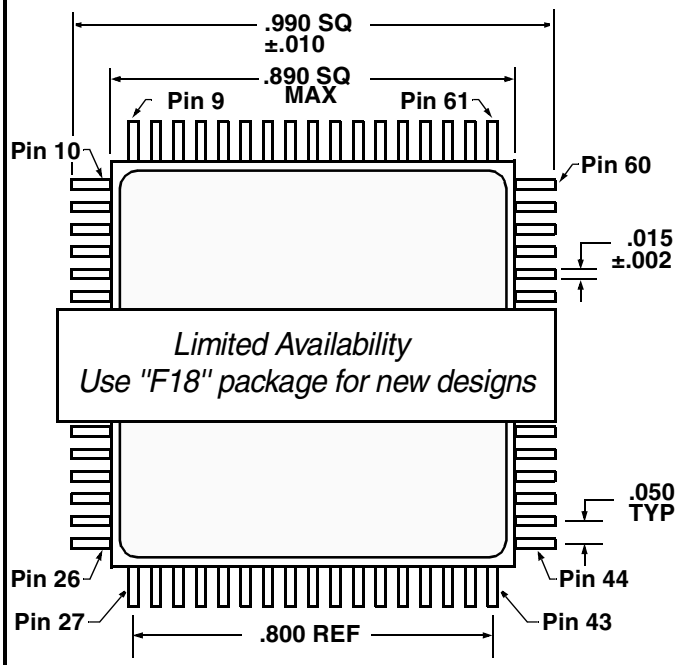
All dimensions in inches

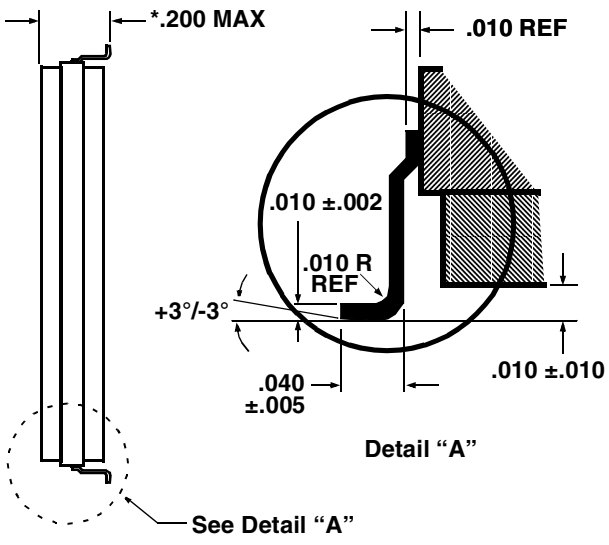
Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	A_{17}	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$\overline{WE}_2$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	$\overline{WE}_3$	56	I/O_{20}
6	A_2	23	I/O_{12}	40	$\overline{WE}_4$	57	I/O_{19}
7	A_1	24	I/O_{13}	41	A_{18}	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE1}$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

Package Outline — Dual-Cavity CQFP "F2"

Top View





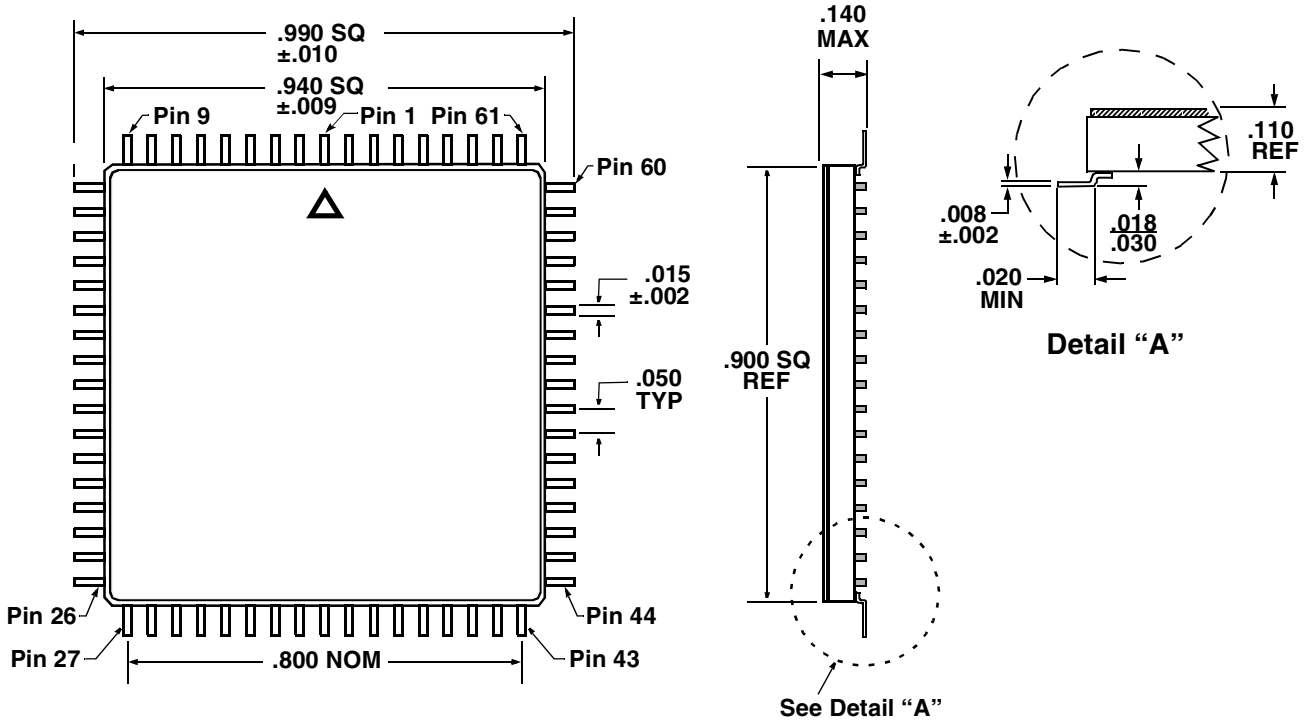
***.180 MAX available, call factory for details**

All dimensions in inches

Pin Numbers & Functions

68 Pins — Single-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	A_{17}	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$\overline{WE}_2$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	$\overline{WE}_3$	56	I/O_{20}
6	A_2	23	I/O_{12}	40	$\overline{WE}_4$	57	I/O_{19}
7	A_1	24	I/O_{13}	41	A_{18}	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE1}$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

Package Outline — CQFP Single Cavity "F18"



All dimensions in inches

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Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT–S512K32N–017F1Q	5962–9461110HYC	17ns	1.56"sq CQFP
ACT–S512K32N–020F1Q	5962–9461109HYC	20ns	1.56"sq CQFP
ACT–S512K32N–025F1Q	5962–9461108HYC	25ns	1.56"sq CQFP
ACT–S512K32N–034F1Q	5962–9461107HYC	35ns	1.56"sq CQFP
ACT–S512K32N–045F1Q	5962–9461106HYC	45ns	1.56"sq CQFP
ACT–S512K32N–055F1Q	5962–9461105HYC	55ns	1.56"sq CQFP
ACT–S512K32N–017F2Q	5962–9461110HMC	17ns	.88"sq CQFP
ACT–S512K32N–020F2Q	5962–9461109HMC	20ns	.88"sq CQFP
ACT–S512K32N–025F2Q	5962–9461108HMC	25ns	.88"sq CQFP
ACT–S512K32N–035F2Q	5962–9461107HMC	35ns	.88"sq CQFP
ACT–S512K32N–045F2Q	5962–9461106HMC	45ns	.88"sq CQFP
ACT–S512K32N–055F2Q	5962–9461105HMC	55ns	.88"sq CQFP
ACT–S512K32N–017F18Q	5962–9461110H9C	17ns	.94"sq CQFP
ACT–S512K32N–020F18Q	5962–9461109H9C	20ns	.94"sq CQFP
ACT–S512K32N–025F18Q	5962–9461108H9C	25ns	.94"sq CQFP
ACT–S512K32N–035F18Q	5962–9461107H9C	35ns	.94"sq CQFP
ACT–S512K32N–045F18Q	5962–9461106H9C	45ns	.94"sq CQFP
ACT–S512K32N–055F18Q	5962–9461105H9C	55ns	.94"sq CQFP
ACT–S512K32N–017P1Q	5962–9461110HXC	17ns	1.38"sq PGA-Type
ACT–S512K32N–020P1Q	5962–9461109HXC	20ns	1.38"sq PGA-Type
ACT–S512K32N–025P1Q	5962–9461108HXC	25ns	1.38"sq PGA-Type
ACT–S512K32N–035P1Q	5962–9461107HXC	35ns	1.38"sq PGA-Type
ACT–S512K32N–045P1Q	5962–9461106HXC	45ns	1.38"sq PGA-Type
ACT–S512K32N–055P1Q	5962–9461105HXC	55ns	1.38"sq PGA-Type
ACT–S512K32N–017P7Q	5962–9461110HTC	17ns	1.09"sq PGA-Type
ACT–S512K32N–020P7Q	5962–9461109HTC	20ns	1.09"sq PGA-Type
ACT–S512K32N–025P7Q	5962–9461108HTC	25ns	1.09"sq PGA-Type
ACT–S512K32N–035P7Q	5962–9461107HTC	35ns	1.09"sq PGA-Type
ACT–S512K32N–045P7Q	5962–9461106HTC	45ns	1.09"sq PGA-Type
ACT–S512K32N–055P7Q	5962–9461105HTC	55ns	1.09"sq PGA-Type

Model Number Breakdown

ACT– S 512K 32 N– 020 F18 Q

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Memory Type
S = SRAM

Memory Depth, Locations

Memory Width, Bits

Pinout Options
N = None

Memory Speed, ns

Screening
C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screened *
Q = MIL-PRF-38534 Compliant/SMD

* **Screened to the individual test methods of MIL-STD-883**

Package Type & Size

Surface Mount Packages	*Thru-Hole Packages*
F1 = 1.56"SQ 68 Pin CQFP	P1 = 1.385"SQ PGA 66 Pins
F2 = .88"SQ 68 Pin Dual-Cavity CQFP	P7 = 1.085"SQ PGA 66 Pins
F18 = .94"SQ 68 Leads CQFP Single-Cavity Low Profile	

Specification subject to change without notice

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