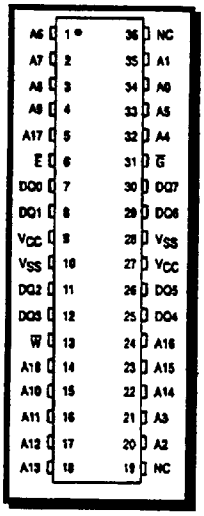
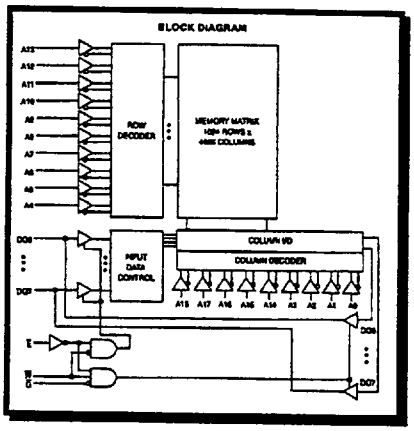
Radiation Hardened 32C408ARP

4 Megabit SRAM - CMOS 512K x 8 bit Static RAM



PIN NAMES	
A0 -A18	Address Inputs
W\	Write Enable
G\	Output Enable
E\	Chip Enable
DQ0-DQ7	Data Input / Output
NC	No Connection
Vcc	+ 5V Power Supply
Vss	Ground



- 524,288 x 8 bit Organization
- Industry Standard Pinout
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness > 100 Krad (Si)
- Single Event Effects:
  SEL_{TH} LET: >108 MeV/mg/cm^2
  SEU_{TH} LET: 2.3 MeV/mg/cm^2
- Package : 36 Pin RAD-PAK® flat pack
- Fast Access Time: 25 / 35 ns Maximum Times Available
- Completely Static Memory - No clock or timing strobe required
- High Speed silicon - gate CMOS Technology
- Single 5V ± 10% power supply
- Equal Address and Chip Enable access times
- Three-State Outputs
- All Inputs and outputs are TTL compatible
- Low Power operation:
  185/170 mA Maximum, Active AC
  50/40 mA Maximum, Standby AC
- Screening per TM 5004
- QCI per TM 5005

SEi's 32C408ARP (RP for RAD-PAK®) high density 4 megabit SRAM microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEi's radiation hardened RAD-PAK® packaging technology, the 32C408ARP is fully compatible with the industry standard pinout and architecture. It realizes a higher density and power consumption by employing a high-performance silicon-gate CMOS process technology. Capable of surviving space environments, the 32C408ARP is ideal for satellite, spacecraft, and space probe missions.

RAD-PAK® incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. The 32C408ARP features the same advanced 512K x 8 SRAM, high speed, and low power demand as the commercial counterpart. This product is available in Class S packaging and screening.

TQM
Total Quality Management

Specifications and design are subject to change without notice.

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32C408ARP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power Supply Voltage Relative to Vss	V_{CC}	-0.5	+7.0	V
Voltage Relative to Vss for Any Pin Except Vcc	V_{IN}, V_{OUT}	-0.5	+0.5	V
Output Current (per I/O)	I_{OUT}	-20	+20	mA
Power Dissipation	P_D		1.1	W
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{stg}	-65	+150	°C

32C408ARP RECOMMENDED OPERATING CONDITIONS
(Vcc = 5.0 V ±10%, T_A = -55 to +125°C, Unless Otherwise Noted)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage, (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	Vcc +0.3[1]	V
Input Low Voltage	V_{IL}	-0.5[2]	0.8	V

Note:
[1] V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0ns).
[2] V_{IL} (min) = -0.5 V dc; V_{IL} (min) = -2.0 V ac (pulse width ≤ 2.0ns).

TRUTH TABLE
(X = Don't Care)

E\	G\	W\	Mode	I/O Pin	Cycle	Current
H	X	X	Not selected	High-Z		Isb1, Isb2
L	H	H	Output Disabled	High-Z		Icca
L	L	H	Read	Dout	Read	Icca
L	X	L	Write	High-Z	Write	Icca

CAPACITANCE
(f =1.0 MHz, dV =3.0 V, T_A =25°C)

PARAMETER	SYMBOL	TYP.	MAX	Unit
Input Capacitance All Inputs (except Clocks and DQs)	C_{in}	4	6	pF
E\, G\, W\	C_{ck}	5	8	
I/O Capacitance DQ	$C_{I/O}$	5	8	pF

32C408ARP DC CHARACTERISTICS AND POWER SUPPLY CURRENTS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Leakage Current (all inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$		±1.0	µA
Output Leakage Current (E\[1] = V_{IH}, V_{OUT} = 0 to V_{CC})	$I_{lkg(O)}$		±1.0	µA
AC Active Supply Current (I_{out} = 0.0mA, V_{CC} = max) 32C408ARP-25 32C408ARP-35	I_{CC}		185 170	mA
AC Standby Current (V_{CC} = max, E\[1] = V_{IH}, No other restrictions on other inputs 32C408ARP 32C408ARP	I_{SB1}		50 40	mA
CMOS Standby Current (E\[1] ≥ V_{CC} -0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} - 0.2, V_{CC} = max, f = 0.0 MHz)	I_{SB2}		15	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -4.0 mA)	V_{OH}	2.4		V

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AC OPERATING CODITIONS AND CHARACTERISTICS

(Vcc = 5.0 V ±10%, T_A = -55 to +125°C, Unless Otherwise Noted)

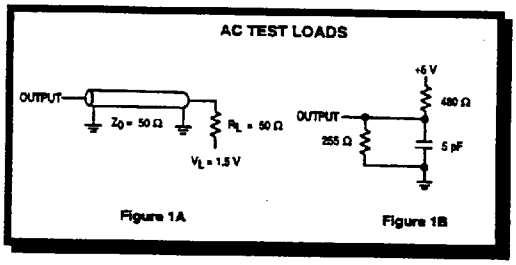
Input Pulse Level	0 to 3.0V
Output Timing Measurement Reference Level	1.5V
Input Rise/Fall Time	2ns
Input Timing Measurement Reference Level	1.5V
Output Load	See Figure 1A

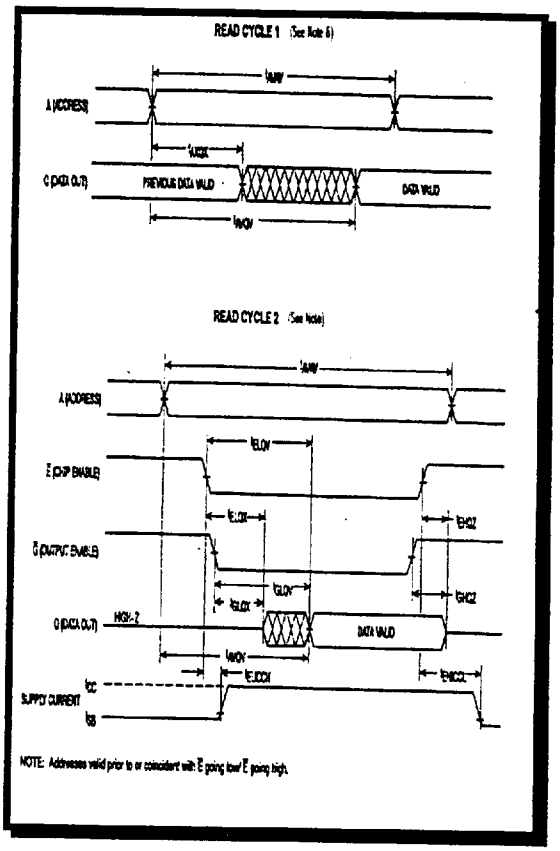
32C408ARP - READ CYCLE

(Vcc = 5.0 V ±10%, T_A = -55 to +125°C, Unless Otherwise Noted)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Read Cycle Time[2,3] 32C408ARP-25 32C408ARP-35	t_{AVAV}	 25 35		ns
Address Access Time 32C408ARP-25 32C408ARP-35	t_{AVQV}		 25 35	ns
Enable Access Time [4] 32C408ARP-25 32C408ARP-35	t_{ELQV}		 25 35	ns
Output Enable Access Time 32C408ARP-25 32C408ARP-35	t_{GLQV}		 8 10	ns
Output Hold from Address Change 32C408ARP-25 32C408ARP-35	t_{AXQX}	 5 5		ns
Enable Low to Output Active[5,6,7] 32C408ARP-25 32C408ARP-35	t_{ELQX}	 5 5		ns
Output Enable Low to Output Active[5,6,7] 32C408ARP-25 32C408ARP-35	t_{GLQX}	 0 0		ns
Enable High to Output High-Z[5,6,7] 32C408ARP-25 32C408ARP-35	t_{EHQZ}	 0 0	 10 12	ns
Output EnableHigh toOutput High-Z[5,6,7] 32C408ARP-25 32C408ARP-35	t_{GHQZ}	 0 0	 10 12	ns
Power Up Time 32C408ARP-25 32C408ARP-35	t_{ELICCH}	 0 0		ns
Power Down Time 32C408ARP-25 32C408ARP-35	t_{EHICCL}		 25 35	ns

1. W\ is high for the read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.





4. Addresses valid prior to or coincidend with E\ going low\ E\ going high.
5. AT any given voltage and temperature, $t_{EHQZ}^{MAX} < t_{ELQX}^{MIN}$, and $t_{GHQZ}^{MAX} < t_{GLQX}^{MIN}$, both for a given device and from device to device.
6. Transition is measured ± 500mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected (E\ ≤V_{IL}, G\ ≤V_{IL})

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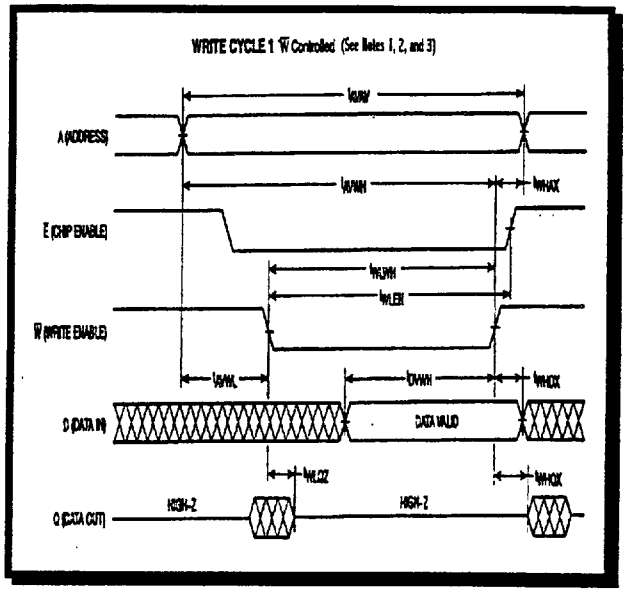
32C408ARP - WRITE CYCLE 1
(W/ Controlled, See Notes [1,2,3])

PARAMETER	SYMBOL	MIN	MAX	UNIT
Write Cycle Time[4] 32C408ARP-25 32C408ARP-35	t_{AVAV}	 25 35		ns
Address Setup Time 32C408ARP-25 32C408ARP-35	t_{AVWL}	 0 0		ns
Address Valid to End of Write 32C408ARP-25 32C408ARP-35	t_{AVWH}	 17 20		ns
Write Pulse Width 32C408ARP-25 32C408ARP-35	t_{WLWH} t_{WLEH}	 17 20		ns
Data Valid to End of Write 32C408ARP-25 32C408ARP-35	t_{DVWH}	 10 15		ns
Data Hold Time 32C408ARP-25 32C408ARP-35	t_{WHDX}	 0 0		ns
Write Low to Data High-Z[5,6,7] 32C408ARP-25 32C408ARP-35	t_{WLQZ}	 0 0	 10 15	ns
Write High to Output Active[5,6,7] 32C408ARP-25 32C408ARP-35	t_{WHQX}	 5 5		ns
Write Recovery Time 32C408ARP-25 32C408ARP-35	t_{WHAX}	 0 0		ns



NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

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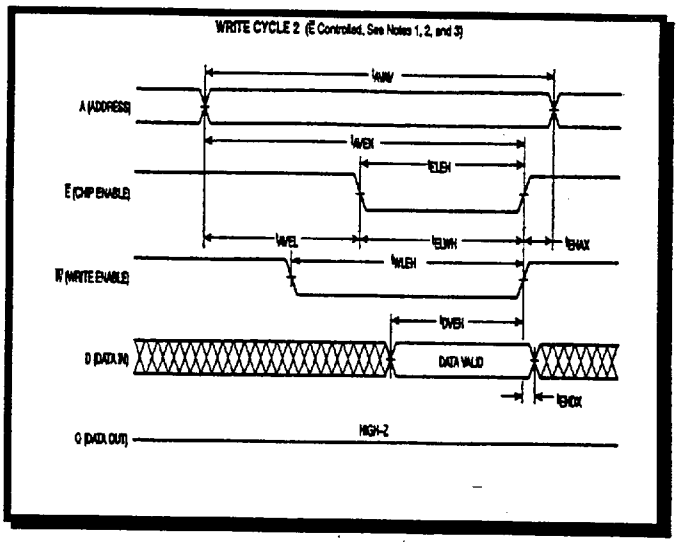
32C408ARP - WRITE CYCLE 2
(E/ Controlled, See Notes [1,2,3])

PARAMETER	SYMBOL	MIN	MAX	UNIT
Write Cycle Time[4] 32C408ARP-25 32C408ARP-35	t_{AVAV}	25 35		ns
Address Setup Time 32C408ARP-25 32C408ARP-35	t_{AVEL}	0 0		ns
Address Valid to End of Write 32C408ARP-25 32C408ARP-35	t_{AVEH}	 17 20		ns
Enable to End of Write[5,6] 32C408ARP-25 32C408ARP-35	t_{ELEH}, t_{ELWH}	 17 20		ns
Write Pulse Width 32C408ARP-25 32C408ARP-35	t_{WLEH}	17 20		ns
Data Valid to End of Write 32C408ARP-25 32C408ARP-35	t_{DVEH}	 10 15		ns
Data Hold Time 32C408ARP-25 32C408ARP-35	t_{EHDX}	0 0		ns
Write Recovery Time 32C408ARP-25 32C408ARP-35	t_{EHAX}	0 0		ns



NOTES:

1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

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