Winbond Electronics Corp.

128K × 16 CMOS FLASH MEMORY

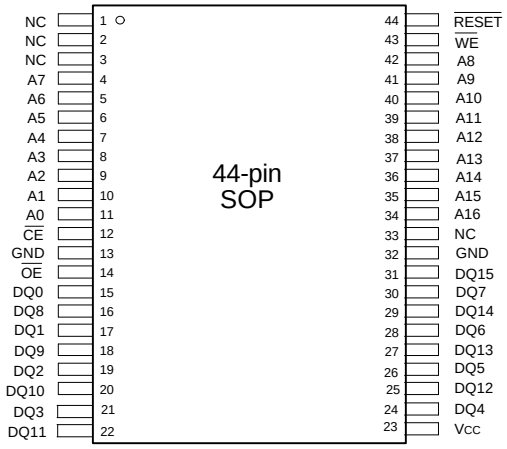
GENERAL DESCRIPTION

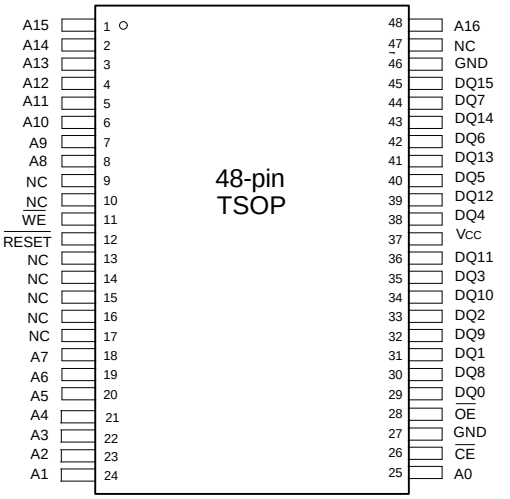
The W49F201 is a 2-megabit, 5-volt only CMOS flash memory organized as 128K × 16 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W49F201 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

FEATURES

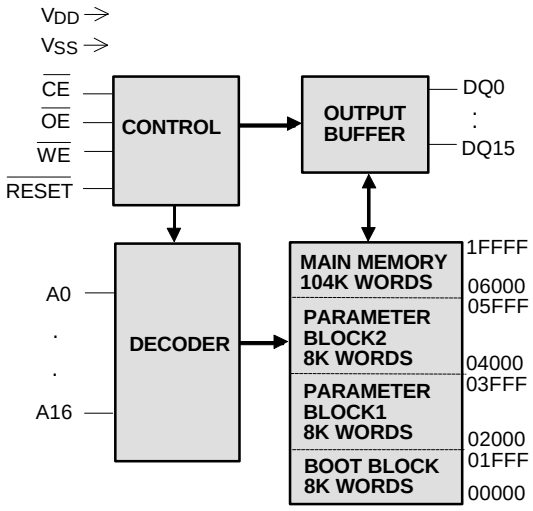
- Single 5-volt operations:
  - 5-volt Read/Erase/Program
- Fast Program operation:
  - Word-by-Word programming: 50 µS (max.)
- Fast Erase operation: 60 mS (typ.)
- Fast Read access time: 45/55 nS
- Endurance: 1K/10K cycles (typ.)
- Ten-year data retention
- Hardware data protection
- Sector configuration
  - One 8K words boot block with lockout protection
  - Two 8K words parameter blocks
  - One 104K words (208K bytes) Main Memory Array Blocks
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 µA (typ.)
- Automatic program and erase timing with internal V_{PP} generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard word-wide pinouts
- Available packages: 44-pin SOP, 48-pin TSOP

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
$\overline{RESET}$	Reset
A0–A16	Address Inputs
DQ0–DQ15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
VDD	Power Supply
GND	Ground
NC	No Connection

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W49F201 is controlled by $\overline{CE}$ and $\overline{OE}$, both of which have to be low for the host to obtain data from the outputs. $\overline{CE}$ is used for device selection. When $\overline{CE}$ is high, the chip is de-selected and only standby power will be consumed. $\overline{OE}$ is the output control and is used to gate data to the output pins. The data bus is in high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. Refer to the timing waveforms for further details.

Reset Operation

The $\overline{RESET}$ input pin can be used in some application. When $\overline{RESET}$ pin is at high state, the device is in normal operation mode. When $\overline{RESET}$ pin is driven low for at least a period of T_{RP}, it will halts the device and all outputs are at high impedance state. The device also resets the internal state machine to read array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence to assure data integrity. As the high state re-asserted to the $\overline{RESET}$ pin, the device will return to read or standby mode, it depends on the control signals. The system can read data T_{RH} after the $\overline{RESET}$ pin returns to V_{IH}. The other function for $\overline{RESET}$ pin is temporary reset the boot block. By applying the 12V to $\overline{RESET}$ pin, the boot block can be reprogrammed even though the boot block lockout function is enabled.

Boot Block Operation

There is one 8K-word boot block in this device, which can be used to store boot code. It is located in the first 8K words of the memory with the address range from 0000(hex) to 1FFF(hex).

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout); other memory locations can be changed by the regular programming method.

There is one condition that the lockout feature can be overrides. Just apply 12V to $\overline{RESET}$ pin, the lockout feature will temporary be inactivated and the boot block can be erased/programmed. Once the $\overline{RESET}$ pin returns to TTL level, the lockout feature will be activated again.

In order to detect whether the boot block feature is set on the 8K-words block, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "0002 hex". If the output data in DQ0 is "1", the boot block programming lockout feature is activated; if the output data in DQ0 is "0", the lockout feature is inactivated and the block can be erased/programmed.

To return to normal operation, perform a three-byte command sequence (or an alternate single-word command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Chip Erase Operation

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be

completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. The entire memory array will be erased to FF(hex). by the chip erase operation if the boot block programming lockout feature is not activated. Once the boot block lockout feature is activated, the chip erase function will erase all the sectors except the boot mode.

Sector Erase Operation

The three sectors, main memory and two parameters blocks, can be erased individually by initiating a six-word command sequence. Sector address is latched on the falling WE edge of the sixth cycle while the 30(hex) data input command is latched at the rising edge of WE. After the command loading cycle, the device enters the internal sector erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

When the boot block lockout feature is inactivated, the boot block and the main memory block will be erased together. Once the boot block is locked, only the main memory block will be erased by the execution of sector erase operation.

Program Operation

The W49F201 is programmed on a word-by-word basis. Program operation can only change logical data "1" to logical data "0" The erase operation (changed entire data in main memory and/or boot block from "0" to "1" is needed before programming.

The program operation is initiated by a 4-word command cycle (see Command Codes for Word Programming). The device will internally enter the program operation immediately after the word-program command is entered. The internal program timer will automatically time-out (50 μS max. - T_{BP}) once completed and return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

Hardware Data Protection

The integrity of the data stored in the W49F201 is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A $\overline{WE}$ pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming operation is inhibited when V_{DD} is less than 2.5V typical.

(3) Write Inhibit Mode: Forcing $\overline{OE}$ low, $\overline{CE}$ high, or $\overline{WE}$ high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

Data Polling (DQ_7)- Write Status Detection

The W49F201 includes a data polling feature to indicate the end of a program or erase cycle. When the W49F201 is in the internal program or erase cycle, any attempt to read DQ_7 of the last word loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ_7 will show the true data. Note that DQ_7 will show logical "0" during the erase cycle, and become logical "1" or true data when the erase cycle has been completed.

Toggle Bit (DQ6)- Write Status Detection

In addition to data polling, the W49F201 provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-word (or JEDEC 3-word) command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code, 00DA(hex). A read from address 0001(hex) outputs the device code, 00AE(hex). The product ID operation can be terminated by a three-word command sequence or an alternative one-word command sequence (see Command Definition table).

In the hardware access mode, access to the product ID is activated by forcing $\overline{CE}$ and $\overline{OE}$ low, $\overline{WE}$ high, and raising A9 to 12 volts.

TABLE OF OPERATING MODES

Operating Mode Selection

(V_{HH} = 12V ±5 %)

MODE	PINS					
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	ADDRESS	DQ.
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A_{IN}	Dout
Erase/Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	A_{IN}	Din
Standby	V_{IH}	X	X	V_{IH}	X	High Z
Erase/Program	X	V_{IL}	X	V_{IH}	X	High Z/D_{OUT}
Inhibit	X	X	V_{IH}	V_{IH}	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	V_{IH}	X	High Z
Product ID	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A0 = V_{IL}; A1–A15 = V_{IL}; A9 = V_{HH}	Manufacturer Code 00DA (Hex)
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A0 = V_{IH}; A1–A15 = V_{IL}; A9 = V_{HH}	Device Code 00AE (Hex)
Reset	X	X	X	V_{IL}	X	High Z

TABLE OF COMMAND DEFINITION

COMMAND DESCRIPTION	NO. OF Cycles	1ST CYCLE	2ND CYCLE	3RD CYCLE	4TH CYCLE	5TH CYCLE	6TH CYCLE
		Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data
Read	1	A_{IN} D_{OUT}					
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10
Main Memory Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	SA 30
Word Program	4	5555 AA	2AAA 55	5555 A0	A_{IN} D_{IN}		
Boot Block Lockout	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 40
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit (1)	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit (1)	1	XXXX F0					

Notes:

1. Address Format: A14–A0 (Hex); Data Format: DQ15–DQ8 (Don't Care); DQ7-DQ0 (Hex)

2. Either one of the two Product ID Exit commands can be used.

3. SA: Sector Address

   SA = 03XXXh for Parameter Block1

   SA = 05XXXh for Parameter Block2

   SA = 1FXXXh

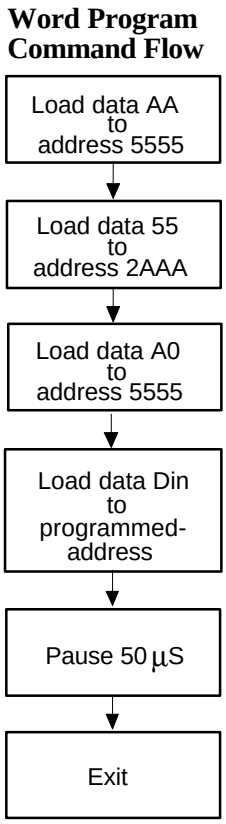
   - for Main Memory Block when Boot Block lockout feature is activated

   - for both Boot Block and Main Memory Block when Boot Block lockout feature is inactivated

Command Codes for Word Program

WORD SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	A0H
3 Write	Programmed-address	Programmed-data
	Pause 50 μS	

Word Program Flow Chart



Notes for software program code:
Data Format: DQ15–DQ8: Don't Care; DQ7-DQ0 (Hex)
Address Format: A14–A0 (Hex)

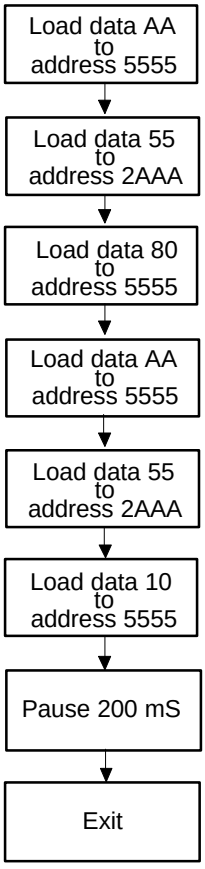
*It is not allowed to assert read command during the 4-word command sequence(program).

To assert the read command during the 4-word command sequence will abort programming procedure.

Command Codes for Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	10H
	Pause 200 mS	

Chip Erase Acquisition Flow

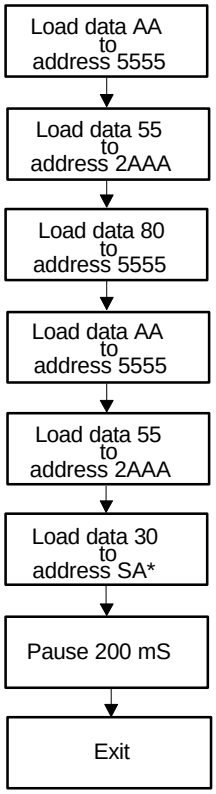


Notes for chip erase:
Data Format: DQ15-DQ8: Don't Care; DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

Command Codes for Sector Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	SA*	30H
	Pause 200 mS	

Sector Erase Acquisition Flow



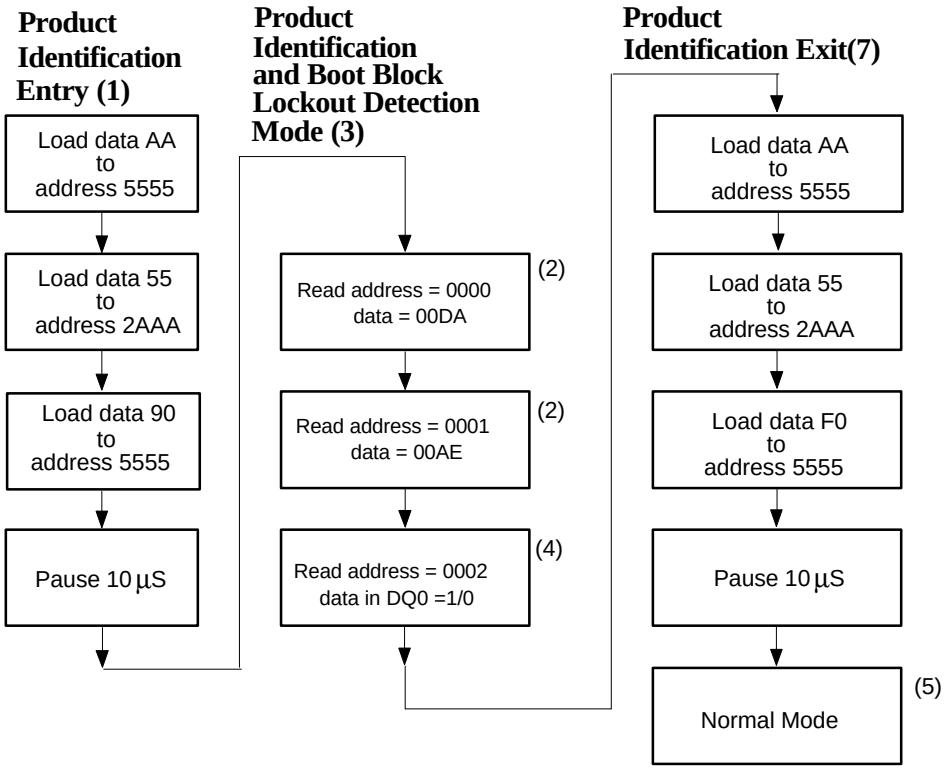
Notes for chip erase:

Data Format: DQ15-DQ8: Don't Care; DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)
SA = 03XXX for parameter block1
SA = 05XXX for parameter block2
SA = 1FXXX
- for Main Memory Block when Boot Block lockout feature is activated
- for both Boot Block and Main Memory Block when Boot Block lockout feature is inactivated

Command Codes for Product Identification and Boot Block Lockout Detection

BYTE SEQUENCE	ALTERNATE PRODUCT (6) IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY		SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION EXIT (7)	
	ADDRESS	DATA	ADDRESS	DATA
1 Write	5555	AA	5555H	AAH
2 Write	2AAA	55	2AAAH	55H
3 Write	5555	90	5555H	F0H
	Pause 10 µS		Pause 10 µS	

Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ15-DQ8 (Don't Care), DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)

(2) A1–A16 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block lockout detection mode if power down.

(4) If the output data in DQ0 = 1, the boot block programming lockout feature is activated; if the output data in DQ0 = 0, the lockout feature is inactivated and the block can be programmed.

(5) The device returns to standard operation mode.

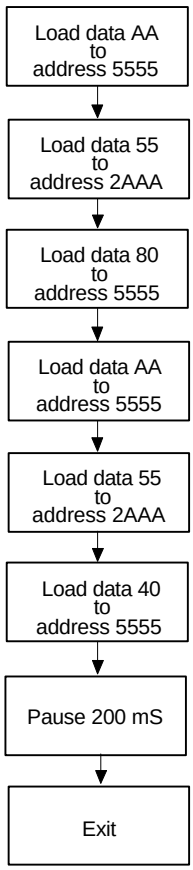
(6) Optional 1-write cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

Command Codes for Boot Block Lockout Enable

BYTE SEQUENCE	BOOT BLOCK LOCKOUT FEATURE SET	
	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	40H
	Pause 200 mS	

Boot Block Lockout Enable Acquisition Flow

Boot Block Lockout Feature Set Flow



Notes for boot block lockout enable:
Data Format: DQ15-DQ8 Don't Care), DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except $\overline{OE}$	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on $\overline{OE}$ Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	$\overline{CE}$=$\overline{OE}$= V_{IL}, $\overline{WE}$= V_{IH}, all DQs open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	25	50	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	$\overline{CE}$ = V_{IH}, all DQs open Other inputs = V_{IL}/V_{IH}	-	2	3	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	$\overline{CE}$ = V_{DD} -0.3V, all DQs open Other inputs = V_{DD} -0.3V/GND	-	20	100	µA
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = GND to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	100	µS
Power-up to Write Operation	$T_{PU. WRITE}$	5	mS

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

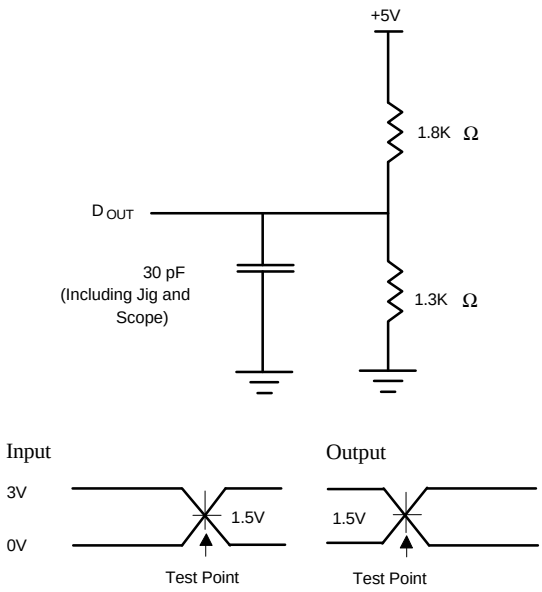
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF

AC Test Load and Waveform



AC Characteristics, continued

Read Cycle Timing Parameters

(V_{CC} = 5.0V ±10 %, V_{CC} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W49F201-45		W49F201-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	45	-	55	-	nS
Chip Enable Access Time	T_{CE}	-	45	-	55	nS
Address Access Time	T_{AA}	-	45	-	55	nS
Output Enable Access Time	T_{OE}	-	35	-	40	nS
$\overline{CE}$ Low to Active Output	T_{CLZ}	0	-	0	-	nS
$\overline{OE}$ Low to Active Output	T_{OLZ}	0	-	0	-	nS
$\overline{CE}$ High to High-Z Output	T_{CHZ}	-	25	-	25	nS
$\overline{OE}$ High to High-Z Output	T_{OHZ}	-	25	-	25	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	nS

Note: The parameter of T_{CLZ}, T_{OLZ}, T_{CHZ}, T_{OHZ} are characterized only and is not 100% tested.

Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	T_{AS}	0	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Setup Time	T_{CS}	0	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Hold Time	T_{CH}	0	-	-	nS
$\overline{OE}$ High Setup Time	T_{OES}	0	-	-	nS
$\overline{OE}$ High Hold Time	T_{OEH}	0	-	-	nS
$\overline{CE}$ Pulse Width	T_{CP}	70	-	-	nS
$\overline{WE}$ Pulse Width	T_{WP}	70	-	-	nS
$\overline{WE}$ High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	10	-	-	nS
Word programming Time	T_{BC}	-	35	50	µS
Erase Cycle Time	T_{EC}	-	60	200	mS

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

AC Characteristics, continued

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	W49F201-45		W49F201-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
$\overline{OE}$ to Data Polling Output Delay	TOEP	-	35	-	40	nS
$\overline{CE}$ to Data Polling Output Delay	TCEP	-	45	-	55	nS
$\overline{WE}$ High to $\overline{OE}$ Low for Data Polling	TOEHP	100	-	100	-	nS
$\overline{OE}$ to Toggle Bit Output Delay	TOET	-	35	-	40	nS
$\overline{CE}$ to Toggle Bit Output Delay	TCET	-	45	-	55	nS
$\overline{WE}$ High to $\overline{OE}$ Low for Toggle Bit	TOEHT	100	-	100	-	nS

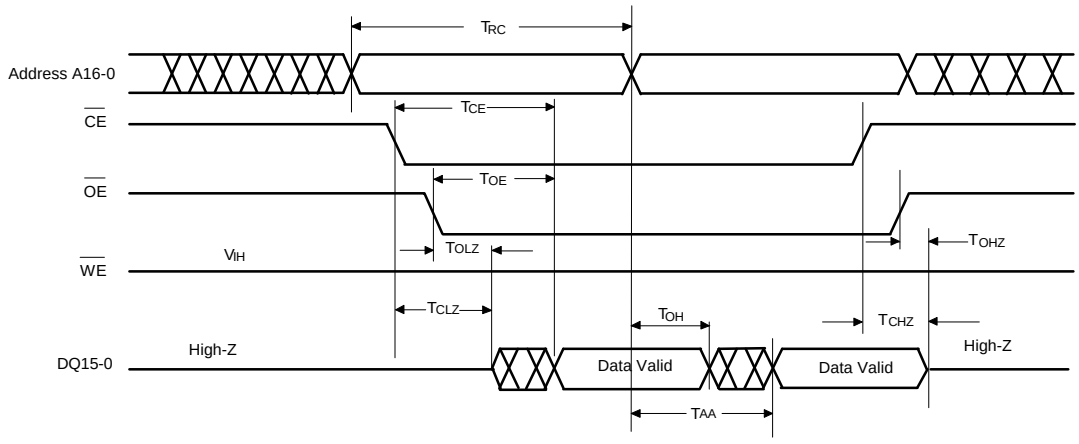
Hardware Reset Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{RESET}$ Pulse Width	TRP	500	-	nS
$\overline{RESET}$ High Time Before Read(1)	TRH	50	-	nS

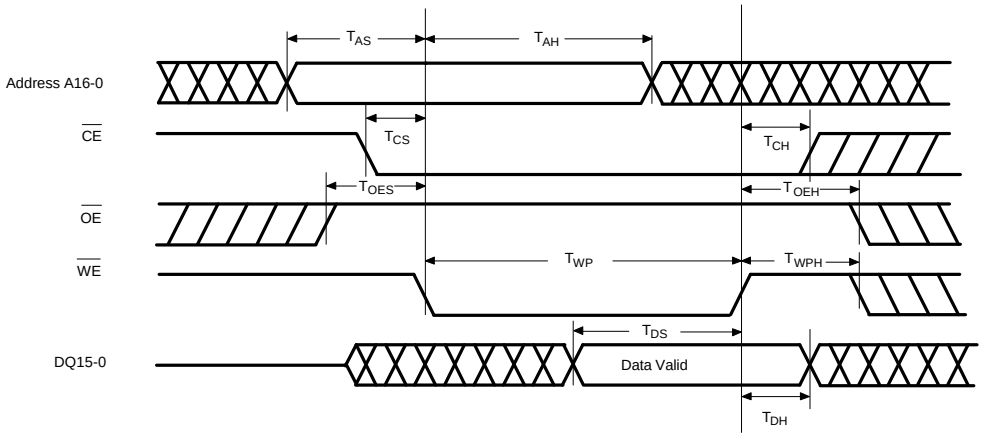
Note: 1. The parameters are characterized only and is not 100% tested.

TIMING WAVEFORMS

Read Cycle Timing Diagram

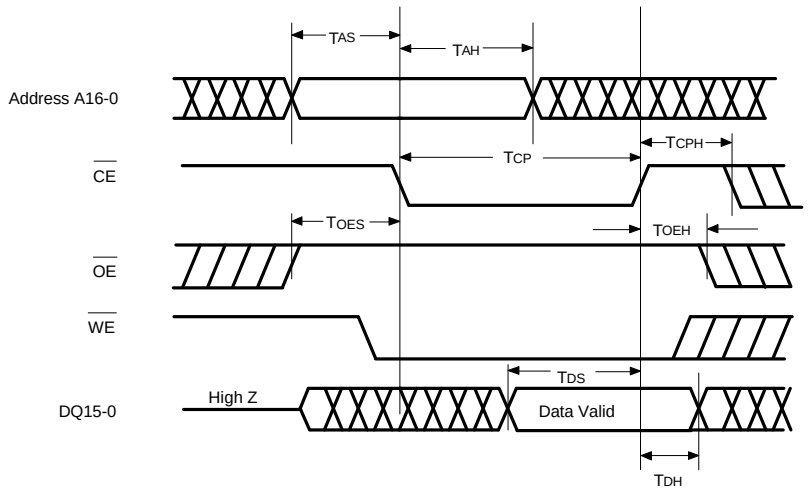


WE Controlled Command Write Cycle Timing Diagram

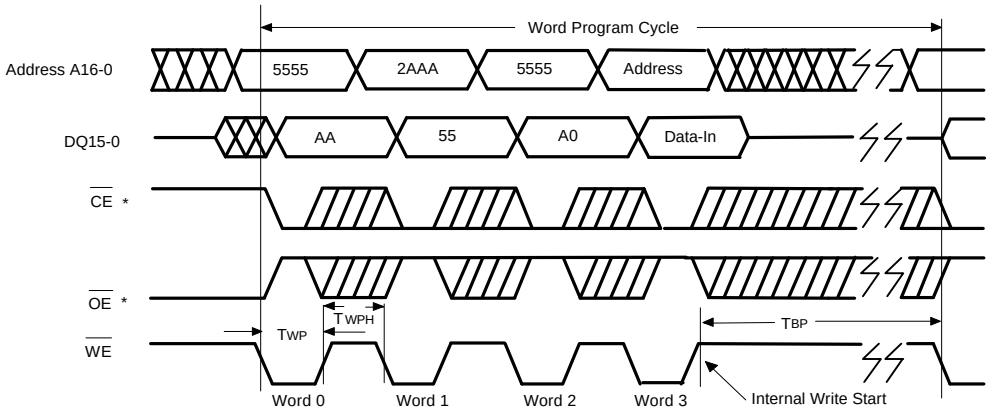


Timing Waveforms, continued

$\overline{CE}$ Controlled Command Write Cycle Timing Diagram



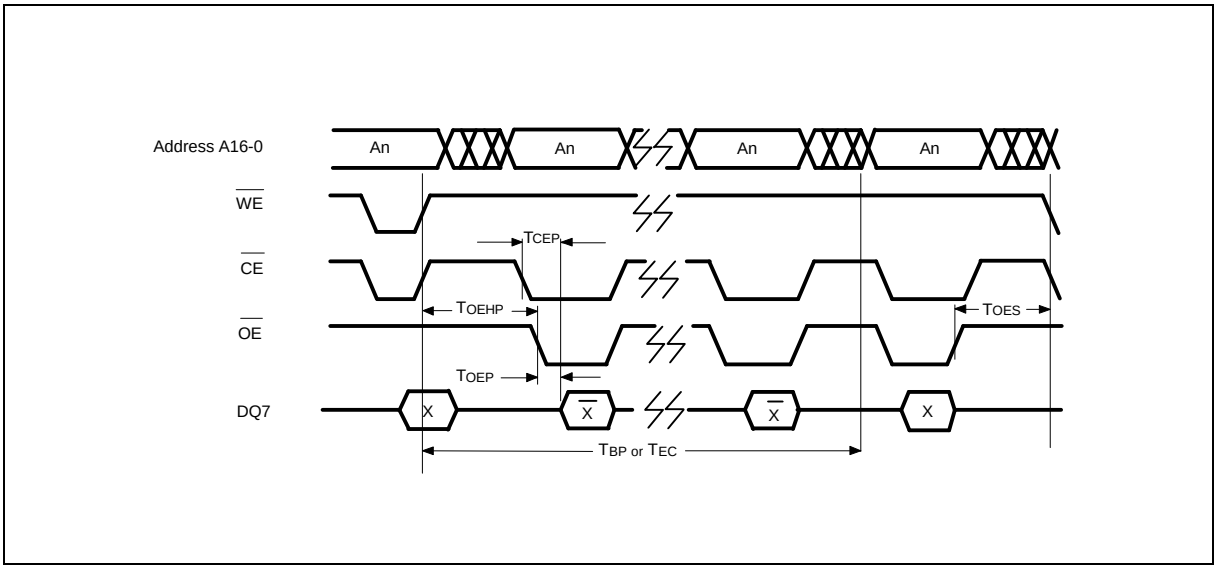
Program Cycle Timing Diagram



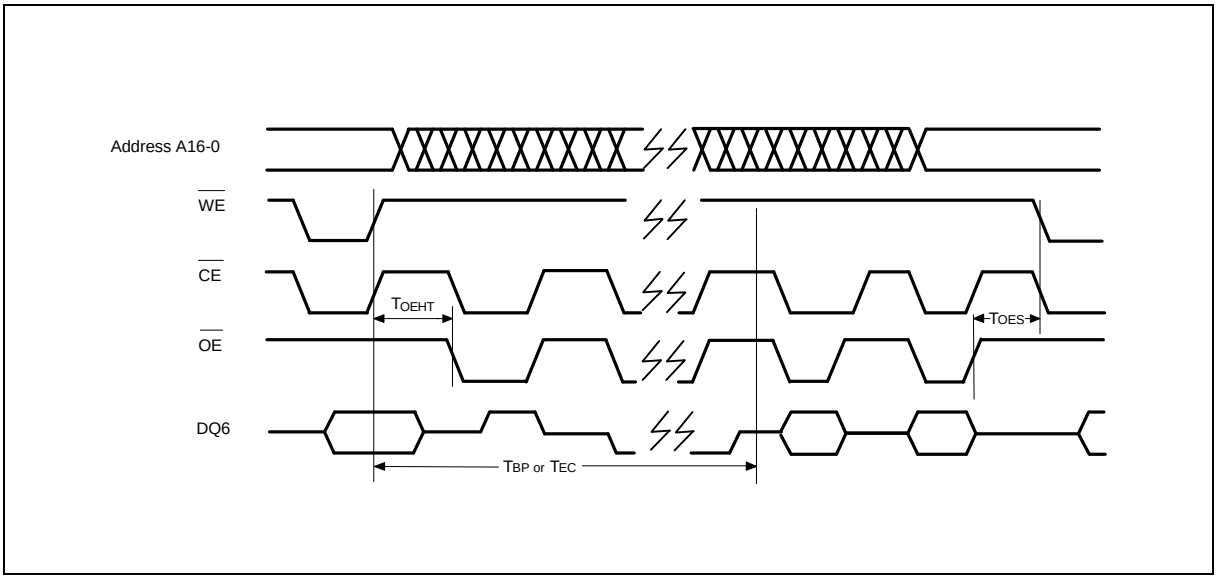
*Note: It is not allowed to assert read operation(CE# &OE# are both active) during the command sequence. If read command is asserted during the command sequence, then the device will return to read mode(abort write).

Timing Waveforms, continued

$\overline{\text{DATA}}$ Polling Timing Diagram

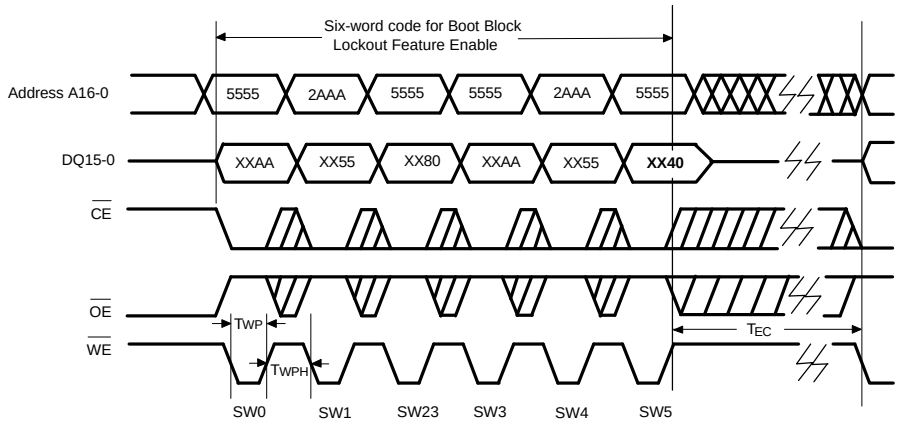


Toggle Bit Timing Diagram



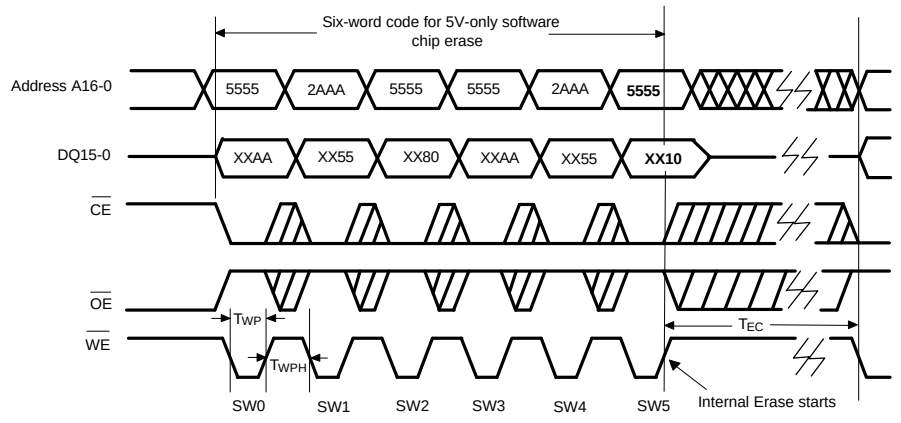
Timing Waveforms, continued

Boot Block Lockout Enable Timing Diagram



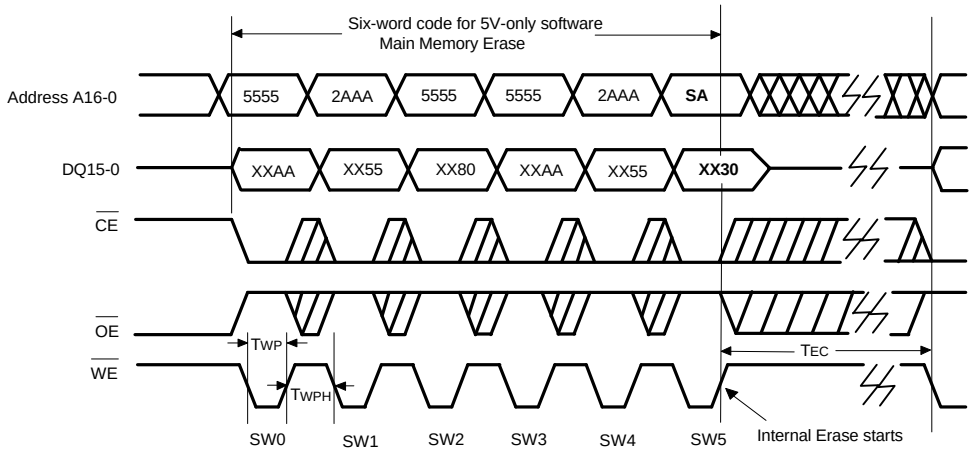
*Note: It is not allowed to assert read operation(CE# &OE# are both active) during the command sequence. If read command is asserted during the command sequence, then the device will return to read mode(abort write).

Chip Erase Timing Diagram



Timing Waveforms, continued

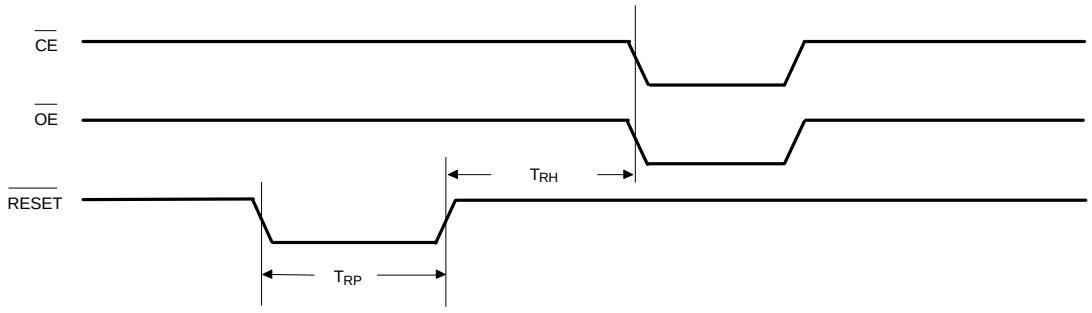
Sector Erase Timing Diagram



*Note: It is not allowed to assert read operation(CE# &OE# are both active) during the command sequence. If read command is asserted during the 4-word command sequence, then the device will return to read mode(abort write).

SA = Sector Address

Reset Timing Diagram



ORDERING INFORMATION

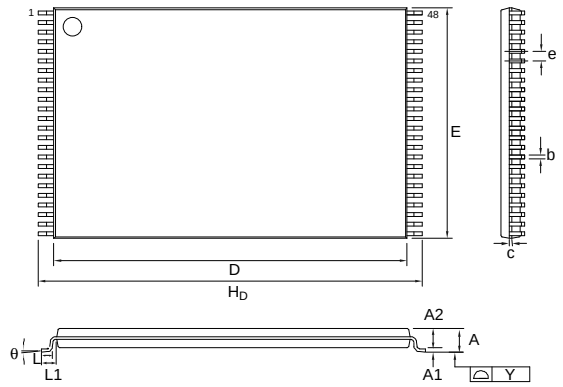
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (mA)	PACKAGE	CYCLE
W49F201S-45	45	50	200 (CMOS)	44-pin SOP	1K
W49F201S-55	55	50	200 (CMOS)	44-pin SOP	1K
W49F201T-45	45	50	200 (CMOS)	48-pin TSOP (12 mm × 20 mm)	1K
W49F201T-55	55	50	200 (CMOS)	48-pin TSOP (12 mm × 20 mm)	1K
W49F201S-45B	45	50	200 (CMOS)	44-pin SOP	10K
W49F201S-55B	55	50	200 (CMOS)	44-pin SOP	10K
W49F201T-45B	45	50	200 (CMOS)	48-pin TSOP (12 mm × 20 mm)	10K
W49F201T-55B	55	50	200 (CMOS)	48-pin TSOP (12 mm × 20 mm)	10K

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

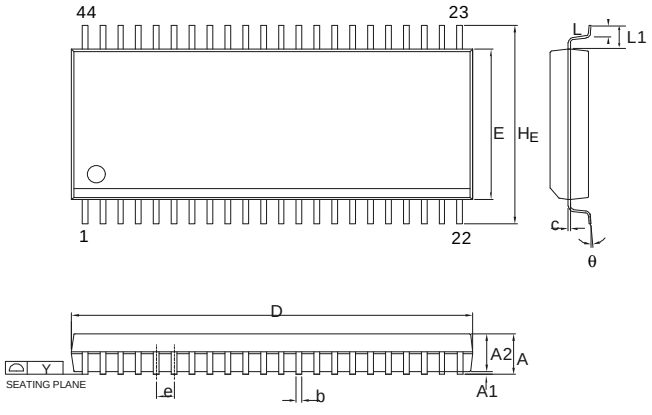
PACKAGE DIMENSIONS

48-pin TSOP (12 mm · 20 mm)



Symbol	Dimension in mm			Dimension in Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	—	0.002	—	—
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.3	18.4	18.5	0.720	0.724	0.728
H_D	19.8	20.0	20.2	0.780	0.787	0.795
E	11.9	12.0	12.1	0.468	0.472	0.476
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	—	0.21	0.004	—	0.008
e	—	0.50	—	—	0.020	—
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
Y	—	—	0.10	—	—	0.004
θ	0	—	5	0	—	5

44-pin SOP



Symbol	Dimension in mm			Dimension in Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.26	—	2.82	0.089		0.111
b	0.36	0.41	0.50	0.014	0.016	0.020
c	0.10	0.15	0.21	0.004	0.006	0.008
D	28.07	28.19	28.32	1.105	1.110	1.115
E	13.10	13.30	13.50	0.516	0.524	0.531
HE	15.80	16.00	16.20	0.622	0.630	0.638
e	1.12	1.27	1.42	0.044	0.050	0.056
L	0.60	0.80	1.00	0.024	0.032	0.040
L1	—	1.35	—	—	0.053	—
Y	—	—	0.10	—	—	0.004
θ	0	—	7	0	—	7

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jun. 1999	-	Renamed from W29F201C

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