GENERAL DESCRIPTION

The ST16C1550 and ST16C1551 UARTs (here on denoted as the ST16C155X) are improved versions of the SSI 73M155X and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C155X provides enhanced UART functions with 16 byte FIFOs, a modem control interface, independent programmable baud rate generators with clock rates up to 1.5 Mbps. Onboard status registers provide the user with error indications and operational status. System interrupt and modem control features may be tailored by external software to meet specific user requirements. An internal loopback capability allows onboard diagnostics. The baud rate generator can be configured for either crystal or external clock input with the exception of the 28 pin ST16C1551 package (where an external clock must be provided). Each package type, with the exception of the 28 pin ST16C155X, provides a buffered reset output that can be controlled through user software. DMA monitor signals TXRDY/RXRDY are not available at the ST16C155X I/O pins but these signals are accessible through ISR register bits 4-5. Except as listed above, all package versions have the same features. The ST16C155X is not a MS Windows compatible UART. For a MS Windows compatible UART, see the ST16C550.

FEATURES

- Pin and functionally compatible to SSI 73M1550/2550
- 16 byte Transmit FIFO
- 16 byte Receive FIFO with error flags
- 4 selectable Receive FIFO interrupt trigger levels
- Modem Control Signals (CTS#, RTS#, DSR#, DTR#, RI#, CD#)
- Programmable character lengths (5, 6, 7, 8) with even, odd or no parity
- Crystal or external clock input (except 28 pin ST16C1551, external clock only)
- 1.5 Mbps Transmit/Receive operation (24 MHz) with programmable clock control
- Power Down Mode (50 uA at 3.3 V, 200 uA at 5 V)
- Software controllable reset output
- 2.97 to 5.5 Volt operation

APPLICATIONS

- Battery Operated Electronics
- Internet Appliances
- Handheld Terminal
- Personal Digital Assistants
- Cellular Phones DataPort

FIGURE 1. BLOCK DIAGRAM

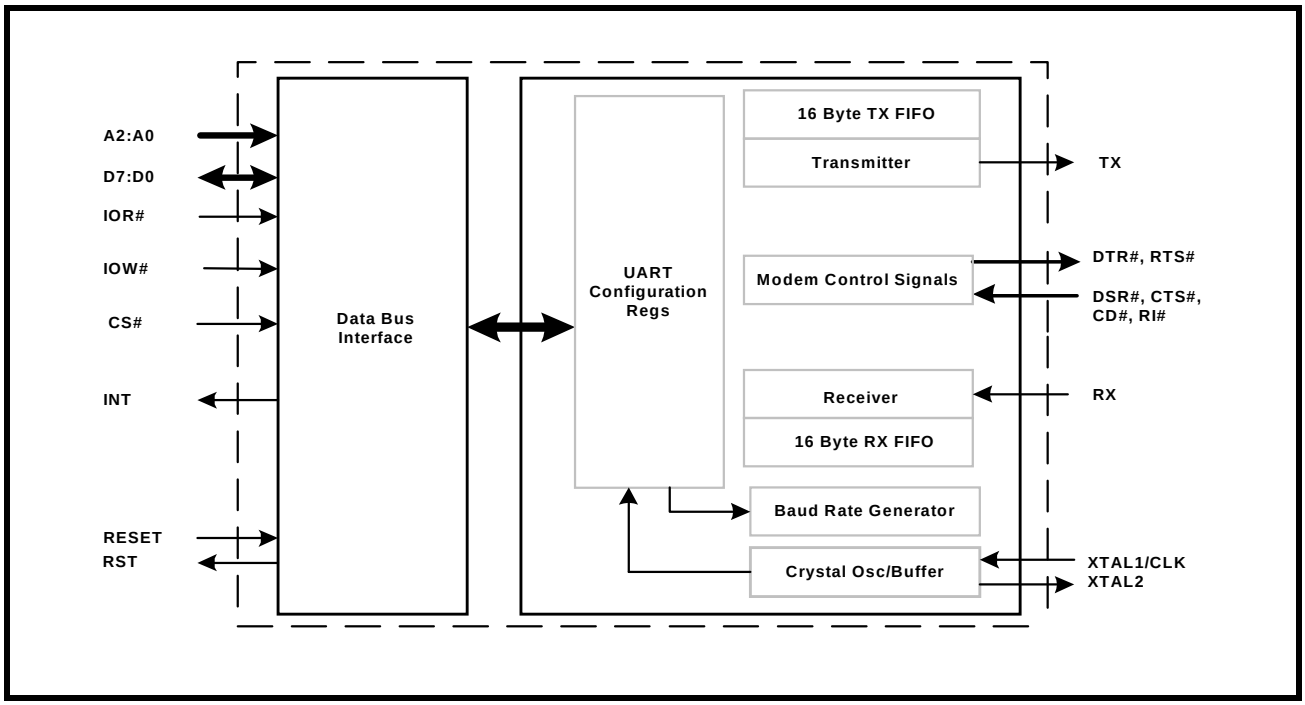
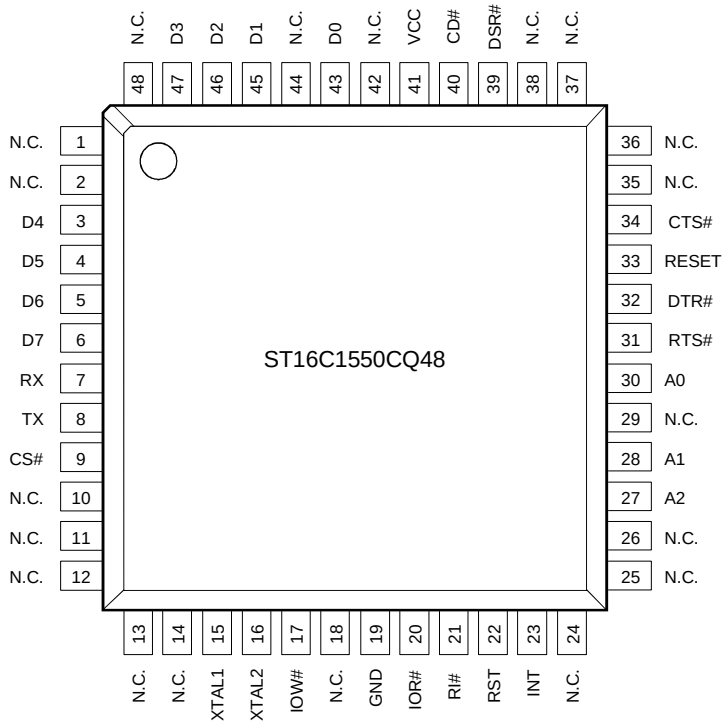


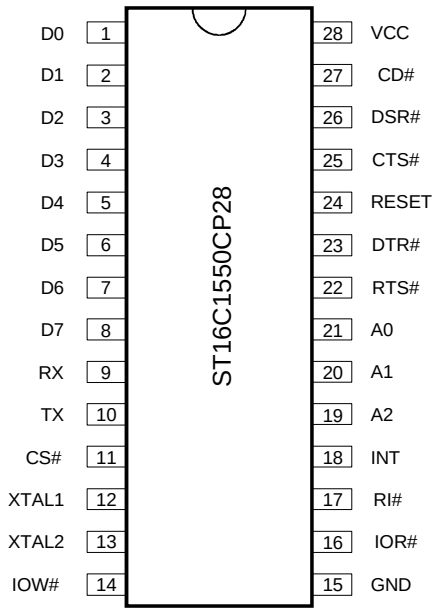
FIGURE 2. ST16C1550 PINOUTS

48-TQFP PACKAGE



NOTE: PINOUTS NOT TO SCALE. ACTUAL SIZE OF TQFP PACKAGE IS SMALLER THAN PLCC PACKAGE.

28-PDIP PACKAGES



28-PLCC PACKAGES

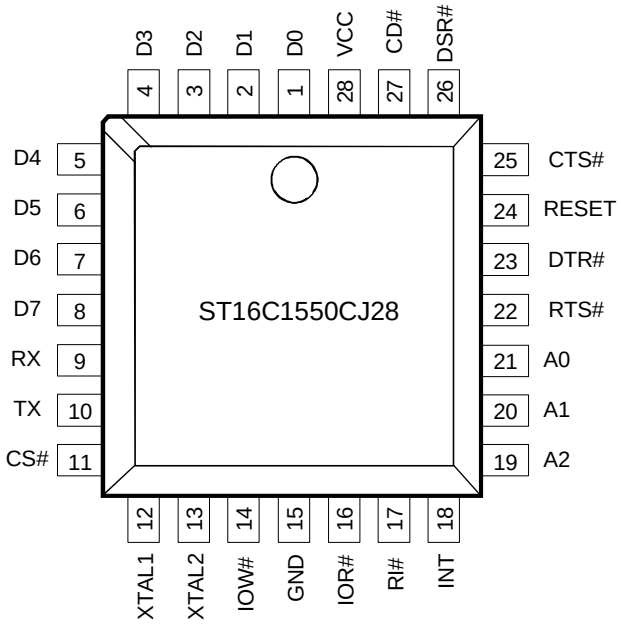
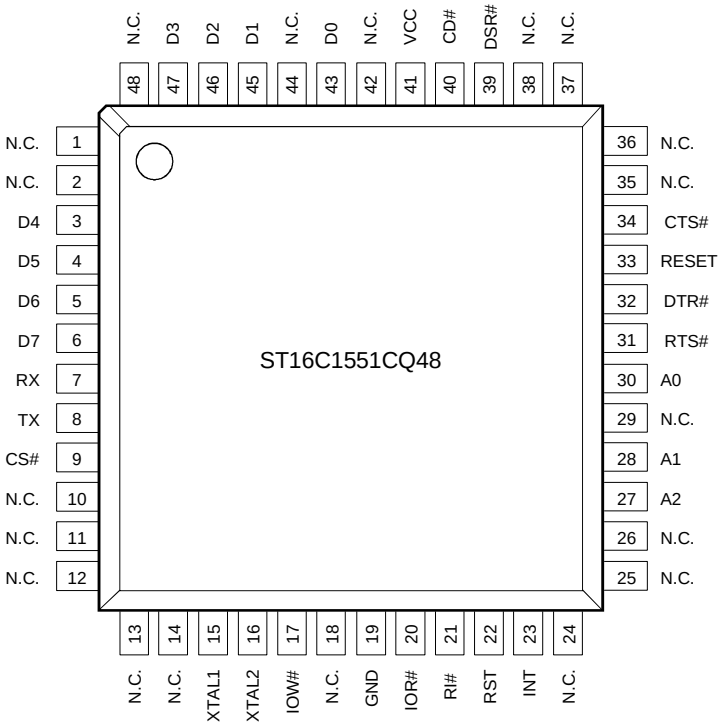


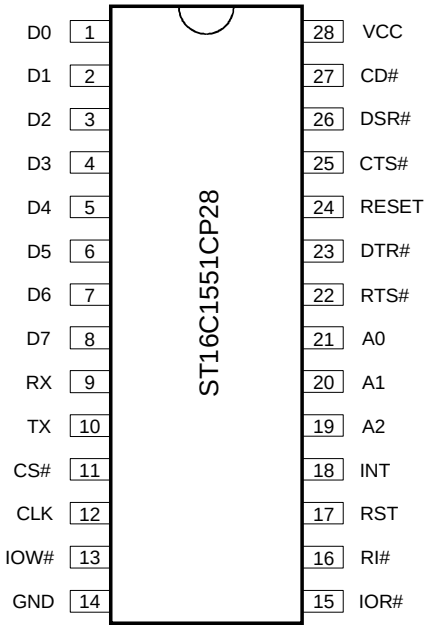
FIGURE 3. ST16C1551 PINOUTS

48-TQFP PACKAGE

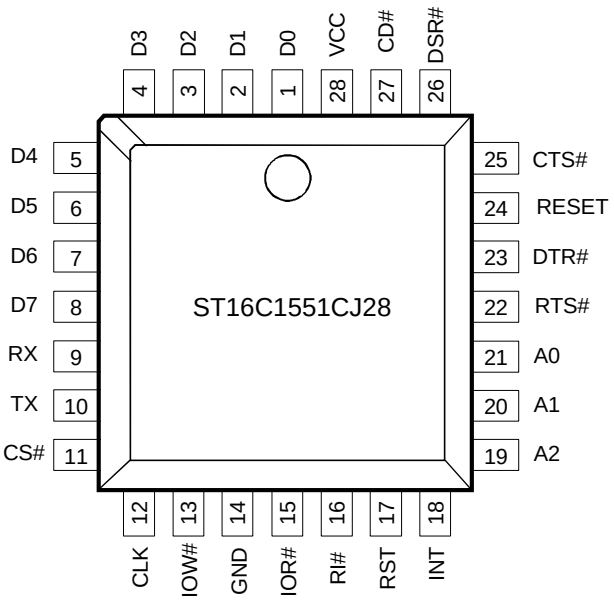


NOTE: PINOUTS NOT TO SCALE. ACTUAL SIZE OF TQFP PACKAGE IS SMALLER THAN PLCC PACKAGE.

28-PDIP PACKAGES



28-PLCC PACKAGES



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
ST16C1550CP28	28-Lead PDIP	0°C to +70°C	Discontinued. See the ST16C1550CQ48 for a replacement.
ST16C1550CJ28	28-Lead PLCC	0°C to +70°C	Active
ST16C1550CQ48	48-Lead TQFP	0°C to +70°C	Active
ST16C1551CP28	28-Lead PDIP	0°C to +70°C	Discontinued. See the ST16C1551CQ48 for a replacement.
ST16C1551CJ28	28-Lead PLCC	0°C to +70°C	Active
ST16C1551CQ48	48-Lead TQFP	0°C to +70°C	Active
ST16C1550IP28	28-Lead PDIP	-40°C to +85°C	Discontinued. See the ST16C1550IQ48 for a replacement.
ST16C1550IJ28	28-Lead PLCC	-40°C to +85°C	Active
ST16C1550IQ48	48-Lead TQFP	-40°C to +85°C	Active
ST16C1551IP28	28-Lead PDIP	-40°C to +85°C	Discontinued. See the ST16C1551IQ48 for a replacement.
ST16C1551IJ28	28-Lead PLCC	-40°C to +85°C	Active
ST16C1551IQ48	48-Lead TQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

NAME	28-PIN PDIP (1550)	28-PIN PDIP (1551)	28-PIN PLCC (1550)	28-PIN PLCC (1551)	48-PIN TQFP	TYPE	DESCRIPTION
DATA BUS INTERFACE							
A0 A1 A2	21 20 19	21 20 19	21 20 19	21 20 19	30 28 27	I	Address data lines [2:0]. A2:A0 selects internal UART's configuration registers.
D0 D1 D2 D3 D4 D5 D6 D7	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	43 45 46 47 3 4 5 6	I/O	Data bus lines [7:0] (bidirectional).
IOR#	16	15	16	15	20	I	Input/Output Read (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], places it on the data bus to allow the host processor to read it on the leading edge.
IOW#	14	13	14	13	17	I	Input/Output Write (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines [A2:A0].
CS#	11	11	11	11	9	I	Chip Select input (active low). A logic 0 on this pin selects the ST16C155X device.
INT	18	18	18	18	23	O	Interrupt Output (three-state, active high). INT output defaults to three-state mode and becomes active high when MCR bit-3 is set to a logic 1. INT output becomes a logic high level when interrupts are enabled in the interrupt enable register (IER), and whenever the transmitter, receiver, line and/or modem status register has an active condition.
MODEM OR SERIAL I/O INTERFACE							
TX	10	10	10	10	8	O	Transmit Data. This output is associated with individual serial transmit channel data from the 155X. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loopback mode, the TX output pin is disabled and TX data is internally connected to the UART RX input.
RX	9	9	9	9	7	I	Receive Data. This input is associated with individual serial channel data to the 155X. Normal received data input idles at logic 1 condition. This input must be connected to its idle logic state, logic 1, else the receiver may report "receive break" and/or "error" condition(s).

NAME	28-PIN PDIP (1550)	28-PIN PDIP (1551)	28-PIN PLCC (1550)	28-PIN PLCC (1551)	48-PIN TQFP	TYPE	DESCRIPTION
RTS#	22	22	22	22	31	O	Request to Send or general purpose output (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, leave it unconnected.
CTS#	25	25	25	25	34	I	Clear to Send or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
DTR#	23	23	23	23	32	O	Data Terminal Ready or general purpose output (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, leave it unconnected.
DSR#	26	26	26	26	39	I	Data Set Ready input or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
CD#	27	27	27	27	40	I	Carrier Detect input or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
RI#	17	16	17	16	21	I	Ring Indicator input or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
ANCILLARY SIGNALS							
CLK	-	12	-	12	-	I	External Clock Input. This function is associated with 28 pin PDIP and 28 pin PLCC packages only. An external clock must be connected to this pin to clock the baud rate generator and internal circuitry.
XTAL1	12	-	12	-	15	I	Crystal or external clock input. See Figure 4 for typical oscillator connections.
XTAL2	13	-	13	-	16	O	Crystal or buffered clock output. See Figure 4 for typical oscillator connections.
RESET	24	24	24	24	33	I	Reset Input (active high). When it is asserted, the UART configuration registers are reset to default values, see Table 8.
RST	-	17	-	17	22	O	Reset Output (active high). This output is only available on the ST16C1551. When IER bit-5 is a logic 0, RST will follow the logical state of the RESET pin. When IER bit-5 is a logic 1, the user may send software (soft) resets via MCR bit-2. Soft resets from MCR bit-2 are “ORed” with the state of the RESET pin.
VCC	28	28	28	28	41	Pwr	Power supply input.

NAME	28-PIN PDIP (1550)	28-PIN PDIP (1551)	28-PIN PLCC (1550)	28-PIN PLCC (1551)	48-PIN TQFP	TYPE	DESCRIPTION
GND	15	14	15	14	19	Pwr	Power supply common ground.
N.C.	-	-	-	-	1, 2, 10-14, 18, 24-26, 29, 35-38, 42, 44, 48	-	Not connected.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The ST16C155X provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required in digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors.

ENHANCED FEATURES

The ST16C155X is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of none in the 16C145X. The 155X is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 155X by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C550 with a 16 byte FIFO, unloads 16 bytes of receive data in 93 microseconds (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO less than every 100 microseconds. However with the 16 byte FIFO in the 155X, the data buffer will not require unloading/loading for 1.53 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the 4 selectable levels of FIFO trigger interrupt are provided for maximum data throughput performance especially when operating in a multi-channel environment. The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

DATA RATE

The 155X is capable of operation up to 1.5 Mbps with a 24 MHz crystal or external clock input with a 16X sampling clock (at VCC = 5.0V). With a crystal of 14.7456 MHz and through a software option, the user can select data rates up to 921.6 Kbps.

The rich feature set of the 155X is available through internal registers. Selectable receive FIFO trigger levels, selectable baud rates, and modem interface controls are all standard features. Following a power on reset or an external reset, the 155X is software compatible with the ST16C145X.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Internal Registers

The 155X has a set of enhanced registers for controlling, monitoring and data loading and unloading. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible scractchpad register (SPR). All the register functions are discussed in full detail later in "Section 3.0, UART INTERNAL REGISTERS" on page 14.

2.2 DMA Mode

The DMA Mode (a legacy term) in this document does not mean "Direct Memory Access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY and TXRDY bits (ISR bits 5 and 4 respectively). The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 155X activates the TXRDY & RXRDY output pin for each data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. In this mode, the 155X sets the TXRDY bit when the transmit FIFO becomes full, and sets the RXRDY pin when the receive FIFO becomes empty. The following table shows their behavior.

TABLE 1: TXRDY AND RXRDY BITS IN FIFO AND DMA MODE

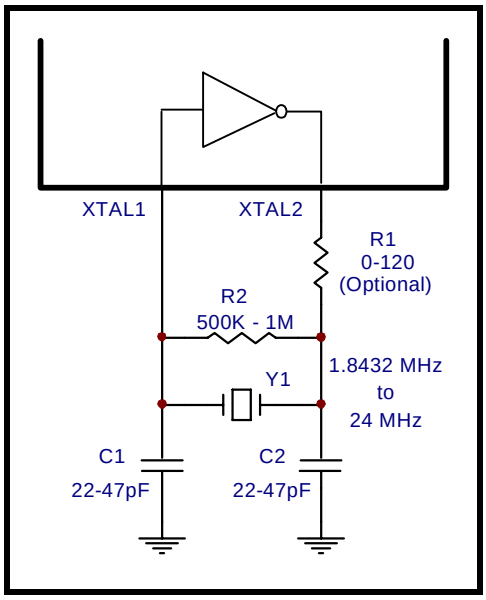
PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
RXRDY	1 = 1 byte 0 = no data	1 = at least 1 byte in FIFO 0 = FIFO empty	1 = FIFO reaches the trigger level, or timeout occurs 0 = FIFO empty
TXRDY	1 = THR empty 0 = byte in THR	1 = FIFO empty 0 = at least 1 byte in FIFO	1 = FIFO has at least 1 empty location 0 = FIFO is full

2.3 Crystal Oscillator or External Clock

The 155X includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see "Section 2.4, Programmable Baud Rate Generator" on page 9.

The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see Figure 4). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typical oscillator connections are shown in Figure 4. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

FIGURE 4. TYPICAL OSCILLATOR CONNECTIONS



2.4 Programmable Baud Rate Generator

The UART has its own Baud Rate Generator (BRG) with a prescaler. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up or a reset. Therefore, the BRG must be programmed during initialization to the operating data rate. Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. Table 2 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X clock rate. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16)

TABLE 2: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0	DIVISOR FOR 16X Clock (Decimal)	DIVISOR FOR 16X Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

2.5 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 16 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

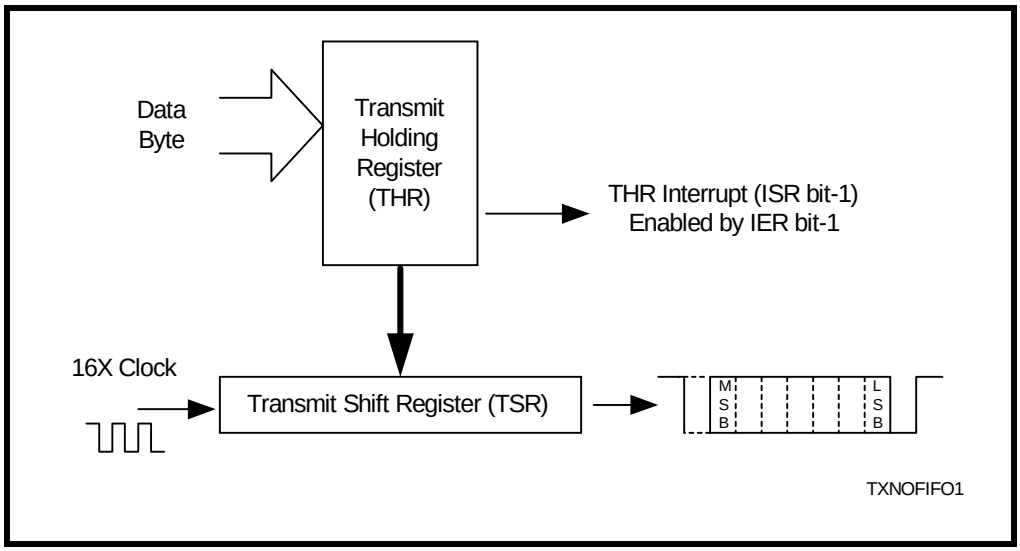
2.5.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 16 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.5.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

FIGURE 5. TRANSMITTER OPERATION IN NON-FIFO MODE



2.5.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 16 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

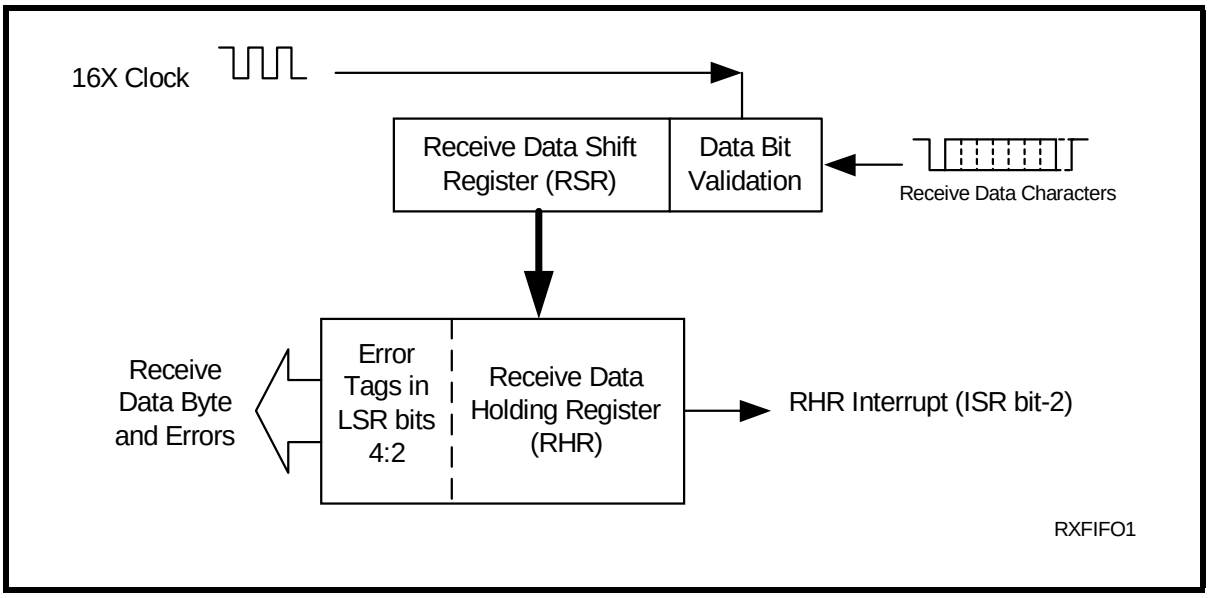
2.6 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 16 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.6.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 16 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 6. RECEIVER OPERATION IN NON-FIFO MODE



2.7 Special (Enhanced Feature) Mode

The 155X supports the standard features of the ST16C550. In addition the 155X supports some enhanced features not available for the ST16C550. These features are enabled by IER bit-5 and include a software controllable (SOFT) reset, power down feature and FIFO monitoring bits.

2.7.1 Soft Reset

Soft resets are useful when the user desires the capability of resetting an externally connected device only. MCR bit-2 can be used to initiate a SOFT reset at the RST output pin. This does not reset the 155X (only the RESET input pin can reset the 155X). Soft resets from MCR bit-2 are “ORed” with the RESET input pin. Therefore both reset types will be seen at the RST output pin.

2.7.2 Power Down Mode

The power down feature (controlled by MCR bit-7) provides the user with the capability to conserve power when the package is not in actual use without destroying internal register configuration data. This allows quick turnarounds from power down to normal operation.

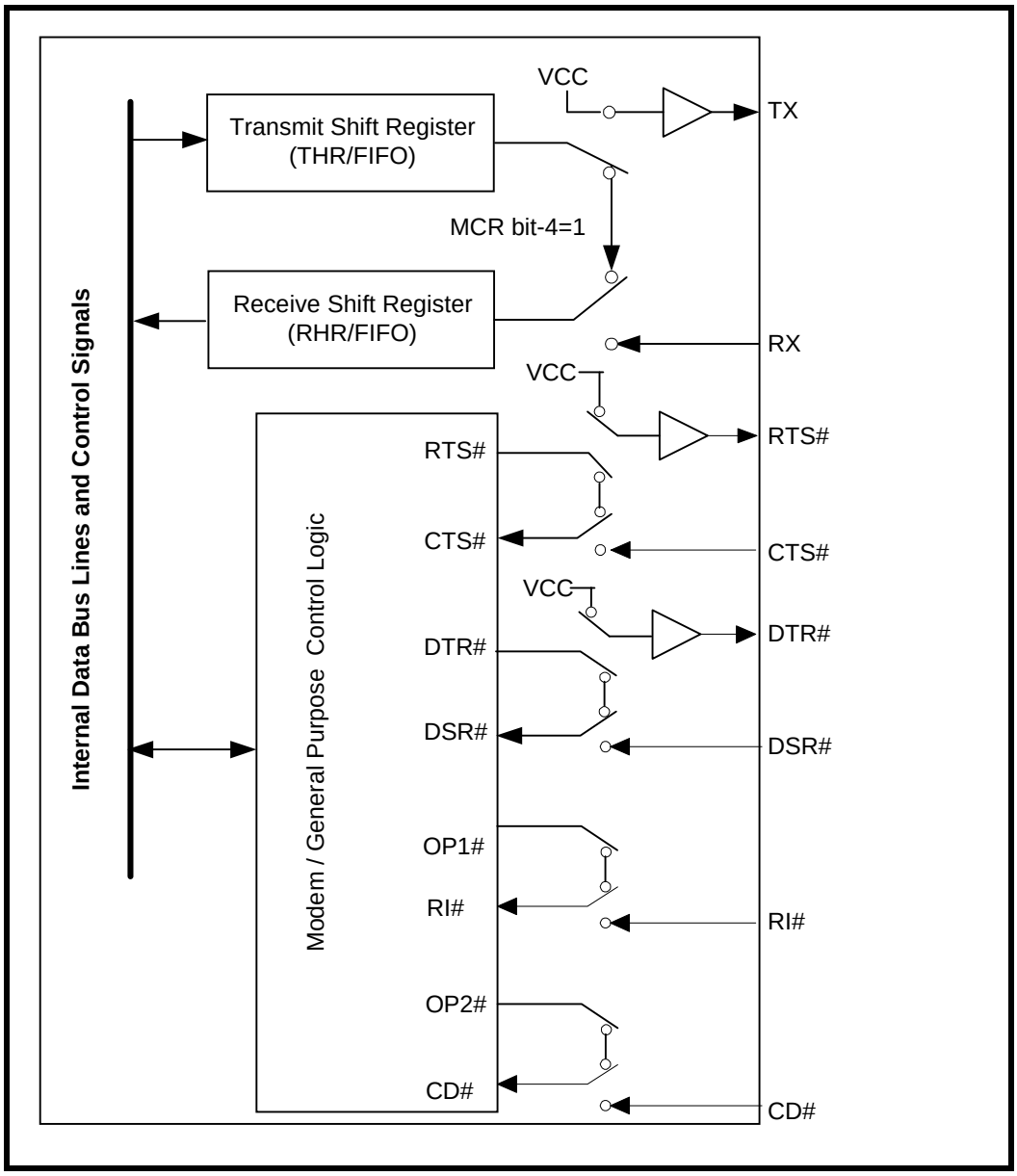
2.7.3 TXRDY and RXRDY bits

When IER bit-5 is set to a logic 1, ISR bits 4 and 5 represent the compliment (inversion) of the TXRDY status and RXRDY status, respectively. See Table 1.

2.8 Internal Loopback

The 155X UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 7 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

FIGURE 7. INTERNAL LOOPBACK



3.0 UART INTERNAL REGISTERS

The 155X has a set of configuration registers selected by address lines A0, A1 and A2. The 16C550 compatible registers can be accessed when LCR[7] = 0 and the baud rate generator divisor registers can be accessed when LCR[7] = 1. The complete register set is shown on Table 3 and Table 4.

TABLE 3: ST16C155X UART INTERNAL REGISTERS

A2,A1,A0 ADDRESSES	REGISTER	READ/WRITE	COMMENTS
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Div Latch Low Byte	Read/Write	LCR[7] = 1
0 0 1	DLM - Div Latch High Byte	Read/Write	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR[7] = 0
1 0 1	LSR - Line Status Register Reserved	Read-only Write-only	
1 1 0	MSR - Modem Status Register Reserved	Read-only Write-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	

.

TABLE 4: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0	0	Special Mode Enable (Enable ISR bits 5-4, FCR bits 5-4, MCR bits 7, 2)	0	Modem Status Int. Enable	RX Line Status Int. Enable	TX Empty Int. Enable	RX Data Int. Enable	LCR[7] = 0
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ RXRDY	0/ TXRDY	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0 1 0	FCR	WR	RX FIFO Trigger (MSB)	RX FIFO Trigger (LSB)	0/ TX FIFO Trigger (MSB)	0/ TX FIFO Trigger (LSB)	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ Power Down Mode	0	0	Internal Loop-back Enable	(OP2#)/ INT Output Enable	(OP1#)/ SOFT Reset	RTS# Output Control	DTR# Output Control	
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Over-run Error	RX Data Ready	LCR[7] = 0
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

See “Receiver” on page 11.

4.2 Transmit Holding Register (THR) - Write-Only

See “Transmitter” on page 10.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the ST16C155X in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR is empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated. Note that this interrupt does not behave in the same manner as the industry standard 16C550. See “Interrupt Clearing:” on page 17.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt when the character with errors is read out of the FIFO.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Reserved

IER[5]: Special Mode Enable

- Logic 0 = Disable special mode functions (default).
- Logic 1 = Enable special mode functions in addition to basic ST16C1450 functions. Enables ISR bits 4-5 (TXRDY/RXRDY), MCR bit-2 (soft reset) and MCR bit-7 (power down) functions.

IER[7:6]: Reserved

4.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 5, shows the data values (bits 0-3) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty.
- MSR is by any of the MSR bits 0, 1, 2 and 3.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register (but flags and tags not cleared until character(s) that generated the interrupt(s) has been emptied or cleared from FIFO).
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR until empty.
- TXRDY interrupt is cleared by a read to the ISR register AND disabling the TXRDY interrupt (set IER bit-1 = 0), or by loading data into the TX FIFO.
- MSR interrupt is cleared by a read to the MSR register.

TABLE 5: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS				SOURCE OF INTERRUPT
	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	1	1	0	LSR (Receiver Line Status Register)
2	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	MSR (Modem Status Register)
-	0	0	0	1	None (default)

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Interrupt Source Table 5).

ISR[4]: TXRDY

This bit represents the compliment (inversion) of the TXRDY status when IER bit-5 is set to a logic 1. See Table 1.

ISR[5]: RXRDY

This bit represents the compliment (inversion) of the RXRDY status when IER bit-5 is set to a logic 1. See Table 1.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.5 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a ‘1’.

- Logic 0 = No receive FIFO reset (default).
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

Controls the behavior of the TXRDY# and RXRDY# pins. See DMA operation section for details.

- Logic 0 = Normal Operation (default).
- Logic 1 = DMA Mode.

FCR[5:4]: Transmit FIFO Trigger Select

These 2 bits are only active when IER bit-5 is a '1'.

(logic 0 = default, TX trigger level = 1)

These 2 bits set the trigger level for the transmit FIFO. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 6 shows the selections.

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1)

These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. Table 6 shows the complete selections.

TABLE 6: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION

FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL
		0	0		1
		0	1		4
		1	0		8
		1	1		14
0	0			1	
0	1			4	
1	0			8	
1	1			14	

4.6 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 7 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR[5] = logic 0, parity is not forced (default).
- LCR[5] = logic 1 and LCR[4] = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR[5] = logic 1 and LCR[4] = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

TABLE 7: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, "1"
1	1	1	Forced parity to space, "0"

LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a "space', logic 0, state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a "space", logic 0, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL/DLM) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

4.7 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force DTR# output to a logic 1 (default).
- Logic 1 = Force DTR# output to a logic 0.

MCR[1]: RTS# Output

The RTS# pin is a modem control output and may be used for automatic hardware flow control by enabled by EFR bit-6. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# output to a logic 1 (default).
- Logic 1 = Force RTS# output to a logic 0.

MCR[2]: OP1# Output/Soft Reset

OP1# is not available as an output pin on the 155X. But it is available for use during Internal Loopback Mode. In the Loopback Mode, this bit is used to write the state of the modem RI# interface signal.

- Logic 0 = OP1# output (RI# input) is at logic 1 (default).
- Logic 1 = OP1# output (RI# input) is at logic 0.

In normal operation, this bit is associated with the RST (buffered reset) output pin. The logical state of the RST pin will follow exactly the logical state of the RESET pin. When IER bit-5 = 1, soft resets from MCR bit-2 are ORed with the state of the RESET input pin. Therefore both reset types will be seen at the RST pin. Note that asserting MCR bit-2 does not reset the 155X.

- Logic 0 = The RST output pin is a logic 0 (default).
- Logic 1 = The RST output pin is a logic 1.

MCR[3]: OP2# or INT Output Enable

When not in Internal Loopback Mode:

- Logic 0 = INT output is three-state (default).
- Logic 1 = INT output is active high.

OP2# is not available as an output pin on the 155X. But it is available for use during Internal Loopback Mode. In the Loopback Mode, this bit is used to write the state of the modem CD# interface signal.

- Logic 0 = OP2# output (CD# input) is a logic 1 (default).
- Logic 1 = OP2# output (CD# input) is a logic 0.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and Figure 7.

MCR[6:5]: Reserved

MCR[7]: Power Down Enable

This bit can only be accessed when IER bit-5 = 1.

- Logic 0 = Normal mode (default).
- Logic 1 = Power down mode. See “Power Down Mode” on page 12.

4.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host. If IER bit-2 is set to a logic 1, an LSR interrupt will be generated when the character that is ready to be read from the RX FIFO has an error (parity, framing, overrun, break).

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Error Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[2]: Receive Data Parity Error Tag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The received character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Tag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The received character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[4]: Receive Break Error Tag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication remains until the RX input returns to the idle condition, “mark” or logic 1.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to a logic 1 whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in any of the bytes in the RX FIFO.

4.9 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface input signals. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used for general purpose inputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

CTS# (active high, logical 1). Normally this bit is the compliment of the CTS# input. In the loopback mode, this bit is equivalent to bit-1 in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

DSR# (active high, logical 1). Normally this bit is the compliment of the DSR# input. In the loopback mode, this bit is equivalent to bit-0 in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

RI# (active high, logical 1). Normally this bit is the compliment of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

CD# (active high, logical 1). Normally this bit is the compliment of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

4.10 Scratch Pad Register (SPR) - Read/Write

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

TABLE 8: UART RESET CONDITIONS

REGISTERS	RESET STATE
DLL	Bits 7-0 = 0xXX
DLM	Bits 7-0 = 0xXX
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = Logic 0 Bits 7-4 = Logic levels of the inputs inverted
SPR	Bits 7-0 = 0xFF
I/O SIGNALS	**RESET STATE**
TX	Logic 1
RTS#	Logic 1
DTR#	Logic 1
RST	Logic 1
INT	Three-State Condition

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	7 Volts
Voltage at Any Pin	GND-0.3 V to 7 V
Operating Temperature	-40^{o} to +85^{o}C
Storage Temperature	-65^{o} to +150^{o}C
Package Dissipation	500 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (48-TQFP)	theta-ja = 59^{o}C/W, theta-jc = 16^{o}C/W
Thermal Resistance (28-PDIP)	theta-ja = 57^{o}C/W, theta-jc = 23^{o}C/W
Thermal Resistance (28-PLCC)	theta-ja = 55^{o}C/W, theta-jc = 28^{o}C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97V TO 5.5V

SYMBOL	PARAMETER	LIMITS 3.3V		LIMITS 5.0V		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{ILCK}	Clock Input Low Level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock Input High Level	2.4	VCC	3.0	VCC	V	
V_{IL}	Input Low Voltage	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	VCC	2.2	VCC	V	
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 6 mA
V_{OL}	Output Low Voltage		0.4			V	I_{OL} = 4 mA
V_{OH}	Output High Voltage			2.4		V	I_{OH} = -6 mA
V_{OH}	Output High Voltage	2.0				V	I_{OH} = -1 mA
I_{IL}	Input Low Leakage Current		±10		±10	uA	
I_{IH}	Input High Leakage Current		±10		±10	uA	
C_{IN}	Input Pin Capacitance		5		5	pF	
I_{CC}	Power Supply Current		1.3		3	mA	
I_{PWRDN}	Power Down Current		50		200	uA	See Test 1

Test 1: The following inputs should remain steady at VCC or GND state to minimize Power Down current: A0-A2, D0-D7, IOR#, IOW#, CS# and modem inputs. Also, RX input must idle at logic 1 state while in Power Down mode.

AC ELECTRICAL CHARACTERISTICS

TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97V TO 5.5V

SYMBOL	PARAMETER	LIMITS 3.3V		LIMITS 5.0V		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
CLK	Clock Pulse Duration	63		21		ns	
OSC	Oscillator/External Clock Frequency		8		24	MHz	
T_{AS}	Address Setup Time	5		0		ns	
T_{AH}	Address Hold Time	10		5		ns	
T_{CS}	Chip Select Width	50		40		ns	
T_{RD}	IOR# Strobe Width	35		25		ns	
T_{DY}	Read/Write Cycle Delay	40		30		ns	
T_{RDV}	Data Access Time		35		25	ns	
T_{DD}	Data Disable Time	0	25	0	15	ns	
T_{WR}	IOW# Strobe Width	40		25		ns	
T_{DS}	Data Setup Time	20		15		ns	
T_{DH}	Data Hold Time	5		5		ns	
T_{WDO}	Delay From IOW# To Output		50		40	ns	100 pF load
T_{MOD}	Delay To Set Interrupt From MODEM Input		40		35	ns	100 pF load
T_{RSI}	Delay To Reset Interrupt From IOR#		40		35	ns	100 pF load
T_{SSI}	Delay From Stop To Set Interrupt		1		1	Bclk	
T_{RRI}	Delay From IOR# To Reset Interrupt		45		40	ns	100 pF load
T_{SI}	Delay From Stop To Interrupt		45		40	ns	
T_{INT}	Delay From Initial INT Reset To Transmit Start	8	24	8	24	Bclk	
T_{SSR}	Delay From Stop To Reset RXRDY		1		1	Bclk	
T_{RR}	Delay From IOR# To Set RXRDY		45		40	ns	
T_{WT}	Delay From IOW# To Reset TXRDY		45		40	ns	
T_{SRT}	Delay From Center of Start To Set TXRDY		8		8	Bclk	
T_{RST}	Reset Pulse Width	40		40		ns	
N	Baud Rate Divisor	1	2^{16}-1	1	2^{16}-1	-	
Bclk	Baud Clock	16X of data rate				Hz	

FIGURE 8. CLOCK TIMING

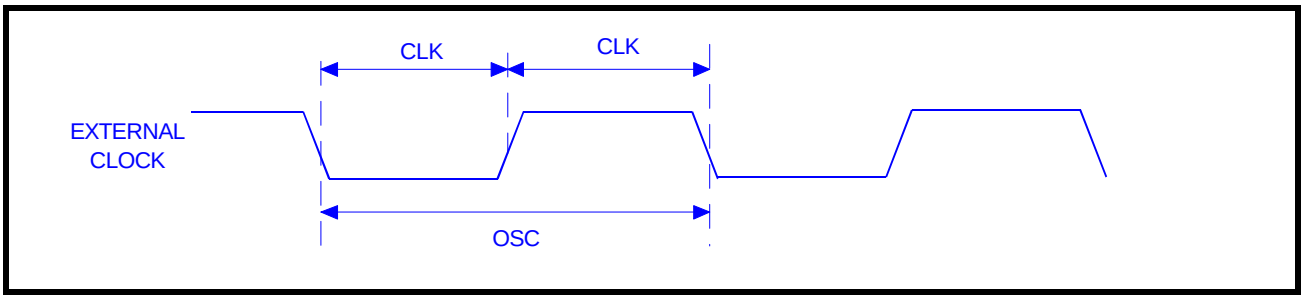


FIGURE 9. MODEM INPUT/OUTPUT TIMING

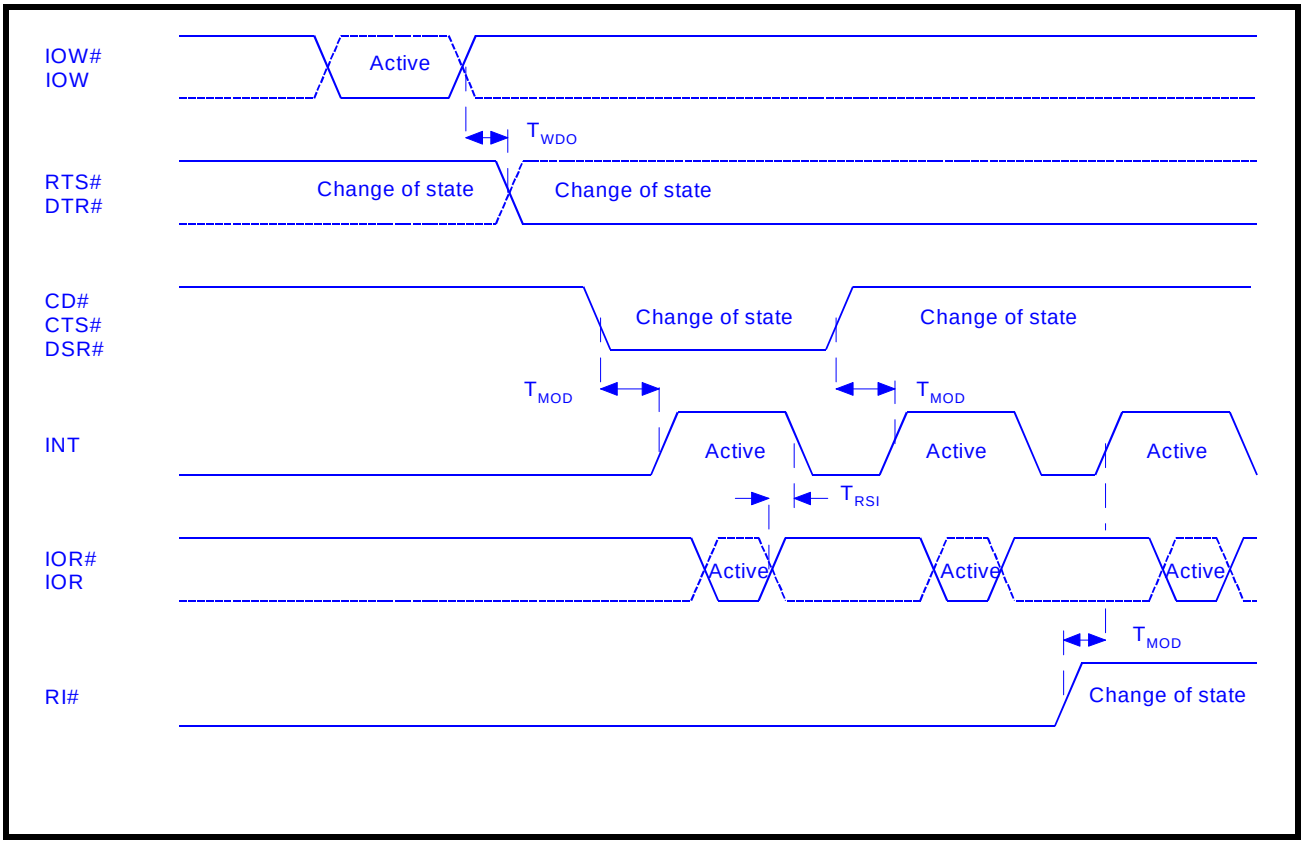


FIGURE 10. DATA BUS READ TIMING

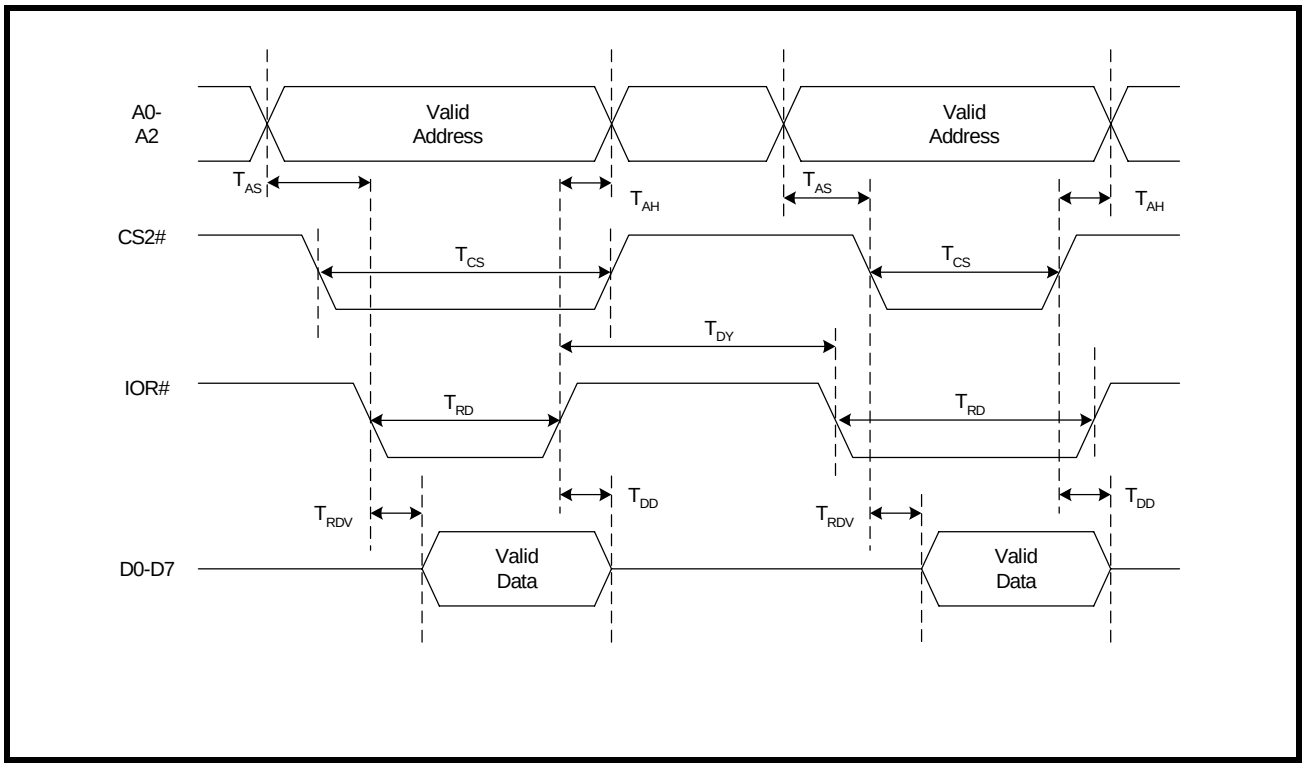


FIGURE 11. DATA BUS WRITE TIMING

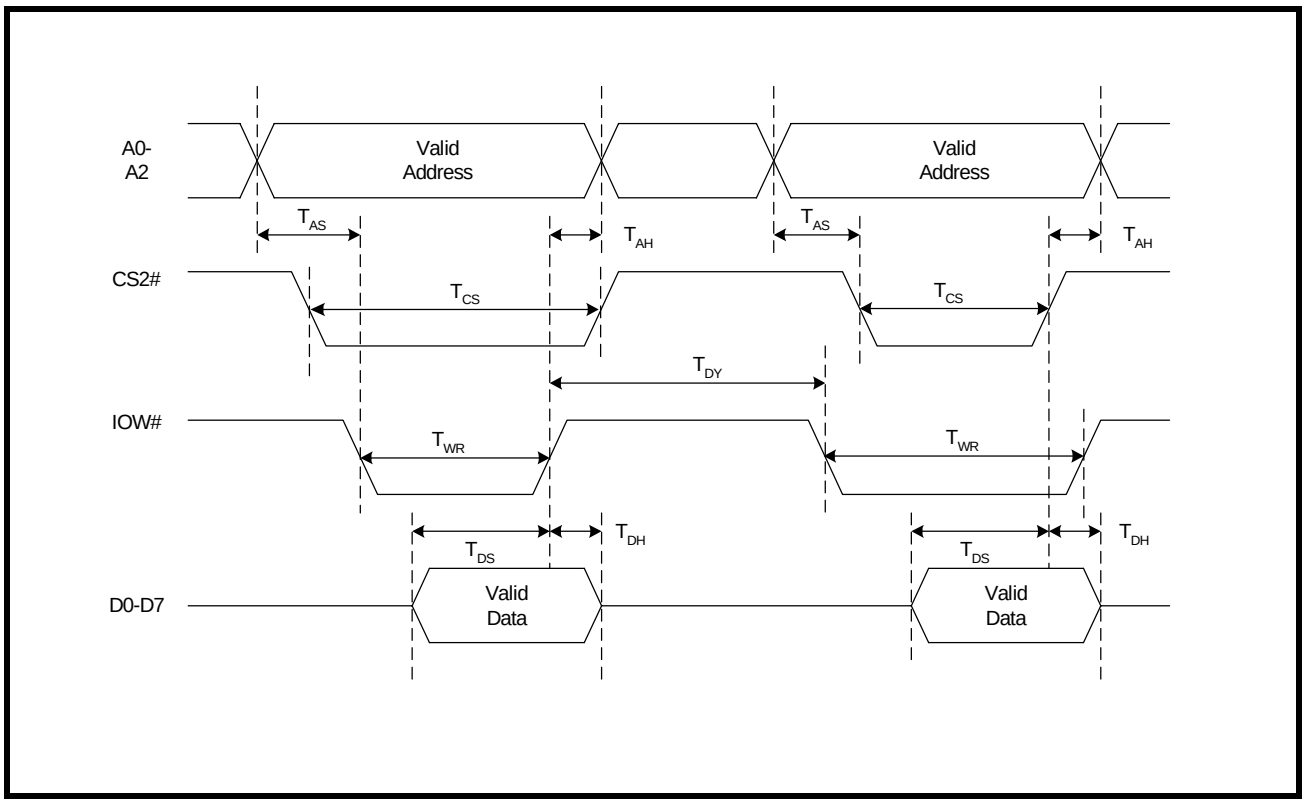


FIGURE 12. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE]

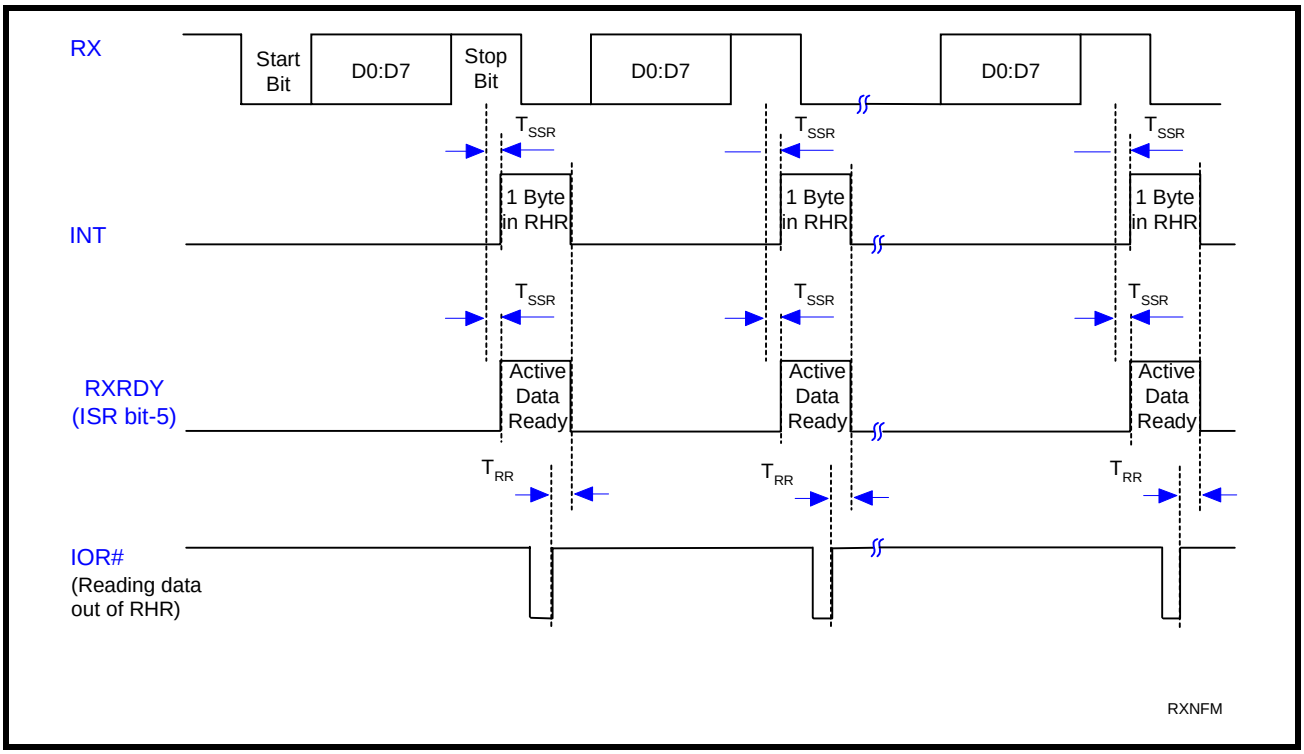


FIGURE 13. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE]

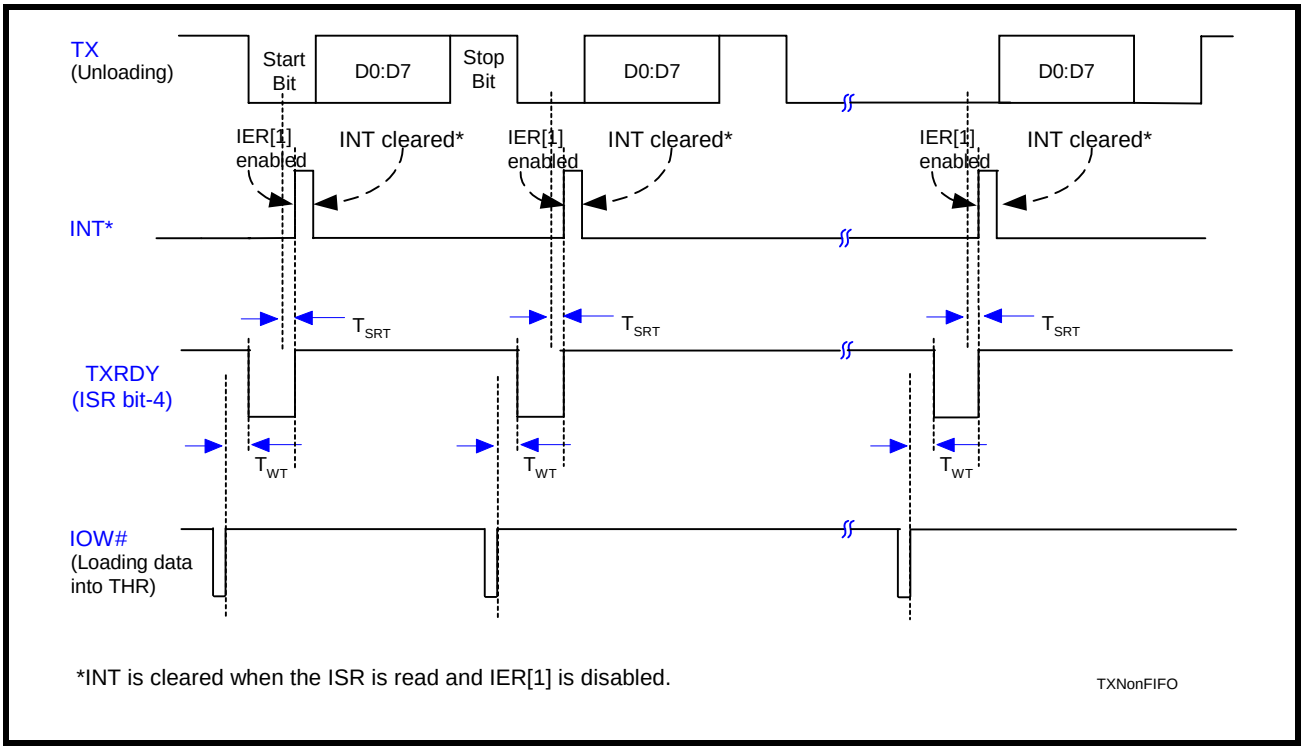


FIGURE 14. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED]

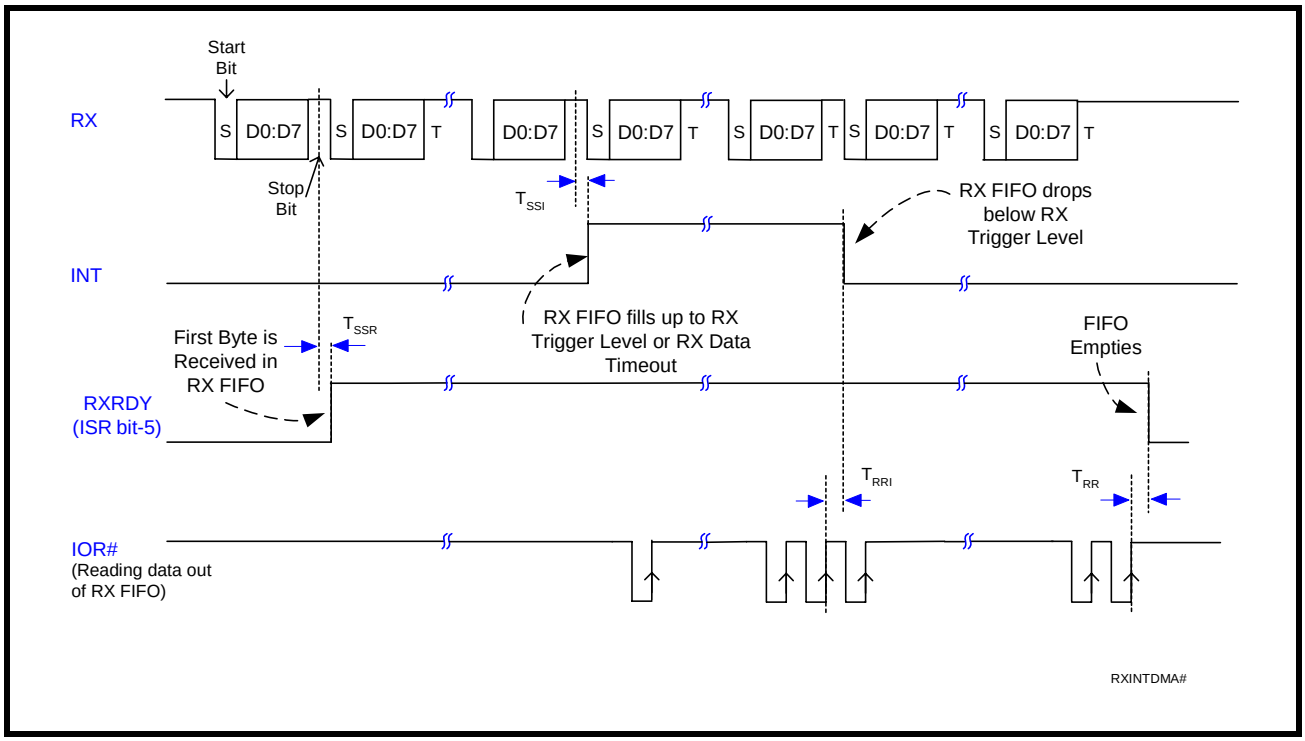


FIGURE 15. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED]

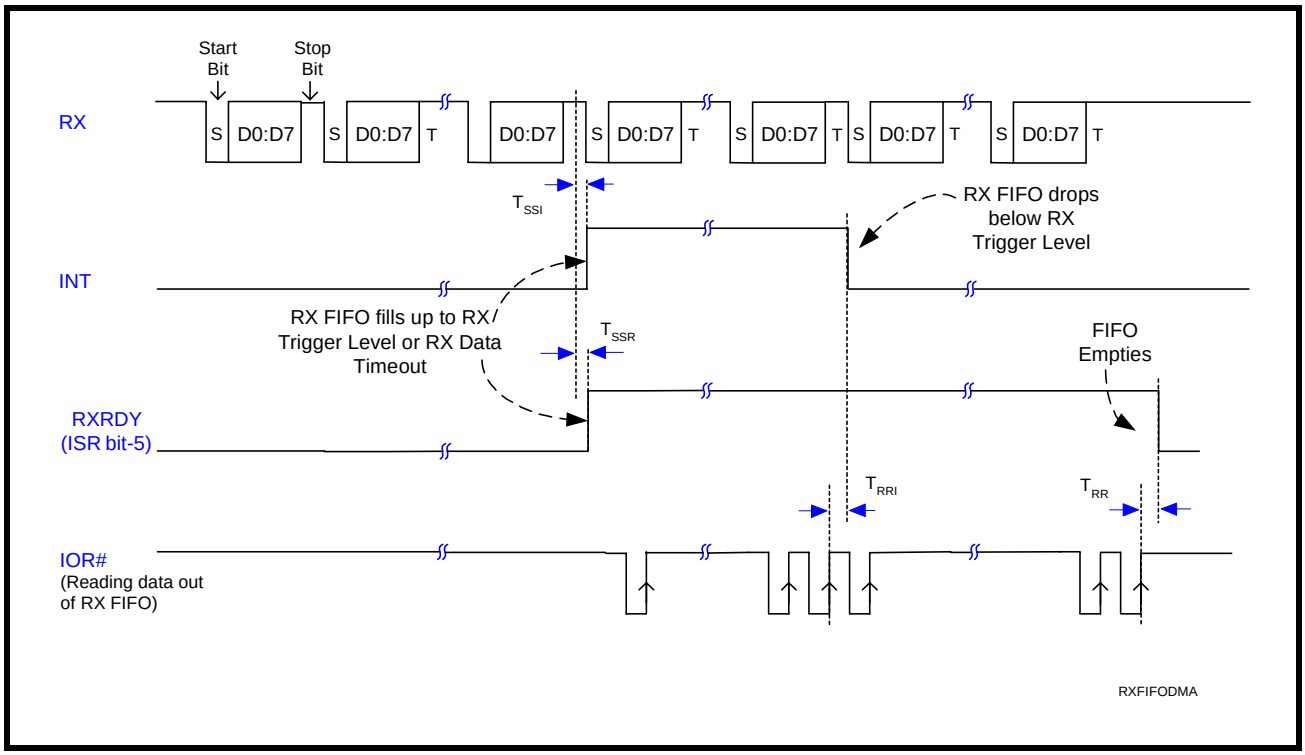


FIGURE 16. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED]

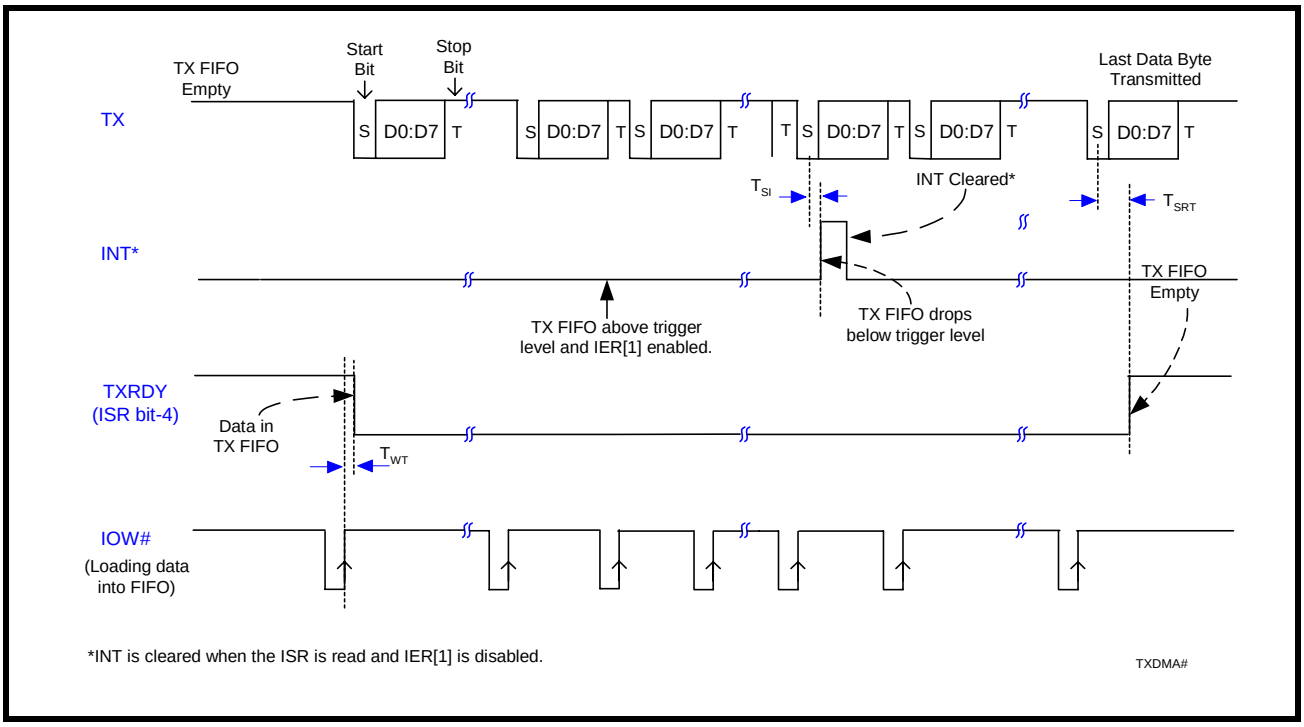
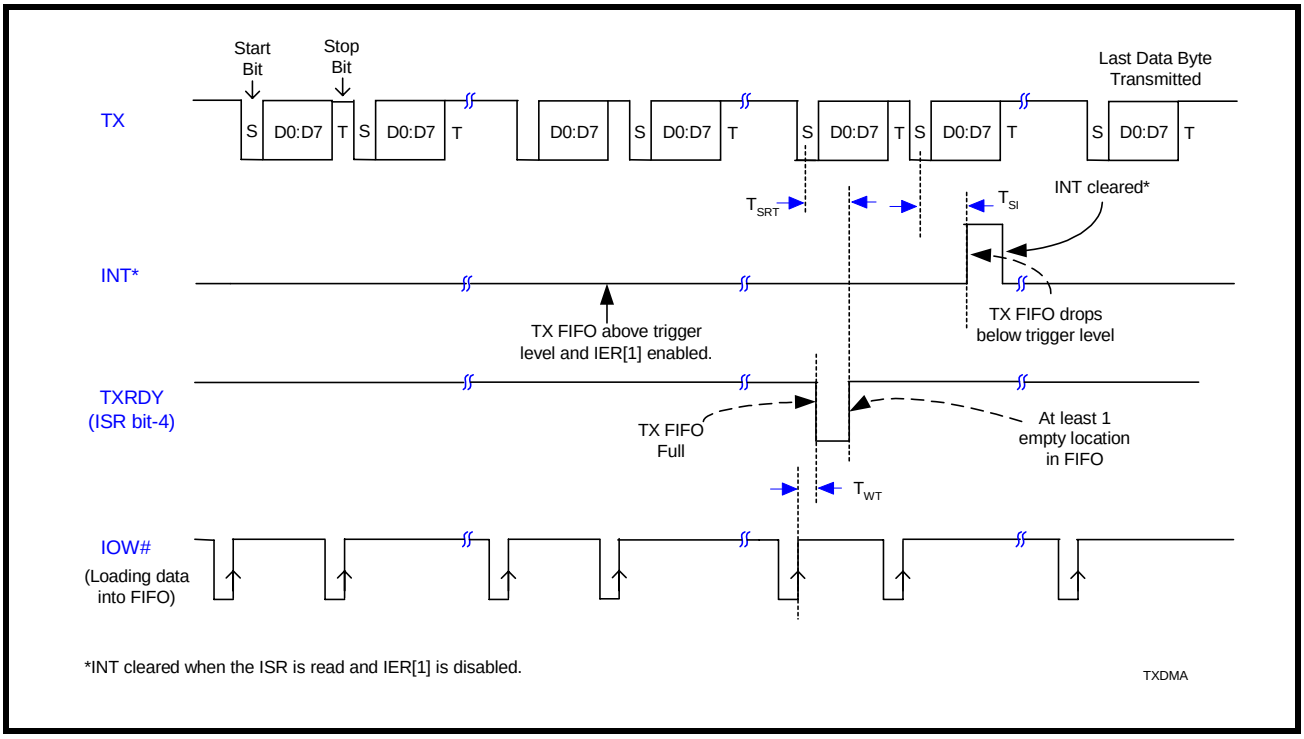
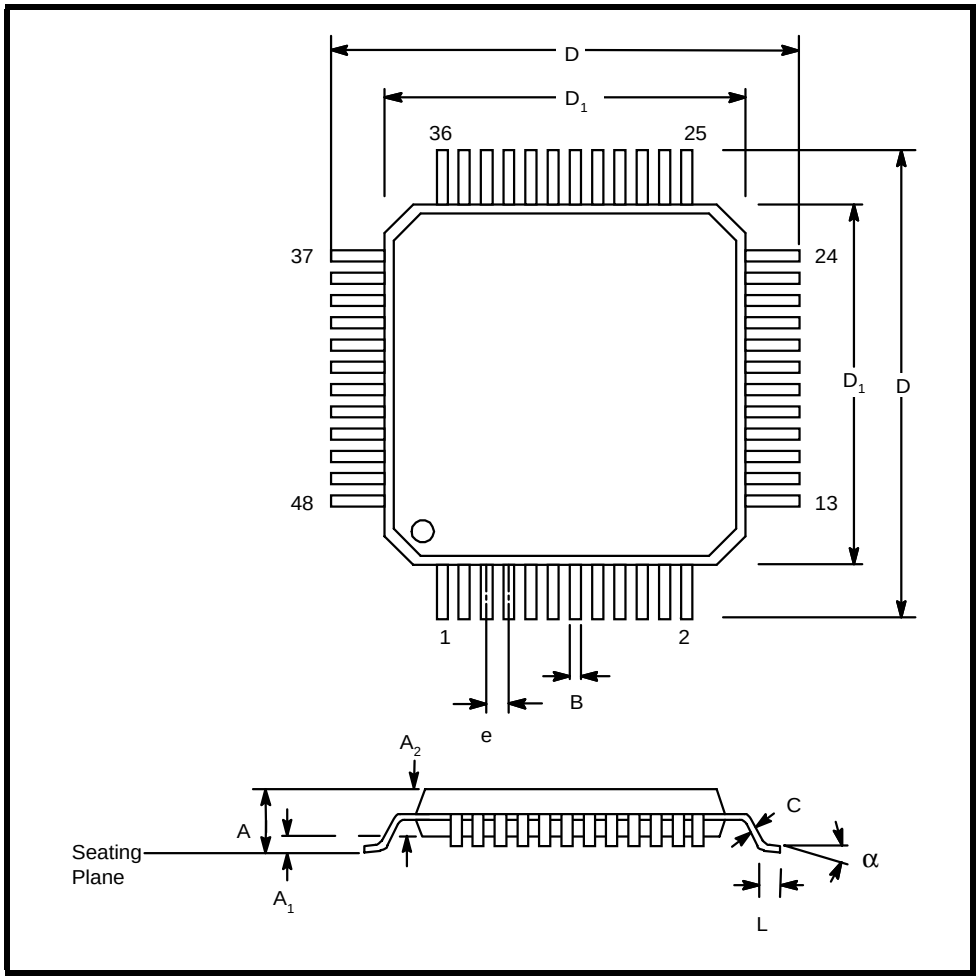


FIGURE 17. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED]



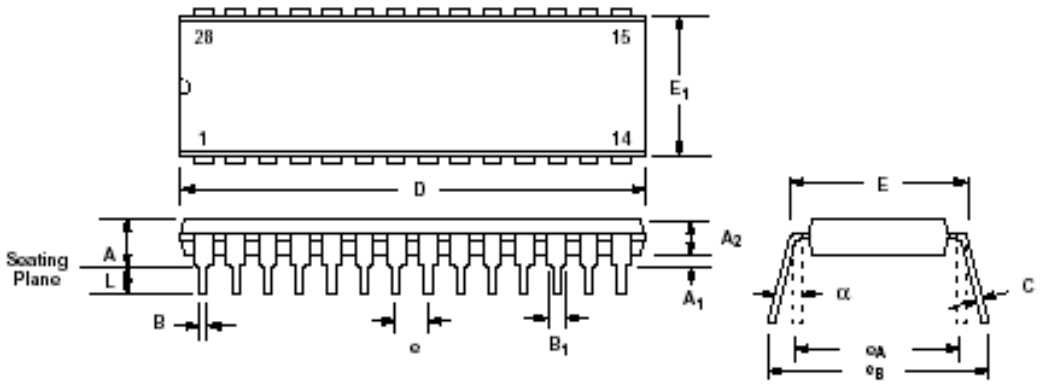
PACKAGE DIMENSIONS (48 PIN TQFP - 7 X 7 X 1 mm)



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A1	0.002	0.006	0.05	0.15
A2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

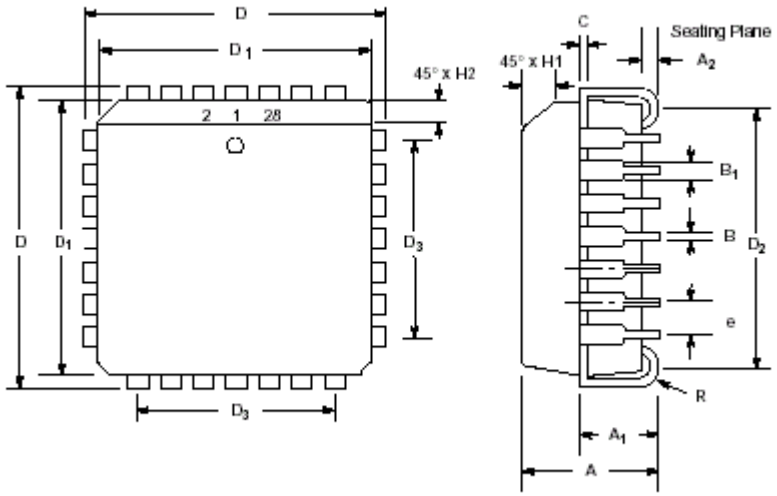
PACKAGE DIMENSIONS (28 PIN PDIP)



Note: The control dimension is the inch column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.250	4.06	6.35
A1	0.015	0.070	0.38	1.78
A2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.380	1.565	35.05	39.75
E	0.600	0.625	15.24	15.88
E1	0.485	0.580	12.32	14.73
e	0.100 BSC		2.54 BSC	
eA	0.600 BSC		15.24 BSC	
eB	0.600	0.700	15.24	17.78
L	0.115	0.200	2.92	5.08
α	0°	15°	0°	15°

PACKAGE DIMENSIONS (28 PIN PLCC)



Note: The control dimension is the inch column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.020	-	0.51	-
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.390	0.430	9.91	10.92
D3	0.300 typ.		7.62 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

REVISION HISTORY

Date	Revision	Description
January 2003	Rev 4.0.0	Changed to standard style format. Clarified that the TX interrupt is not MS Windows compatible. Clarified timing diagrams. Renamed Rclk (Receive Clock) to Bclk (Baud Clock) and timing symbols. Added T_{AH}, T_{CS} and OSC.
April 2003	Rev 4.0.1	Updated Ordering Information.
September 2003	Rev 4.1.0	Added Status Column to Ordering Information.

NOTICE

Datasheet September 2003.

Send your UART technical inquiry with technical details to hotline: uarttechsupport@exar.com.