iATC 29C48
FEATURE CONTROL COMBO

- **External and User Programmable Transmit and Receive Gain**
- **Programmable External Hybrid Balance Network Select**
- **Programmable Analog, Digital and Subscriber Loopback**
- **Programmable μ/A-Law Select**
- **Secondary Analog Input Channel**
- **Low Power Consumption**
- **External Tone Injection to Receive Path**
- **SLD A/B Channel Select (for 16 Channel Line Cards)**

The Intel iATC 29C48 Feature Control Combo is a low cost, user-programmable, fully integrated PCM Codec with transmit/receive filters fabricated in a CMOS technology. This technology is built on CHMOS and will allow the 29C48 to realize the same excellent transmission performance as in the Intel 2913/2914 combo while achieving the low power consumption typical of CMOS circuits.

The 29C48 supports the analog subscriber with a variety of added per-line features to the normal BORSCHT functions associated with the analog line circuit. Some of these features include secondary analog input channel, programmable transmit and receive gain, custom hybrid balancing network selection, and programmable μ or A-law conversions. Additionally, the 29C48 can operate on either the A or B channel of the SLD interface, allowing two combos to be connected to one SLD link. In order to facilitate the SLIC interface in this configuration, the 29C48 generates SLIC chip select signals for the proper routing of signaling information.

A unique feature of the 29C48 is programmable tone injection. This feature and its SLD interface makes it particularly easy to use in conjunction with Intel's advanced transceivers, such as the iATC 29C53AA, in subscriber equipment environments. The 29C53AA handles transfer of voice and feature control information to the 29C48.

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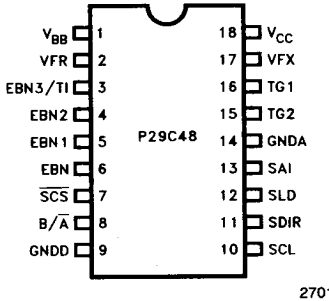
18-Lead Plastic Dual-In-Line Package



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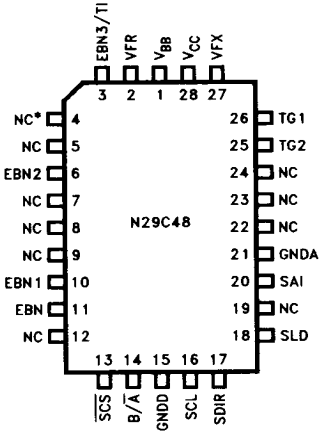
Plastic Leaded Chip Carrier



*Not connected

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Figure 1. Pin Configurations

October 1991
Order Number: 270153-007

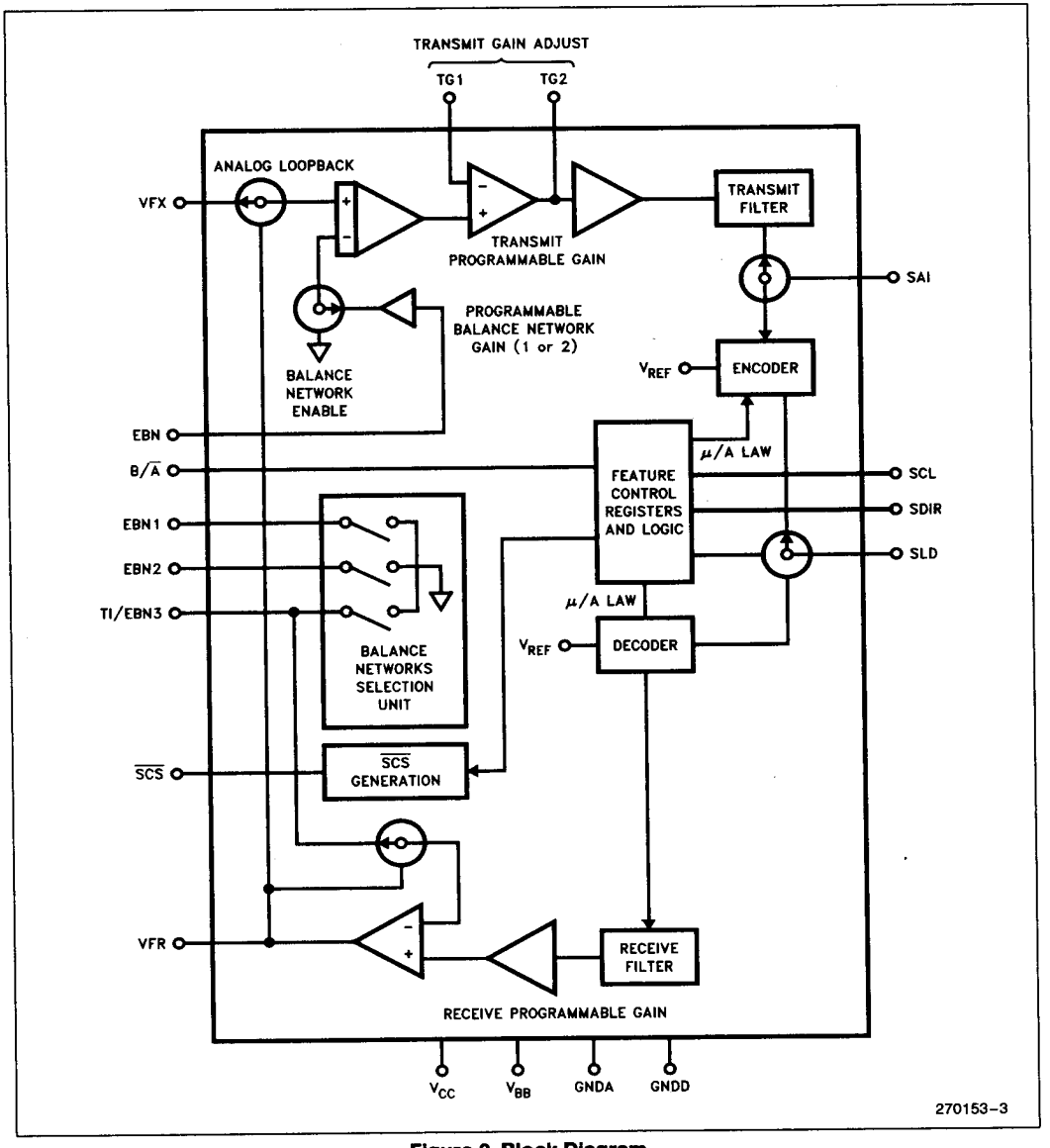

Figure 2. Block Diagram

Table 1. Pin Names

VFX	Analog Input	SCL	Subscriber Clock
VFR	Analog Output	SLD	Subscriber Data Link
GNDD	Digital Ground	SDIR	Subscriber Direction
GNDA	Analog Ground	TG1, TG2	Transmit Gain Adjust
VCC	Power (+5V)	EBN1/2	External Balance Network Selection Inputs
VBB	Power (−5V)	EBN3/T1	External Balance Network Selection Input or Tone Injection
B/$\overline{A}$	Channel Selection		
$\overline{SCS}$	SLIC Chip Select	EBN	External Balance Input
		SAI	Secondary Analog Input

Table 2. Pin Description

Symbol	Function
VCC	Most positive supply; input voltage is +5V ±5%.
VBB	Most negative supply; input voltage is −5V ±5%.
GNDA	Analog ground return line. Not internally connected to GNDD.
GNDD	Digital ground return line. Not internally connected to GNDA.
VFX	Analog voice input to transmit channel. Input impedance is typically larger than 100 KΩ.
TG1	Inverting input to transmit gain adjusting op-amp. Feedback point for external gain adjusting resistor network or frequency compensation network. Input impedance is typically larger than 10 MΩ.
TG2	Output of the transmit gain adjusting op-amp. Will drive external gain adjusting resistor network as well as frequency compensation network with an impedance of at least 10 KΩ.
VFR	Receive voice output. Capable of directly driving transformer hybrids or impedance loads of 600Ω.
EBN	Input to the hybrid balancing circuit. Input impedance is typically larger than 10 MΩ.
EBN1	Input connected to a grounded switch. The switch's on resistance is not greater than 600Ω.
EBN2	Input connected to a grounded switch. The switch's on resistance is not greater than 600Ω.
EBN3/T1	This pin is multiplexed according to the feature control registers. When programmed to be EBN3, it is an input connected to a grounded switch. The switch's on resistance is not greater than 600Ω. If this pin is programmed to be TI, an analog signal applied on this pin will be added to the received voice signal before the receive power amplifier.
SCL	Subscriber clock. This is an input which should be 512 KHz with a duty cycle ranging from 25% to 75%. Input will accept TTL levels.
SDIR	Subscriber direction signal and frame sync input. When high, SLD becomes an input and data is received by the 29C48. When low, the output buffer on the 29C48 SLD pin is enabled and data is transmitted by the 29C48. Input will accept TTL levels.
SLD	Subscriber Line Datalink. A 512 Kbps bi-directional seral data port, which is clocked by SCL. SLD becomes a TTL compatible input when SDIR is high and an output capable of driving one TTL load when SDIR is low, during the appropriate SLD fields for the assigned channel.
B/$\overline{A}$	Pin strapped to assign the 29C48 to process either A or B channel information from the SLD bus. A low level (GNDD) on this pin selects channel A, a high level (VCC) channel B.
$\overline{SCS}$	This pin is TTL compatible output capable of driving one TTL load: when low, it informs a SLIC device connected to the same SLD bus as the 29C48 that it can process the receive and transmit signaling data of the present SLD frame.
SAI	Secondary analog input.

FUNCTIONAL DESCRIPTION

The 29C48 is a combined channel filter and PCM codec for use in ISDN subscriber equipment or analog line interface circuit boards in digital switching systems.

The 29C48 incorporates features which make it particularly suited to subscriber applications. Tone injection allows easy implementation of DTMF feedback and side tone injection, and secondary analog signal input allows remote control and monitoring.

(See Figure 3 for a typical ISDN subscriber equipment application.)

For analog line interface circuit boards this device resides between the circuitry which provides the "BORSHT" functions for a given line, and the shared line board controller. It provides the transmit and receive voice-path filtering and companded analog-to-digital and digital-to-analog conversions necessary to interface a full duplex voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. (See Figures 4a and 4b for typical line card applications.)

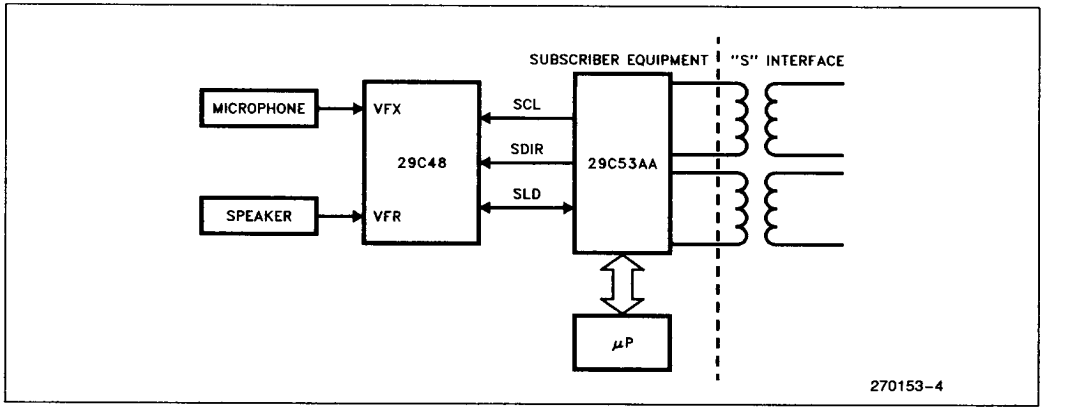

Figure 3. Subscriber Equipment

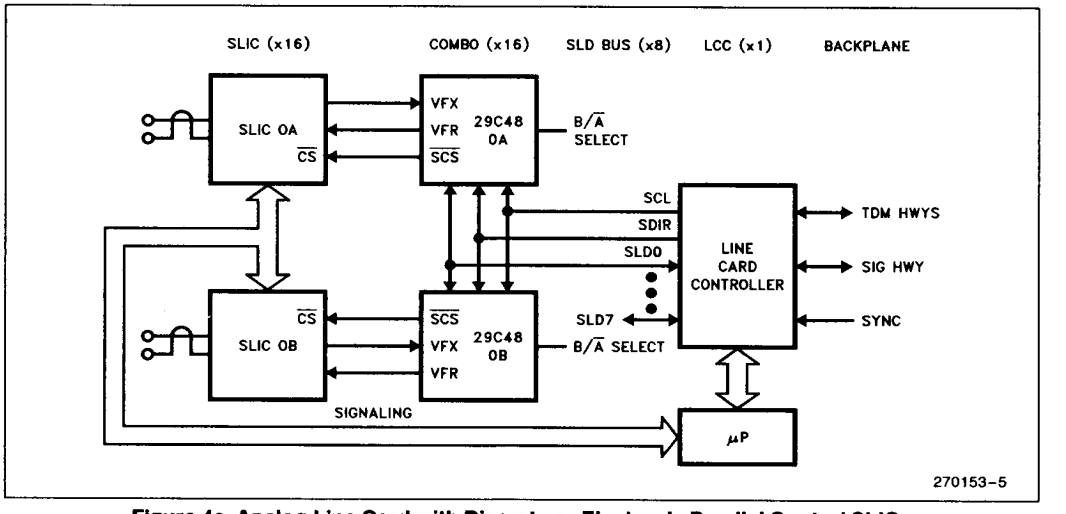

Figure 4a. Analog Line Card with Discrete or Electronic Parallel Control SLICs

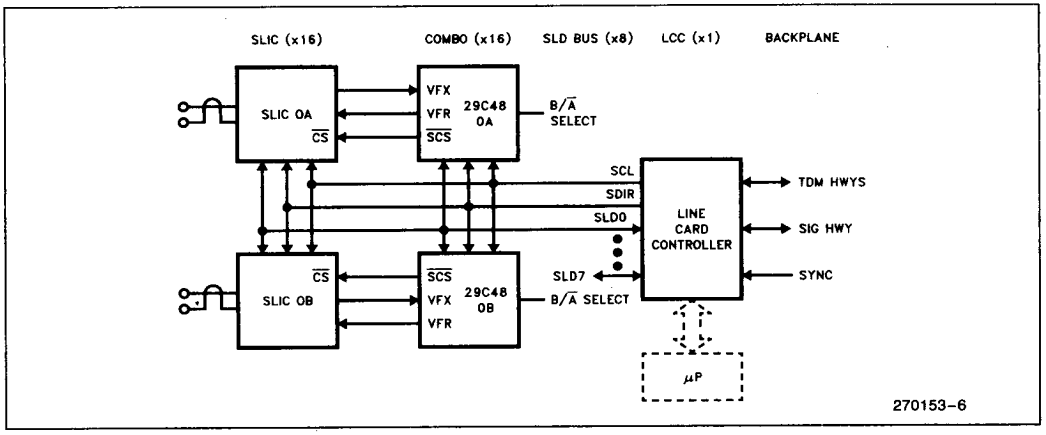

Figure 4b. Analog Line Card with SLD Compatible SLICs

TRANSMIT AND RECEIVE OPERATION

Transmit Filter

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 specification and the CCITT G.714 recommendation. The 29C48 specifications meet the digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 12.

A high pass section configuration rejects low frequency noise from 50 Hz and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. The transmit filter also provides additional loss at 12 KHz and 16 KHz to support metering pulses.

Encoding

The output of the transmit filter or the secondary analog input is internally sampled by the encoder and held on an internal sample and hold capacitor. DC offset is corrected by an no-chip auto zero circuit. The signal is then encoded and presented as PCM data on the SLD lead. (First or second byte of the transmit half-frames depending upon the channel assignment of the device.)

Decoding

The PCM word received on the SLD lead (first or second byte of the receive half-frame, depending upon the channel assignment of the device) is sent to the decoder after a serial to parallel conversion. The decoded value is held on an internal sample and hold capacitor.

Receive Filter

The receive section of the filter provides a passband flatness and stopband rejection which fulfills the AT&T D3/D4 specification and the CCITT G.714 recommendation. It also provides additional loss at 12 KHz and 16 KHz. The receive filter transfer characteristics and specifications will be within the limits shown in Figure 13.

GENERAL OPERATION

External Gain Setting

Both transmit and receive gain levels can be modified by external resistors during line card assembly. The value of transmit gain is adjusted by connecting resistors RT1 and RT2 (see Figure 5) at the two external gain setting control pins, TG1 and TG2. These two pins are the input and output of an on-board gain amplifier stage, and the resistors provide the necessary input and feedback for gain control. External gain of up to 20 dB can be set without degrading the performance of the amplifier. The value of external gain is given by:

$$A = 1 + RT1/RT2$$

For unity gain, pins TG1 and TG2 are tied together.

For the receive section, the external gain can be set by the external resistors, RR1 and RR2. There are two possible ways of implementing the gain control. The first is illustrated in Figure 6a, where the value of the receive gain is given by:

$$A = RR2/(RR1 + RR2)$$

The value of RR1 + RR2 should not be less than 600Ω to avoid degrading the output power stage's performance. The second way of implementing the receive gain is shown in Figure 6b, where pin EBN3/T1 is used. The value of the receive gain in this configuration is given by:

$$A = 1 + RR1/RR2$$

Hybrid Balancing Network

Three external balancing networks can be applied to the 29C48 by the user to accommodate varying subscriber loop characteristics (see Figure 7 for external connections). Feature control allows the grounding of any combination of these networks in order to best suit a particular application. Feature control also allows the user to select a gain of 0.0 dB or +6.0 dB in the balance signal path to suit the type of SLIC used.

FREQUENCY COMPENSATION

The user may, if desired, compensate for the frequency response characteristics of the SLIC by adjusting the frequency response of the transmission chain. This can be accomplished in the same way as the external gain setting is done in the transmit and receive directions. But, instead of using purely resistive impedances, resistor and capacitor networks have to be used to achieve complex impedances. The two compensation schemes are shown in Figures 8a and 8b. The gains in the transmit and receive directions are repectively:

for Figure 8a $A = 1 + ZX1/ZX2$

for Figure 8b $A = 1 + ZR1/ZR2$

SECONDARY ANALOG INPUT

Although the main application of the 29C48 will be for voice transmission, it also offers a secondary unfiltered input channel. Narrow band analog signals can be supplied through this channel for remote loop testing and various control uses.

The secondary analog input channel is accessed under software control through the SAI input. When the SAIE bit in the feature control register #3 is set to a

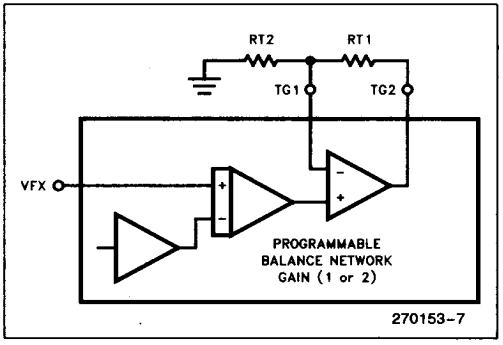

Figure 5. Transmit Gain Setting

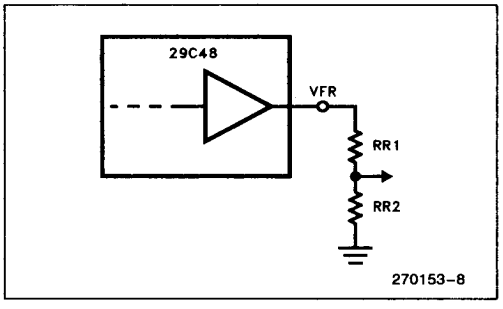

Figure 6a. Receive Gain Setting

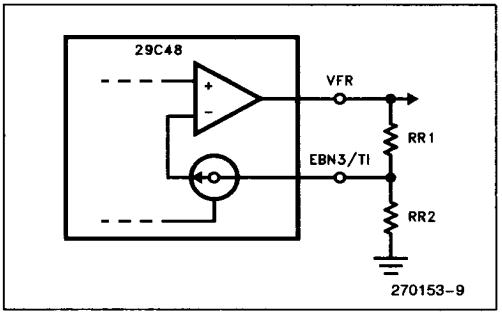

Figure 6b. Receive Gain Setting

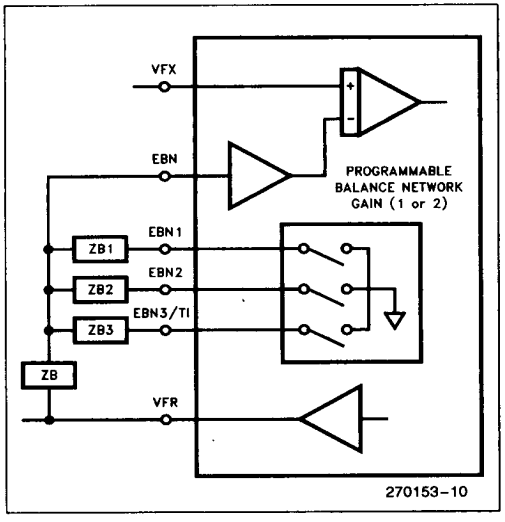

Figure 7. Balance Networks

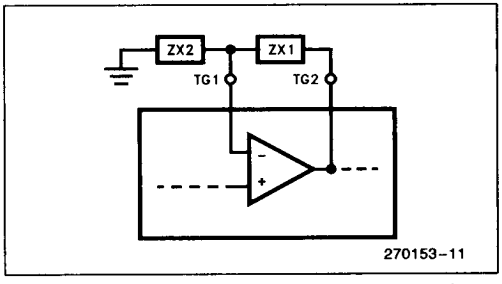

Figure 8a. Transmit Frequency Compensation

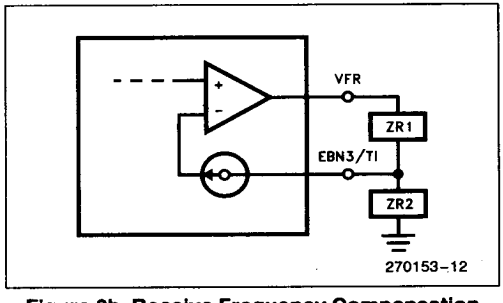

Figure 8b. Receive Frequency Compensation

logical one, the 29C48 will encode and transmit the signal present at the SAI input. The 29C48 will switch back to transmission of the voice signal as soon as the SAIE bit is set back to a logical zero.

TONE INJECTION

When specified by the feature control memory, an audio frequency signal applied to the EBN3/T1 pin will be added to the receive invoice signal at the power amplifier. This feature allows easy implementation of DTMF feedback and side tone injection in ISDN telephone applications, as well as injection of call waiting or metering tones in line card applications. A typical application is shown in Figure 9. Here VFR is the combination of the receive voice signal (V0) and two tones (V1 and V2).

$$VFR = 2V0 - (V1 + V2)/2$$

CHANNEL ASSIGNMENT

Two 29C48s can be attached to the same SLD line to exchange information with the SLD master during each SLD frame.

The B/$\overline{A}$ pin of the 29C48 is used to assign a voice channel of the SLD frame to the device. When the B/$\overline{A}$ pin is tied low, the 29C48 operates as an A-channel combo, receiving and transmitting voice during the first and fifth bytes of the SLD frame. When this pin is tied high, the 29C48 operates as a B-channel combo, receiving and transmitting voice during the second and sixth bytes of the SLD frame.

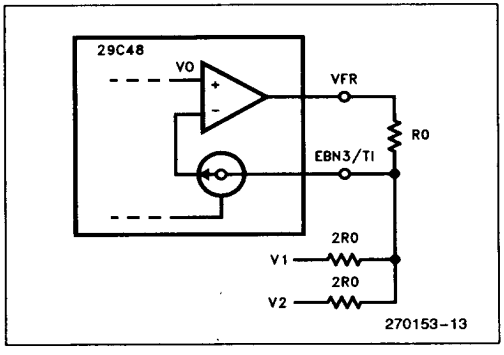

Figure 9. External Tone Injection

The feature control receive and transmit channels of the SLD frame are shared by the two 29C48s. A 29C48 will accept or return feature control information only if it has been instructed to do so during the first byte of a feature control frame. This is accomplished by setting the logic level of the channel selection bit (LSB) in feature control byte #1 to match the logic level of the B/$\overline{A}$ pin of the appropriate 29C48. The selected 29C48 will keep exchanging feature control information until a new framing byte makes a F/new selection. The status of the channel selection bit is sent back during the seventh byte of the SLD frame in which a 00 was received in the F/WE bits of the 3rd byte of the same SLD frame.

The 29C48 does not process data received in the signaling channel. However, it generates chip select signals during the appropriate time slots in order to facilitate the SLIC interface. (See section on SLIC Chip Select.) The 29C48 enters into a high impedance state during the signaling transmit channel, the eighth byte of the SLD frame.

SLIC Chip Select

In order to facilitate interfacing to an SLD compatible SLIC, especially when two SLICs share the same SLD line, the 29C48 includes a programmable chip select signal.

During the receive cycle of the SLD frame, the $\overline{SCS}$ pin of the 29C48 whose channel selection pin (B/$\overline{A}$) has the same logic state as the channel selection bit (see previous section on Channel Assignment) is pulled low during the receive signaling byte.

During the transmit cycle of the SLD frame, the $\overline{SCS}$ signal can operate in two modes. In the first mode, called "byte mode", the $\overline{SCS}$ pin of the selected 29C48 is pulled low during the transmit signaling byte, as described above for the receive direction.

A second mode, called the "half-byte mode", is provided. In this mode, during the transmit cycle of the SLD frame, the $\overline{SCS}$ pin of the channel A combo is pulled low during the least significant four bits (last four bits) of the transmit signaling byte. During the same frame, the $\overline{SCS}$ pin of the channel B combo is pulled low during the most significant four bits (first four bits) of the transmit signaling byte. This allows signaling data from both A and B channel SLD compatible SLICs to be processed by a line card controller during the same frame.

To minimize power consumption, operation of the $\overline{SCS}$ signal during the receive half of the SLD frame can be disabled through the feature control memory. Operation of this signal in the transmit direction remains unaffected to allow continued monitoring of subscriber status by a line card controller. The $\overline{SCS}$ signal remains active in the power down mode.

The eight possible sequences for $\overline{SCS}$ are shown in Figure 10.

Precision Voltage References

Voltage references are generated on-chip and are trimmed during the manufacturing process. Separate references are supplied for both the transmit and receive sections of the chip, each trimmed independently. These references determine the gain and dynamic range of the device and provide the user a significant margin for error in other board components.

SLD Interface

The 29C48 is intended for use with the 29C53AA ISDN transceiver or a SLD compatible line card controller. They manage the transfer of all voice and feature control data to and from the Feature Control Combo. The interface between the two consists of just three leads, two of which are clock signals and the third a serial bus for communication.

The subscriber direction (SDIR) lead provides an 8 KHz signal which divides each frame into transmit and receive halves. During the first half when SDIR is high (RCV half-cycle), the 29C48 receives data and in the second (XMIT half-cycle) the 29C48 transmits data. Frame synchronization and all internal timing for the digital circuitry is derived from the rising edge of the SDIR signal.

The subscriber clock (SCL) input generated by the 29C53AA is a fixed 512 KHz clock signal allowing 64 bits (8 bytes) of data to be transferred on the SLD lead during each 125 μs frame. The SCL duty cycle can range from 25% to 75%.

The Subscriber Line Datalink (SLD) is a bi-directional serial bus that transfers four bytes of serial data to and from the 29C48 each frame. During the first half of each frame, RCV channel information is expected by the 29C48 as one byte consisting of voice and one byte of feature control information, while the other two bytes of the RCV half-frame are simply ignored. Similarly, during the second half-frame, one

byte of voice and, if so instructed, one byte of feature control information is sent by the 29C48. The 29C48 places its SLD lead in a high impedance state while the other device connected to the SLD line transmits its own information, and also while the one byte of signaling information is transmitted by an SLD compatible SLIC. The most significant bit (bit 7) of each byte is sent first on the SLD line. The data format of an SLD frame is shown in Figure 11.

Upon power supply application, feature control read or write of the 29C48 is disabled for 9 SLD frames. During this time, the 29C48 resets and enters the power down mode. The $\overline{SCS}$ output remains high until the 29C48 has been configured as an A or B channel device by the first write to feature control byte #1.

PROGRAMMABLE FEATURES

The 29C48 is configured by a set of five feature control bytes (FCB).

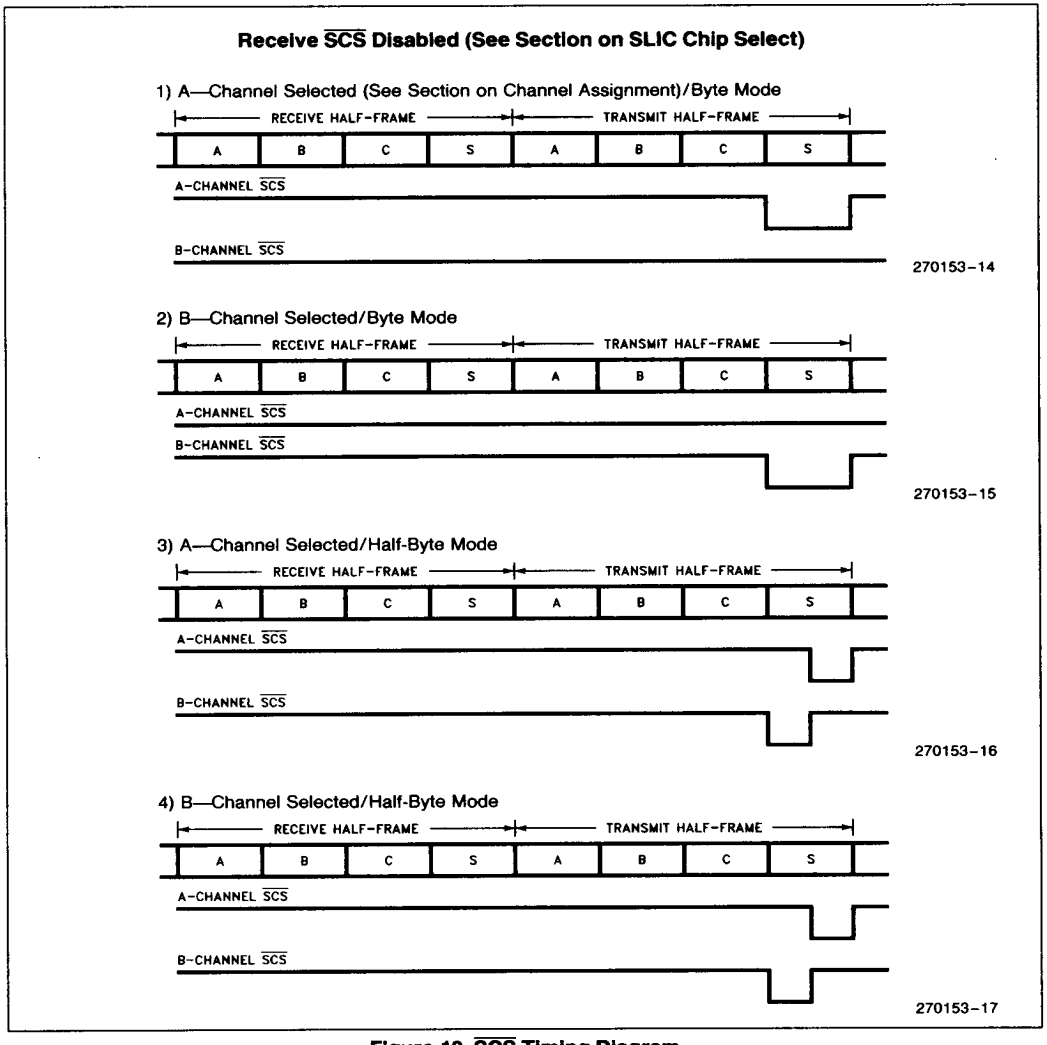

Figure 10. $\overline{SCS}$ Timing Diagram

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These bytes of information are stored in internal registers which are serially multiplexed to and from the SLD interface in the third and seventh byte locations. The first two bits of each byte consist of a multiframe synchronization and write enable code. The framing bit (bit 7, MSB) establishes the beginning of a feature control frame when set to a logical zero, and increments the feature control counter when set to one. The second (bit 6) enables the writing to the 29C48 when it is the logical complement of the framing bit. In addition to the two header bits, feature control byte #1 also includes a channel selection bit (bit 0, LSB). This bit is used to designate one of the two 29C48s sharing an SLD link for feature control information exchange. (See previous section on channel assignment.)

When writing new feature control information to the 29C48, the first byte should contain a framing (F) and write enable (WE) header of 01 (F = 0 and WE = 1), and an appropriate channel selection bit. This designates a new frame of information to transfer. The subsequent bytes should each have F = 1 to advance the counter, and WE = 0 to enable the write operation.

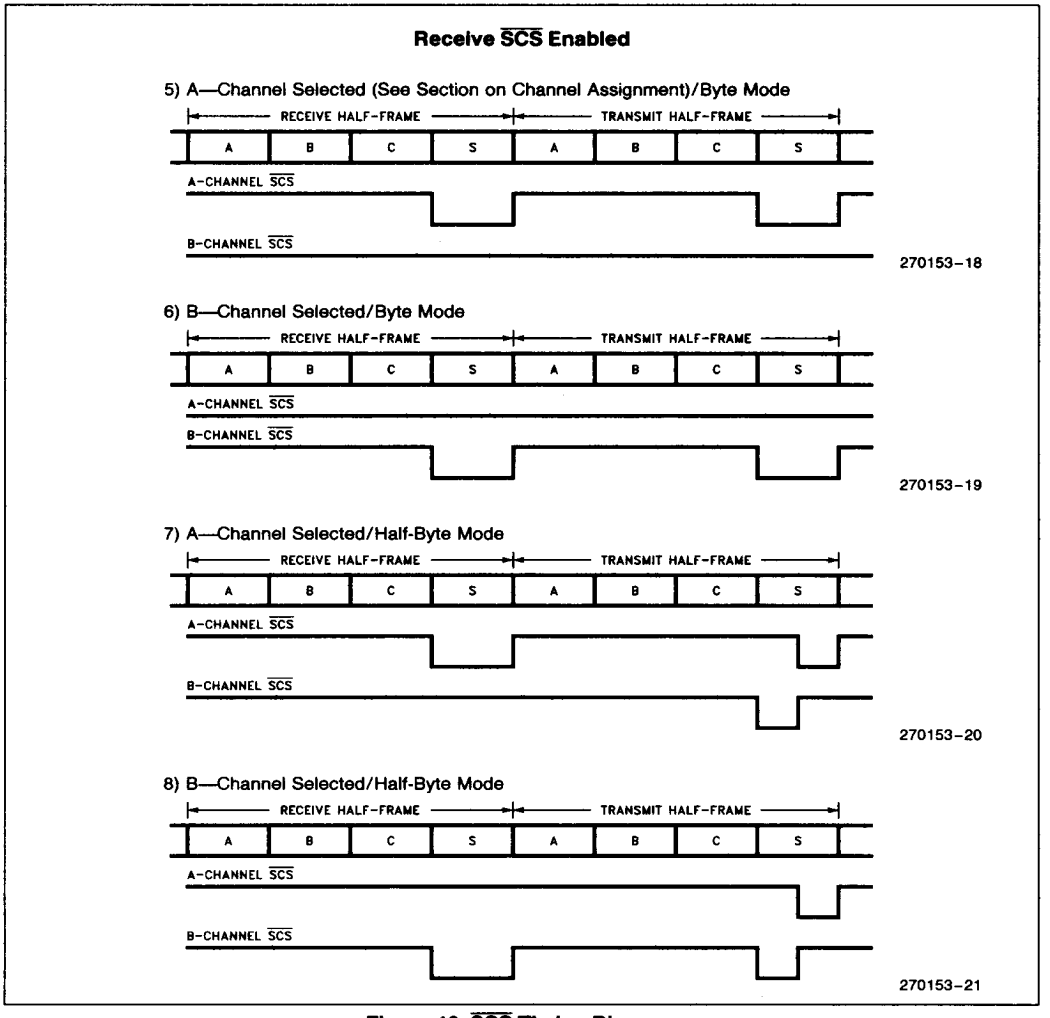
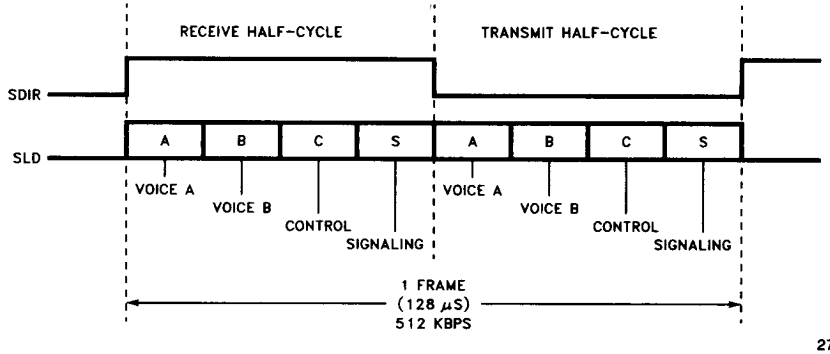


Figure 10. SCS Timing Diagram



NOTES:
Voice A, Voice B: A and B channel voice bytes respectively.
Control: Feature control information. This information is exchanged with the 29C48 whose channel selection pin matches the channel selection bit of the latest framing feature control byte.
Signaling: Signaling information which controls the subscriber line. The 29C48 enters into a high impedance state during the transmit signaling time slot, and generates a chip select signal (see section on SLIC chip select).

Figure 11. 29C48 SLD Interface

The SLD master can also request to verify the feature control register contents by sending a 00 or 11 at the beginning of the byte to be read. To read the first byte, a 00 F/WE code and an appropriate channel selection bit should be sent while each subsequent byte should have a 11 header. An internal six-stage counter is set on the first byte verified then incremented once each 125 μs frame. It is reset only upon detection of a 01 or 00 F/WE. Once the counter is greater than five, neither read nor write modes may be selected by sending the 29C48 a 11 or 10 framing and write enable code. While in this state, the 29C48 will then echo in byte 7 the data it received in byte 3. Another feature control information exchange cycle can only be initiated by establishing a new feature control frame (sending F = 0).

FCB # 1—Power Up/Down, Loop Back Mode, μA/-Law, Channel Select Register

POWER UP AND DOWN

The 29C48 can be instructed to go into the power down or standby mode for reduced power consumption. In this mode, all analog inputs and outputs are placed in a high impedance state, inhibiting voice signals. A code of all ones will be output in the voice byte on the SLD. Signaling and feature control information will continue to be processed to allow the 29C48 to be read or reprogrammed.

The state of the feature control combo can be changed from standby to active by the first feature control byte only. All other register contents will be preserved during power down provided the power supplies remain connected.

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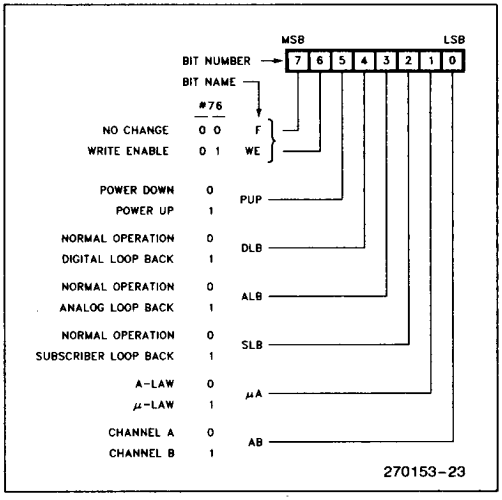
LOOP BACK MODE SELECT

Three modes of remote testing are incorporated in the 29C48 and can be selected by appropriate coding in this register. The loopback features allow a number of tests to be performed to determine line quality and balancing. These include digital loop back, analog loop back, and subscriber loop back.

In the digital loopback mode, the combo retransmits the PCM word it receives in the voice A or B byte of the SLD back to the SLD master in the same frame. This feature allows path verification and testing of the circuit up to the combo.

When the analog loopback mode is selected, the analog output VFR is internally connected to the analog input VFX. This feature allows functional testing of the combo as well as gain adjustment.



In the third test mode, subscriber loopback, the digital output of the A/D converter is internally connected to the input of the D/A converter. The analog signal input to VFX is sent through the transmit filter, encoded, then decoded, filtered and output to VFR. This mode is used primarily for simplifying analog to analog testing from the subscriber side of the line card. Simultaneous selection of more than one loopback mode is prohibited.

CONVERSION LAWS

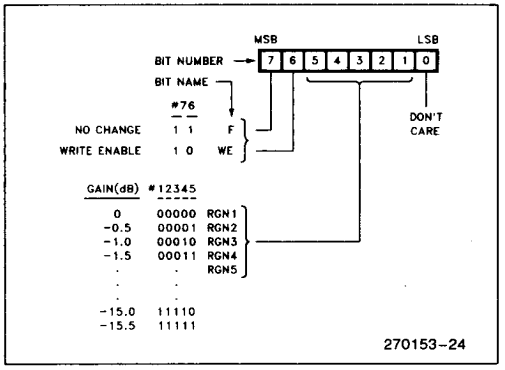
The 29C48 can be selected for either μ-law or A-law operation. A user can select either conversion law by assigning the corresponding bit. A logical 1 in bit 1 would select μ-law while a logical 0 would select A-law conversions. Both conversions follow CCITT recommendation G.711.

FEATURE CONTROL EXCHANGE CHANNEL SELECT

The LSB of feature control byte #1 is the channel selection bit. It is used to select one of the two 29C48s sharing an SLD line for feature control information exchange. A logical zero will select the channel A combo, and a logical one will select the channel B combo.

FCB #2—Receive Programmable Gain Register

The receive gain levels can be adjusted by applying external resistors as mentioned earlier, or by selective programming of this register. A range from 0 to −15.5 in 0.5 dB increments can be set for the receive channel.



FCB #3—Secondary Analog Channel, Chip Select, and Tone Injection Register

SECONDARY ANALOG INPUT

The 29C48 can be instructed to switch the input of its encoder to the secondary analog input by setting the SAIE bit to a logical one. Transmission of the voice signal will resume as soon as SAIE is set back to a logical zero.

PROGRAMMABLE SLIC CHIP SELECT

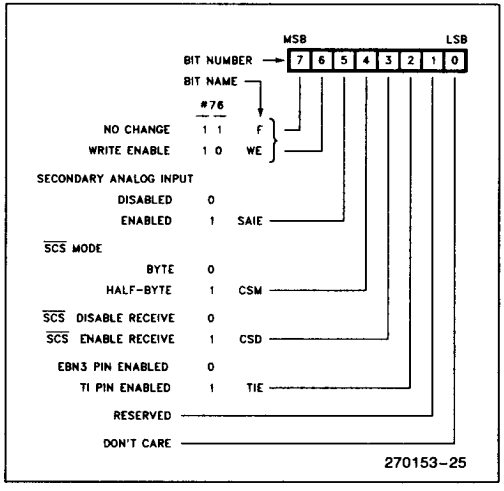
Although the 29C48 does not process signaling information, it generates chip select signals in order to help in interfacing to SLD compatible SLICs.

During the transmit half-frame, the chip select works in two possible modes determined by the CSM bit. In the byte mode, the $\overline{SCS}$ pin of the 29C48 selected by the channel selection bit in feature control byte #1 will be pulled low during the transmit signaling byte. In the half-byte mode, the $\overline{SCS}$ pin of the A-channel 29C48 will be pulled low during the four least significant bits of the transmit signaling byte, and the $\overline{SCS}$ pin of the B-channel 29C48 will be pulled low during the four most significant bits of the transmit signaling byte.

Generation of chip select signals during the receive half frame can be disabled by setting the CSD bit to a logical zero.

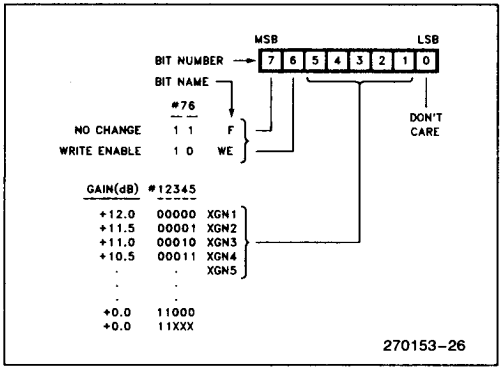
TONE INJECTION

When the TIE bit is set to a logical one, audio signal applied at the EBN3/T1 pin will be added to the output of the receive programmable gain module. This feature can be used for easy implementation of side tone injection and DTMF feedback, as well as injection at the line card of call waiting tones, ringing or metering pulses.



FCB #4—Transmitt Programmable Gain Register

The gain setting of the transmit section of the chip operates in the same manner as the receive gain register. A 12 dB range from 0.0 dB to +12.0 dB in 0.5 dB increments is available.



FCB #5—Balance Network Select and Gain Register

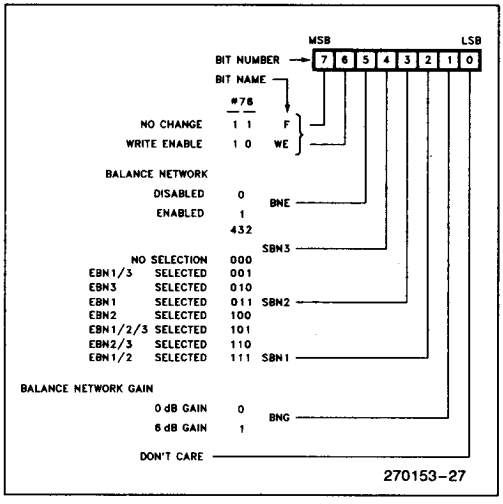
BALANCE NETWORKS

Three external balance networks can be used with the 29C48. Feature control allows the selection of network EBN1, EBN2, and EBN3 individually or in combination in order to best suit a particular application.

EBN3 selection is not effective when TIE is set to a logical one.

GAIN SETTING

An additional 6 dB gain in the balance signal path can be realized by setting the BNG bit to a logical one. A logical zero provides unity gain.



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ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
All Input and Output Voltages with Respect to VBB ..... −0.3V to +13V
All Input and Output Voltages with Respect to VCC ..... −13V to +0.3V
Power Dissipation 1.35W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, VCC = +5V ±5%, VBB = −5V ±5%; SCL (50% duty), SDIR, SLD applied GNDD = 0V, GNDA = 0V. Typical values are for T_A = 25°C and nominal power supply values.

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Leakage Current			±10	μA	$0 \le V_{IN} \le VCC$
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} \ge -1.6$ mA, 1 TTL Load
V_{OH}	Output High Voltage	2.4			V	$I_{OH} \le 50$ μA, 1 TTL Load

POWER DISSIPATION

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC1}	VCC Operating Current		6.0	10	mA	Idle Channel
I_{BB1}	VBB Operating Current		6.0	10	mA	Idle Channel
I_{CCO}	VCC Standby Current		0.3	1.0	mA	
I_{BBO}	VBB Standby Current		0.25	0.6	mA	

A.C. CHARACTERISTICS—TRANSMISSION PARAMETERS

(TG1 = TG2, Transmit Programmable Gain = 4 dB. Receive Programmable Gain = −3 dB)

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response Tolerance			±0.25	dB	Signal Input of 0 dBm0 f = 1.02 KHz
DmW	Digital Milliwatt Response Tolerance			±0.25	dB	f = 1.02 KHz Signal Input of 0 dBm0
$DmW_{\mu V}$	Digital Milliwatt Response VFR, μ-Law		3.11 1.108		dBm Vrms	R_L = 600Ω f = 1.02 KHz
DmW_{AV}	Digital Milliwatt Response VFR, A-Law		3.17 1.116		dBm Vrms	R_L = 600Ω f = 1.02 KHz

GAIN AND DYNAMIC RANGE (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
$OTLP_{\mu X}$	Zero Transmission Level Point Transmit Channel (0 dBm0)		2.09 0.985		dBm Vrms	μ-Law, Referenced to 600Ω
$OTLP_{AX}$	Zero Transmission Level Point Transmit Channel (0 dBm0)		2.15 0.992		dBm Vrms	A-Law, Referenced to 600Ω
ΔGp	Programmable Gain Accuracy			±0.20	dB	f = 1.02 KHz for All Steps Signal Input of 0 dBm0

GAIN TRACKING

Reference Level = 0 dBm0 at 1.02 KHz, TG1 = TG2, Transmit Programmable Gain = 4 dB, Receive Programmable Gain = −3 dB, CCITT G.714—Method 1

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
GT_T	Transmit Gain Tracking Error, Sinusoidal Input (+3 to −10 dBm0), Noise Signal Input (−10 to −55 dBm0); μ or A-Law			±0.3 ±0.4 ±0.7	dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0
GT_R	Receive Gain Tracking Error, Sinusoidal Input (+3 to −10 dBm0), Noise Signal Input (−10 to −55 dBm0); μ or A-Law			±0.3 ±0.4 ±0.7	dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0

ANALOG INTERFACE, RECEIVE CHANNEL

R_{OR}	Output Resistance, VFR		1		Ω	
V_{OSR1}	Output Offset, VFR		30		mV	Relative to GNDA
C_{LR}	Load Capacitance, VFR			100	pF	
V_{OR1}	Max Output Voltage Swing Across R_L, VFR		±3.2		V_p	$R_L \geq 600\Omega$(1)

ANALOG INTERFACE, TRANSMIT PRIMARY AND SECONDARY CHANNELS

I_{BX}	Input Leakage Current, EBN, TG1, T1			100	nA	Operating Range(2)
R_{IX1}	input Resistance, VFX		100		KΩ	
R_{IX2}	Input Resistance, EBN, TG1, TI		10		MΩ	
TGmax	Max Transmit Gain Adjust			20	dB	
V_{OTG}	Max Output Voltage Swing TG2			±1.6	V	$R_L \geq 10$ KΩ(3)
C_{LX}	Load Capacitance, TG2			20	pF	
R_{LX}	Load Resistance, TG2	10			KΩ	
R_{GND}	On Resistance to GNDA, EBN1, EBN2, EBN3		150	600	Ω	

NOTES:

1. The 29C48 power amplifier is designed to drive signals in excess of the maximum encoding level, which is 3.14 dBm0 for A-Law and 3.17 dBm0 for μ-Law.
2. $-3.2V < VFX, EBN, TI < +3.2V$; $-1.6V < TG1 < +1.6V$.
3. Transmit programmable gain must be set to 0 dB to encode this level without clipping in later stages.

DISTORTION (Primary Channel)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
SD_X SD_R	Signal to Distortion, μ or A-Law, Sinusoidal Input (0 to −10 dBm0), Noise Signal Input (−10 to −55 dBm0); CCITT G.714—Method 1 Half Channel	35.4 33.7 29.1 14.1			dB dB dB dB	0 to −27 dBm0 −27 to −34 dBm0 −34 to −40 dBm0 −40 to −55 dBm0
DP_X DP_R	Single Frequency Distortion Products in Band (2nd or 3rd Harmonic Half Channel)		−60	−47	dBm0	Input = 1.02 KHz 0 dBm0 AT&T Advisory #64 (3.8)
IMD_1	Intermodulation Distortion, End to End Measurement			−35	dB	CCITT G.712 (7.1)
IMD_2	Intermodulation Distortion, End to End Measurement			−49	dBm0	CCITT G.712 (7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			−25	dBm0	CCITT G.712(6.1)
SIS	Spurious in Band Signals, End to End Measurement			−40	dBm0	CCITT G.712(9)
D_{AX}	Transmit Absolute Group Delay		220		μs	0 dBm0, 1.4 KHz Includes Delay through A/D
D_{DX}	Transmit Differential Delay; Relative to DAX		170 95 45 75		μs μs μs μs	f = 500–600 Hz f = 600–1000 Hz f = 1000–2600 Hz f = 2600–2800 Hz
D_{AR}	Receive Absolute Group Delay		140		μs	0dBm0, 0.3 KHz Includes Delay through D/A
D_{DR}	Receive Differential Envelope Delay; Relative to DAR		35 35 110 135		μs μs μs μs	f = 500–600 Hz f = 600–1000 Hz f = 1000–2600 Hz f = 2600–2800 Hz

NOISE (Primary Channel)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
N_{XC1}	Transmit Noise, C-Message Weighted			15	dBrnC0	TG1 = TG2; Transmit Programamble Gain = 4 dB
N_{XP1}	Transmit Noise, Psophometrically Weighted			−78	dBm0p	TG1 = TG2; Transmit Programmable Gain = 4 dB
N_{RC1}	Receive Noise, C-Message Weighted			15	dBrnC0	Unity Gain; Idle Code; Receive Programmable Gain = −3 dB
N_{RP1}	Receive Noise, Psophometrically Weighted			−76	dBm0p	Unity Gain; Idle Code; Receive Programmable Gain = −3 dB
$PSRR_1$	VCC or VBB Power Supply Rejection Transmit Channel		−40		dB	Idle Channel; 200 mV P-P Signal on Supply, DC to 50 KHz(1)
$PSRR_2$	VCC or VBB Power Supply Rejection Receive Channel		−40		dB	Idle Channel; 200 mV P-P Signal on Supply, DC to 50 KHz(1)

NOTE:
1. Measured at SLD Voice bytes for transmit channel. Measured at V_{FR} for receive channel. Idle code on feature control byte.

CROSSTALK

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
CT_{TR}	Crosstalk, Transmit Voice to Receive Voice		−90	−75	dB	Input = 0 dBm0, Unity Gain 1.02 KHz; Idle Code on SLD Voice Byte
CT_{RT}	Crosstalk, Receive Voice to Transmit Voice		−80	−72	dB	0 dBm0, 1.02 KHz Signal at SLD Receive Voice Byte; VFX = GNDA

TRANSMIT VOICE FREQUENCY CHARACTERISTICS
TG1 = TG2, Transmit Programmable Gain = 4 dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02 KHz					0 dBm0 Signal Input at VFX
	16.67 Hz			−30	dB	
	50 Hz			−25	dB	
	60 Hz			−23	dB	
	200 Hz	−1.8		−0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.70		−0.10	dB	
	4000 Hz			−14	dB	
	4600 Hz and above			−32	dB	

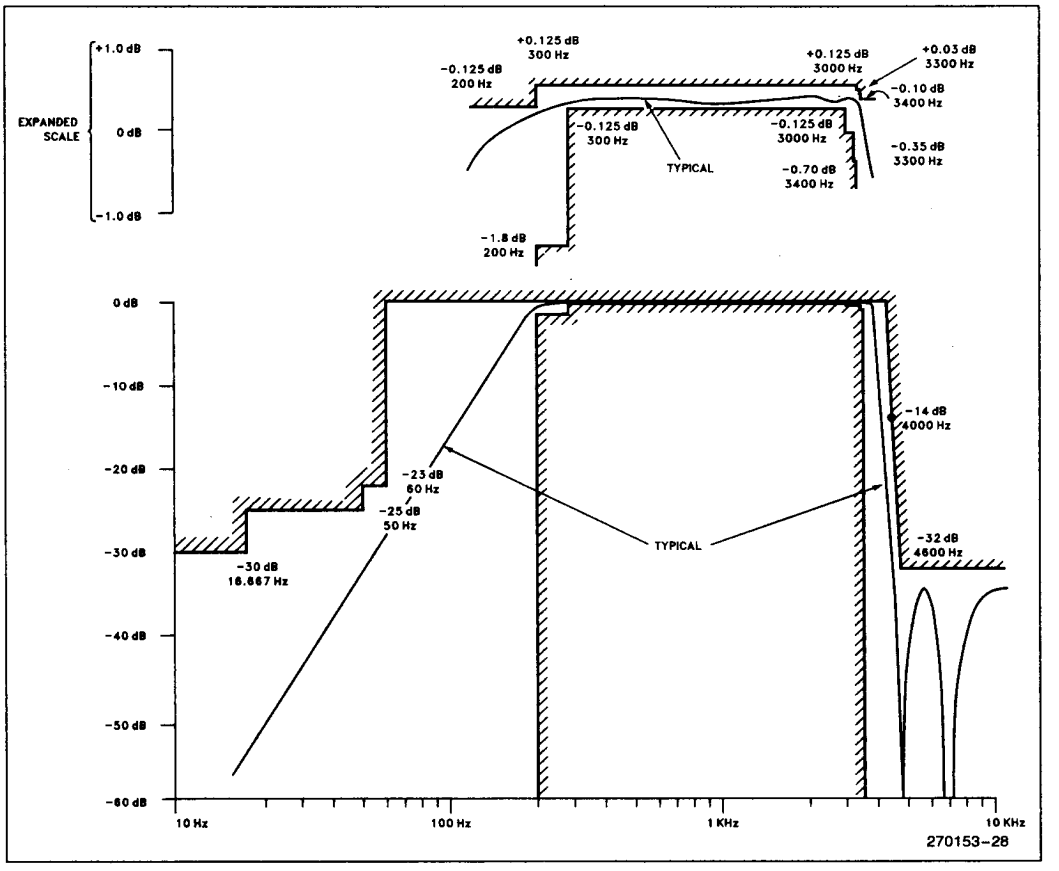
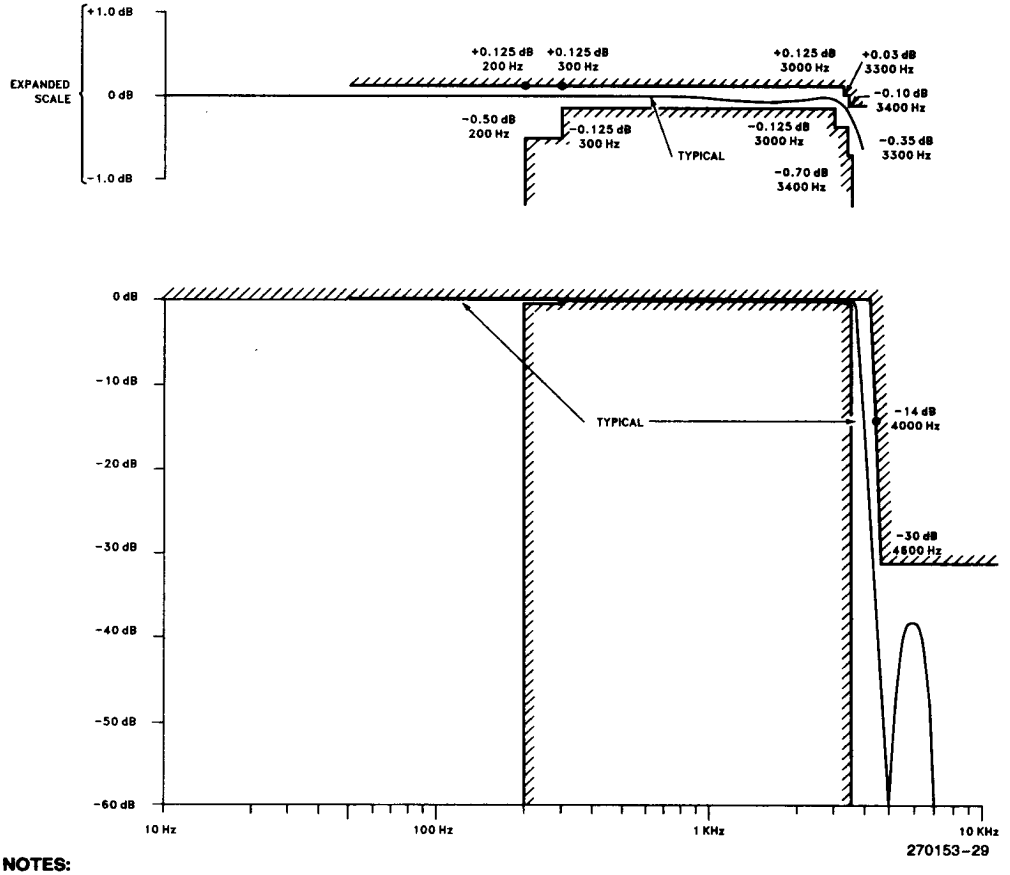


Figure 12. Transmit Voice Frequency Characteristics

RECEIVE VOICE FREQUENCY CHARACTERISTICS

Receive Programmable Gain = −3 dB, Feature Control Bit TIE = 0

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
G_{RR}	Gain Relative to Gain at 1.02 KHz					0 dBm0 Input SLD
	Below 200 Hz			+0.125	dB	
	200 Hz	−0.5		+0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.70		−0.1	dB	
	4000 Hz			−14	dB	
	4600 Hz and above			−30	dB	



NOTES:

1. Typical transfer function of the receive filter as a separate component.
2. Typical transfer function of the receive filter driven by the sample and hold output of the Intel 2910A and 2911A codecs. The combined filter/codec response meets the stated specifications.

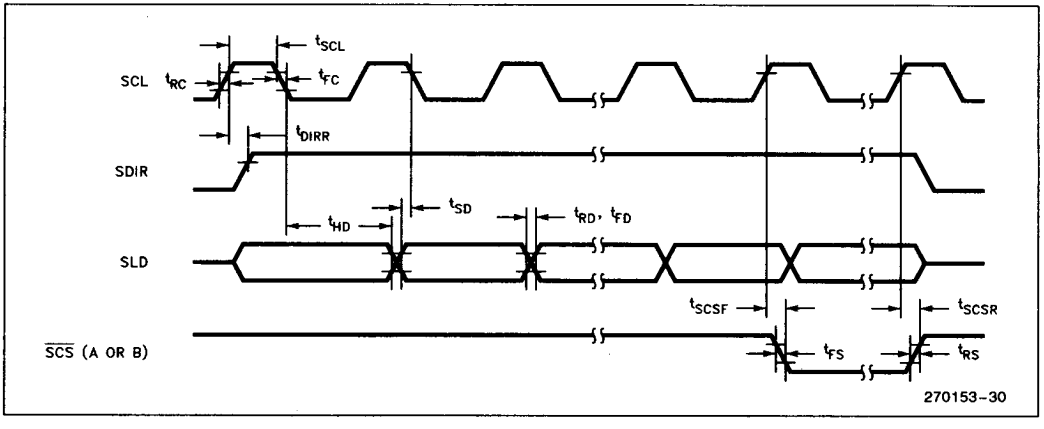
Figure 13. Receive Voice Frequency Characteristics

A.C. CHARACTERISTICS—TIMING PARAMETERS

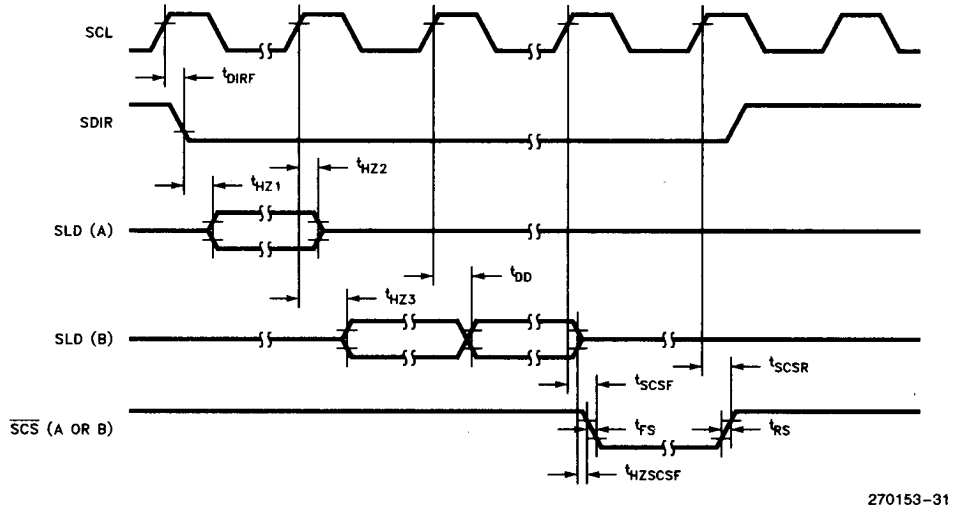
Symbol	Paramter	Min	Typ	Max	Units	Test Conditions
T_{SCL}	SCL Pulse Width	486		1465	ns	
T_{DC}	SCL Duty Cycle	25		75	%	
T_{RC} T_{FC}	Rise, Fall Times, SCL			50	ns	
T_{RD} T_{FD}	Rise, Fall Times, SLD			50	ns	
T_{RS} T_{FS}	Rise, Fall Times, $\overline{SCS}$			50	ns	50 pF Load
T_{DIRR}	SCL to SDIR Delay	−500		500	ns	Receive Cycle
T_{DIRF}	SCL to SDIR Delay	−500		500	ns	Transmit Cycle
T_{DD}*	SCL to SLD Delay	0		200	ns	29C48 Transmitting
T_{SD}	Set-Up Time, SLD to SCL	100			ns	29C48 Receiving
T_{HD}	Hold Time, SCL to SLD	100			ns	29C48 Receiving
T_{HZ1}	SDIR to SLD Active	0		100	ns	Byte 1, Bit 1 29C48 Transmitting, Channel A
T_{HZ2}	SCL to SLD High Impedance	0		100	ns	Channel A, B, or Feature Control as Appropriate (Channel A/B Operation)
T_{HZ3}	SCL to SLD Active	0		100	ns	Channel A, B, or Feature Control as Appropriate (Channel A/B Operation)
T_{SCSF}	SCL to $\overline{SCS}$ Low	TFS		250	ns	50 pF Load
T_{HZSCSF}	SLD High Impedance to $\overline{SCS}$ Low	0			ns	Transmit Feature Control
T_{SCSR}	SCL to $\overline{SCS}$ High	TRS		250	ns	50 pF Load

*In cases where T_{DIRF} is positive, T_{DD} is to be measured from the SDIR edge.

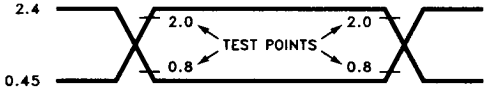
RECEIVE CYCLE



TRANSMIT CYCLE



A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing inputs are driven at 2.4 for a logic "1" and 0.45 for logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

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