16-bit cascadable arithmetic/logic unit

general information

The L4C381 is designed as a flexible, high speed 16-bit Arithmetic and Logic Unit slice. It combines four 381 type 4-bit ALUs, a lookahead carry generator, and miscellaneous interface logic into a single 68-pin package. While containing many new features to support high speed pipelined architectures and single 16-bit bus architectures, it retains full functional and performance compatibility with the bipolar 381 designs.

L4C381 architecture

The L4C381 operates on the 16-bit operands denoted A and B, and produces a single 16-bit result F. Three select lines control the ALU and provide 3 arithmetic, 3 logical, and 2 initialization functions. Full ALU status is provided, allowing the L4C381 to be cascaded to form longer word lengths. Registers are provided on both the ALU inputs and the output, but these may be bypassed under user control. An internal feedback path allows the registered ALU output to be routed to one of the ALU inputs accommodating chain operations and accumulation. Furthermore, the A or B input to the ALU can be forced to zero allowing unary functions to be performed on either operand.

ALU operation

Select lines S_{0-2} determine the operation to be performed. The ALU functions and their corresponding select codes are shown in figure 1.

S_2	S_1	S_0	FUNCTION
0	0	0	CLEAR (F = 00 . . . 0)
0	0	1	NOT(A) + B
0	1	0	A + NOT(B)
0	1	1	A + B
1	0	0	A XOR B
1	0	1	A OR B
1	1	0	A AND B
1	1	1	PRESET (F = 11 . . . 1)

Figure 1. ALU Function Definition

The functions B minus A and A minus B can be achieved by setting the carry input C_0 of the least significant slice and selecting codes 001 and 010 respectively.

ALU status

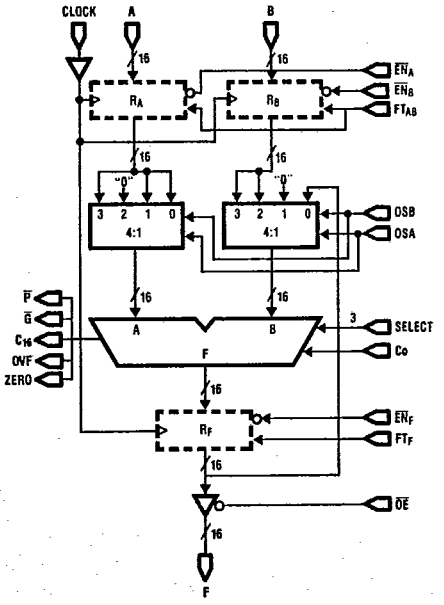
The ALU provides Overflow and Zero status bits. Also, Carry, Propagate, and Generate outputs are provided for cascading. These outputs are defined for the three arithmetic functions only. The ALU sets the Zero output when all sixteen output bits are zero. The Generate, Propagate, C_{16}, and OVF flags for the A + B operation are defined in figure 2. The status flags produced for NOT(A) + B and A + NOT(B) can be found by complementing A_i and B_i in figure 2 respectively.

operand registers

The L4C381 has two 16-bit wide input registers for operands A and B. These registers are rising edge triggered by a common clock. Each register is independently enabled by control signals $\overline{ENA}$ and $\overline{ENB}$.

features

- High-speed, 16-bit ALU
- Input and output registers can be made transparent
- Easily cascadable with or without carry lookahead
- Extension to 54S381 instruction set
- Force A or B → 0 allows two's complement, PASSA, PASSB instructions
- Internal feedback path for accumulation
- Low-power, high-speed CMOS technology
- All status and carry outputs available



L4C381 BLOCK DIAGRAM

absolute maximum ratings

Supply Voltage	– 0.5 to 7.0V
Input Voltage	0 to 5.5V
Output Voltage	0 to 5.5V
Operating Temperature (Ambient)	– 55°C to 125°C
Storage Temperature	– 65°C to 150°C

recommended operating conditions

PARAMETER		min	typ	max	unit
V_{CC}	Supply Voltage Commercial	4.75	5.0	5.25	V
V_{CC}	Supply Voltage Military	4.50	5.0	5.5	V
I_{OL}	Low Level Output Current			8.0	mA
I_{OH}	High Level Output Current			– 2.0	mA
T_{AMB}	Operating Temperature (Commercial)	0	25	70	°C
T_{AMB}	Operating Temperature (Military)	– 55	25	125	°C

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Bit Carry Generate = $g_i = A_iB_i$, for i = 0,1, . . . ,15

Bit Carry Propagate = $p_i = A_i + B_i$, for i = 0,1, . . . ,15

$P_0 = p_0$

$P_i = p_i(P_{i-1})$ for i = 1,2, . . . ,15

and

$G_0 = g_0$

$G_i = g_i + p_i(G_{i-1})$ for i = 1,2, . . . ,15

$C_i = G_{i-1} + P_{i-1}(C_{i-1})$ for i = 1,2, . . . ,15

then

$\overline{G} = NOT(G_{15})$

$\overline{P} = NOT(P_{15})$

$C_{16} = G_{15} + P_{15}C_{15}$

$OVF = C_{15}$ XOR C_{16}

Figure 2. ALU Status Flags

pin definitions

A_{0-15}	A Input
B_{0-15}	B Input
F_{0-15}	Result Output
C_0	Carry Input
C_{16}	Carry Output
$\overline{P}$	Carry Propagate Output
$\overline{G}$	Carry Generate Output
OVF	ALU Overflow Flag
ZERO	ALU Result Zero Flag
$\overline{ENA}$	A Register Enable
$\overline{ENB}$	B Register Enable
FT_{AB}	A, B, Register Feedthrough Control
$\overline{ENF}$	F Register Enable
FT_F	F Register Feedthrough Control
OS_B	B Operand Select
OS_A	A Operand Select
I_{0-2}	Instruction Select
$\overline{OE}$	Output Enable
CLK	Clock
V_{CC}, GND	Power Supply

electrical characteristics

PARAMETER		TEST CONDITIONS	min	typ	max	unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Output Voltage	I_{OL} = 8mA			0.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −2.0mA	3.5			V
I_{IL}	Low Level Input Current	V_{IL} = 0.4V			20	μA
I_{IH}	High Level Input Current	V_{IH} = 2.4V			20	μA
I_{CC}	Supply Current (Quiescent)				0.5	mA
I_{CC}	Supply Current (Dynamic)			15[1]	25[2]	mA

1) Typical I_{CC} conditions: 5MHz clock rate, V_{IH} = 2.4V, V_{IL} = 0.4V, V_{CC} = 5V, T_A = 25°C, random input patterns.
2) Maximum I_{CC} conditions: 5MHZ clock rate, V_{IH} = 2.0V; V_{IL} = 0.8V; V_{CC} = 5.5V; T_A = −55°C, all outputs toggling every cycle.

This architecture allows the L4C381 to accept arguments from a single 16-bit data bus. For those applications which do not require registered inputs, both the A and B operand registers can be made transparent with the FT_{AB} control line. When the FT_{AB} control is asserted, the A and B input registers are bypassed, however, they continue to function normally via the $\overline{EN}_A$ and $\overline{EN}_B$ controls. The contents of the input registers will again be available to the ALU if the FT_{AB} control is released.

output register

The output of the ALU drives the input of a 16-bit register. This rising-edge-triggered register is clocked by the same clock as the input registers. The output register is enabled by the $\overline{ENF}$ control signal. By disabling the output register, intermediate results can be held while loading new input operands. Three-state drivers controlled by the $\overline{OE}$ input allow the L4C381 to be configured in a single bidirectional bus system. The output register can be made tranisparent by asserting the FT_F control signal. When the FT_F control is asserted, the output register is bypassed, however, it continues to function normally via the $\overline{EN}_F$ control. The contents of the output register will again be available on the output pins if FT_F is released. With both FT_{AB} and FT_F true (high) the L4C381 is functionally identical to four cascaded 54S381-type devices.

operand selection

The two operand select lines OS_A and OS_B control multiplexers immediately preceding the ALU inputs. These multiplexers provide an operand force-to-zero function as well as result feedback to the B input. Figure 3 shows the inputs to the ALU as a function of the operand select inputs. Either the A or B operands may be forced to zero.

OS_B	OS_A	OPERAND B	OPERAND A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

Figure 3. Operand Selection Control

When both operand select lines are false (low), the L4C381 is configured as a chain calculation ALU. The registered ALU output is passed back to the B input to the ALU. This allows accumulation operations to be performed by providing new operands via the A input port. The accumulator can be preloaded from the A input by setting OS_A true. By forcing the function select lines to the CLEAR state (000), the accumulator may be cleared. Note that this feedback operation is not affected by the state of the FT_F control. That is, the F outputs of the L4C381 may be driven directly by the ALU (FT_F = true). The output register continues to function, however, and provides the ALU B operand source.

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switching characteristics

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COMBINATIONAL DELAYS (GUARANTEED MAXIMUM DELAYS)

FROM INPUT \ TO OUTPUT	COMMERCIAL F_{0-15}	COMMERCIAL $\overline{P},\overline{G}$	COMMERCIAL OVF,Z	COMMERCIAL C_{16}	MILITARY F_{0-15}	MILITARY $\overline{P},\overline{G}$	MILITARY OVF,Z	MILITARY C_{16}	units
$FT_{AB}=0$, $FT_F=0$									
Clock	32 (26)	38 (30)	53 (44)	36 (32)	37 (28)	44 (34)	63 (50)	45 (34)	ns
C_0	—	—	34 (28)	22 (20)	—	—	42 (32)	25 (23)	ns
I_{0-2}, OS_A, OS_B	—	42 (32)	42 (34)	42 (35)	—	48 (38)	48 (38)	48 (38)	ns
$FT_{AB}=0$, $FT_F=1$									
Clock	56 (46)	38 (30)	53 (44)	36 (32)	68 (56)	44 (34)	63 (50)	45 (34)	ns
C_0	37 (30)	—	34 (28)	22 (20)	42 (32)	—	42 (32)	25 (23)	ns
I_{0-2}, OS_A, OS_B	55 (40)	42 (32)	42 (34)	42 (35)	66 (46)	48 (38)	48 (38)	48 (38)	ns
$FT_{AB}=1$, $FT_F=0$									
A_{0-15}, B_{0-15}	—	36 (30)	46 (40)	37 (32)	—	44 (32)	56 (46)	44 (36)	ns
Clock	32 (26)				37 (28)				ns
C_0	—	—	34 (28)	22 (20)	—	—	42 (32)	25 (23)	ns
I_{0-2}, OS_A, OS_B	—	42 (32)	42 (34)	42 (35)	—	48 (38)	48 (38)	48 (38)	ns
$FT_{AB}=1$, $FT_F=1$									
A_{0-15}, B_{0-15}	55 (42)	36 (30)	46 (40)	37 (32)	65 (45)	44 (32)	56 (46)	44 (36)	ns
Clock									ns
C_0	37 (30)	—	34 (28)	22 (20)	42 (32)	—	42 (32)	25 (23)	ns
I_{0-2}, OS_A, OS_B	55 (40)	42 (32)	42 (34)	42 (35)	66 (46)	48 (38)	48 (38)	48 (38)	ns

SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE (GUARANTEED MINIMUM REQUIREMENTS)

INPUT	COMMERCIAL $FT_{AB}=0$ setup	COMMERCIAL $FT_{AB}=0$ hold	COMMERCIAL $FT_{AB}=1$ setup	COMMERCIAL $FT_{AB}=1$ hold	MILITARY $FT_{AB}=0$ setup	MILITARY $FT_{AB}=0$ hold	MILITARY $FT_{AB}=1$ setup	MILITARY $FT_{AB}=1$ hold	units
A_{0-15}, B_{0-15}	8 (6)	0	35 (28)	0	10 (8)	0	43 (33)	0	ns
C_0	21 (16)	0	21 (16)	0	25 (20)	0	25 (20)	0	ns
I_{0-2}, OS_A, OS_B	44 (32)	0	44 (32)	0	50 (36)	0	50 (36)	0	ns
$\overline{EN}_A$, $\overline{EN}_B$, $\overline{EN}_F$	8 (6)	0	8 (6)	0	10 (8)	0	10 (8)	0	ns

CLOCK CYCLE TIME AND PULSE WIDTH	COMMERCIAL	MILITARY	units
Minimum Cycle Time	43 (34)	52 (38)	ns
Highgoing Pulse	15 (10)	20 (15)	ns
Lowgoing Pulse	15 (10)	20 (15)	ns

THREE STATE ENABLE/DISABLE TIMES	COMMERCIAL	MILITARY	units
t_{EN}	20 (18)	22 (20)	ns
t_{DIS}	20 (18)	22 (20)	ns

Notes:

1) Commercial = 0 – 70°C, V_{CC} = 4.75V
   Military = – 55 – 125°C, V_{CC} = 4.5V
2) All outputs are loaded with 510 Ohms to + 5V, 750 Ohms + 60 pF to ground during functional and AC testing.
3) Data in parentheses represent performance of the L4C381-1, a speed selected version of the L4C381.

16-bit cascadable arithmetic/logic unit
package information

L4C381

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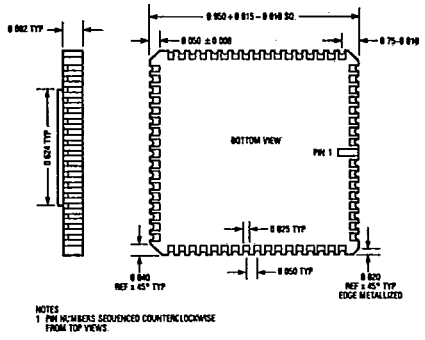
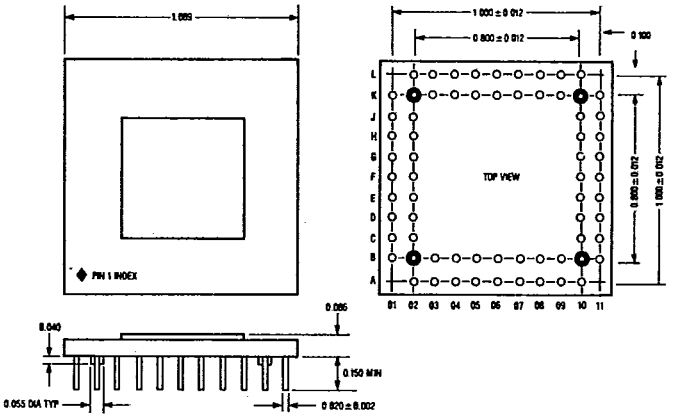
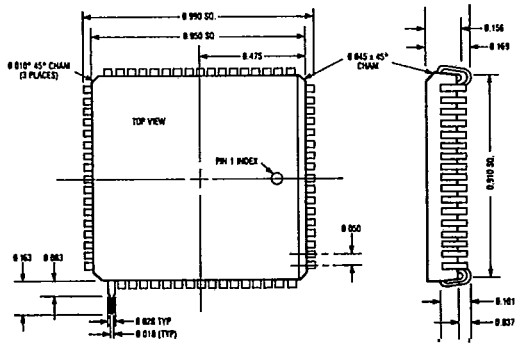
68 TERMINAL CERAMIC LEADLESS CHIP CARRIER (K3)[1,2]



68 TERMINAL PIN GRID ARRAY (G1)[2]



68 TERMINAL PLASTIC LEADED CHIP CARRIER (J2)[1]



Notes:
1) (K,J packages) Pin numbers sequenced counterclockwise from pin 1 in top view.
2) (K,G packages) Gold plating 60μ inches min. over 100μ inches ref. thickness of nickel.

L4C381 Device Pinouts

PIN J,K	PIN G	FUNCTION	PIN J,K	PIN G	FUNCTION
1	F02	A0	35	F10	F8
2	F01	A1	36	F11	F7
3	E02	A2	37	G10	F6
4	E01	A3	38	G11	F5
5	D02	A4	39	H10	F4
6	D01	A5	40	H11	F3
7	C02	A6	41	J10	F2
8	C01	A7	42	J11	F1
9	B01	A8	43	K11	F0
10	B02	A9	44	K10	C0
11	A02	A10	45	L10	I0
12	B03	A11	46	K09	I1
13	A03	A12	47	L09	I2
14	B04	A13	48	K08	OSA
15	A04	A14	49	L08	OSB
16	B05	A15	50	K07	FTAB
17	A05	CLK	51	L07	$\overline{ENB}$
18	B06	Vcc	52	K06	$\overline{ENA}$
19	A06	GND	53	L06	B0
20	B07	C16	54	K05	B1
21	A07	$\overline{P}$	55	L05	B2
22	B08	$\overline{G}$	56	K04	B3
23	A08	ZERO	57	L04	B4
24	B09	OVF	58	K03	B5
25	A09	$\overline{ENF}$	59	L03	B6
26	A10	FTF	60	L02	B7
27	B10	$\overline{OE}$	61	K02	B8
28	B11	F15	62	K01	B9
29	C10	F14	63	J02	B10
30	C11	F13	64	J01	B11
31	D10	F12	65	H02	B12
32	D11	F11	66	H01	B13
33	E10	F10	67	G02	B14
34	E11	F9	68	G01	B15

ordering information

ORDERING CODE	SPEED (NS)	PACKAGE TYPE	OPERATING RANGE
L4C381 JC-1 GC-1 KC-1 GCR-1	34	J2 G1 K3 G1	COMMERCIAL
L4C381 GM-1 KM-1 GMB-1 GME-1 KMB-1 KME-1	38	G1 K3 G1 G1 K3 K3	MILITARY
L4C381 JC GC KC GCR	43	J2 G1 K3 G1	COMMERCIAL
L4C381 GM KM GME KME	52	G1 K3 G1 K3	MILITARY

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16-bit cascadable arithmetic/logic unit

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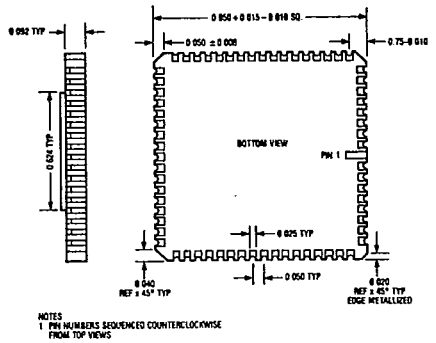
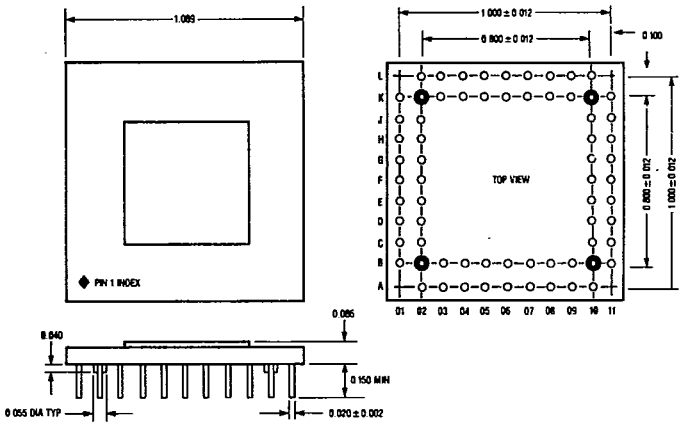
package information

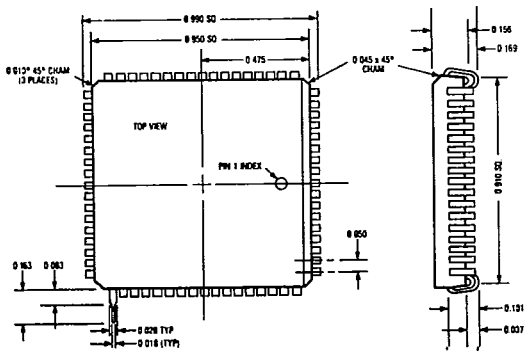
68 TERMINAL CERAMIC LEADLESS CHIP CARRIER (K3)[1,2]



68 TERMINAL PIN GRID ARRAY (G1)[2]



68 TERMINAL PLASTIC LEADED CHIP CARRIER (J2)[1]



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3	E02	A2	37	G10	F6
4	E01	A3	38	G11	F5
5	D02	A4	39	H10	F4
6	D01	A5	40	H11	F3
7	C02	A6	41	J10	F2
8	C01	A7	42	J11	F1
9	B01	A8	43	K11	F0
10	B02	A9	44	K10	C0
11	A02	A10	45	L10	I0
12	B03	A11	46	K09	I1
13	A03	A12	47	L09	I2
14	B04	A13	48	K08	OSA
15	A04	A14	49	L08	OSB
16	B05	A15	50	K07	FTAB
17	A05	CLK	51	L07	ENB
18	B06	Vcc	52	K06	ENA
19	A06	GND	53	L06	B0
20	B07	C16	54	K05	B1
21	A07	P	55	L05	B2
22	B08	G	56	K04	B3
23	A08	ZERO	57	L04	B4
24	B09	OVF	58	K03	B5
25	A09	ENF	59	L03	B6
26	A10	FTF	60	L02	B7
27	B10	OE	61	K02	B8
28	B11	F15	62	K01	B9
29	C10	F14	63	J02	B10
30	C11	F13	64	J01	B11
31	D10	F12	65	H02	B12
32	D11	F11	66	H01	B13
33	E10	F10	67	G02	B14
34	E11	F9	68	G01	B15

ordering information

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L4C381 GM-1 GMB-1 KMB-1	38	G1 G1 K3	MILITARY
L4C381 JC GC KC GCR	43	J2 G1 K3 G1	COMMERCIAL
L4C381 GM GMB KMB	52	G1 G1 K3	MILITARY

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