HN27C301P/FP Series

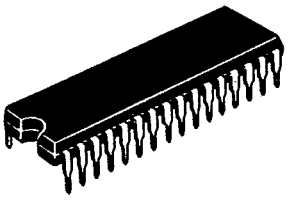
T-46-13-25

131072-word x 8-bit CMOS One Time Electrically Programmable ROM

The HN27C301P Series are 131072-word x 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C301P/FP Series are in the "1" state (output high).

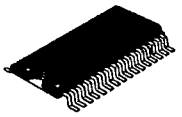
Data is introduced by selectively programming "0" into the desired bit location. This device is packaged in 32 pin plastic package, therefore, this device cannot be rewritten and erased.

HN27C301P Series



(DP-32)

HN27C301FP Series



(FP-32D)

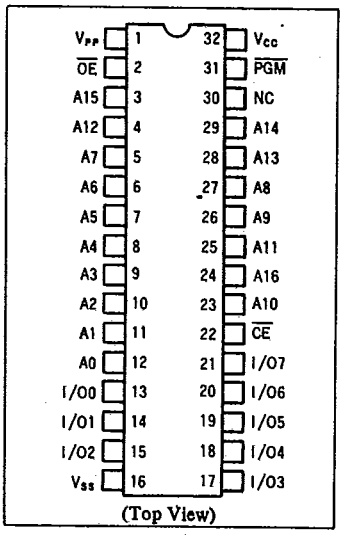
Features

- High speed
  - Access time . . . . . 200/250 ns (max.)
- Low power dissipation
  - Active mode 50 mW/MHz (typ.)
  - Standby mode 5 μW (typ.)
- Single power supply +5V ± 5%
- Fast High-Reliability program mode and Fast High-Reliability page program mode
  - Program voltage: +12.5V DC
  - Fast High-Reliability programming available
- Static . . . . . No clocks required
- Inputs and output TTL compatible during both read and program modes.

Ordering Information

Type No.	Access time	Package
HN27C301P-20	200ns	600 mil 32 pin Plastic DIP
HN27C301P-25	250ns	
HN27C301FP-20	200ns	32 pin Plastic SOP
HN27C301FP-25	250ns	

Pin Arrangement

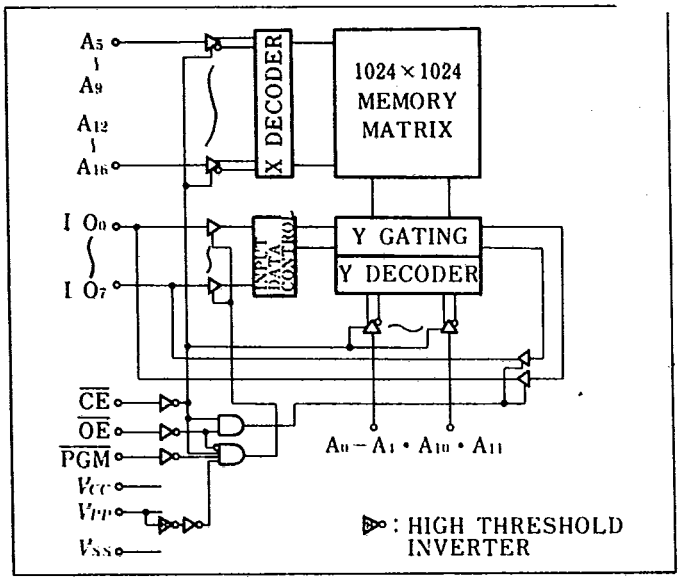


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Note) 1. X: Don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} voltage*1	V_{CC}	−0.6 to +7.0	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C
Storage temperature range under bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. −1.0 V for pulse width ≦ 50 ns

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Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 5.25V
Output Leakage Current	I_{LO}	–	–	2	μA	V_{out} = 5.25V/0.45V
V_{PP} Current	I_{PP1}	–	1	20	μA	V_{PP} = 5.5V
V_{CC} Current	I_{SB1}	–	–	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	–	1	20	μA	$\overline{CE}$ = V_{CC} ±0.3V
V_{CC} Current	I_{CC1}	–	–	30	mA	$\overline{CE}$ = $\overline{V}_{IL}$, I_{out} = 0mA
	I_{CC2}	–	–	30	mA	f = 5 MHz, I_{out} = 0mA
	I_{CC3}	–	–	15	mA	f = 1 MHz, I_{out} = 0mA
Input Low Voltage	V_{IL}	–0.3*1	–	0.8	V	
Input High Voltage	V_{IH}	2.2	–	V_{CC}+1*2	V	
Output Low Voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –400μA

Notes) *1. –1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

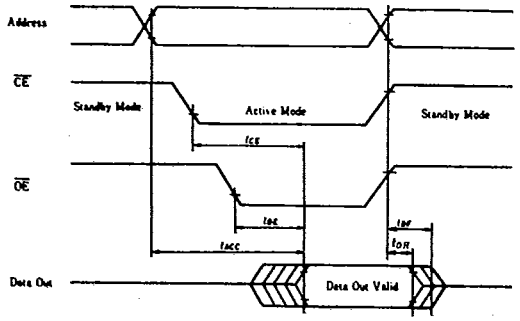
Item	Symbol	HN27C301P-20		HN27C301P-25		Unit	Test conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	200	–	250	ns	$\overline{CE}$=$\overline{OE}$= V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	200	–	250	ns	$\overline{OE}$= V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	70	10	100	ns	$\overline{CE}$= V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	60	ns	$\overline{CE}$= V_{IL}
Address to output hold	t_{OH}	0	–	0	–	ns	$\overline{CE}$=$\overline{OE}$= V_{IL}

Note) t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Switching Characteristics

Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

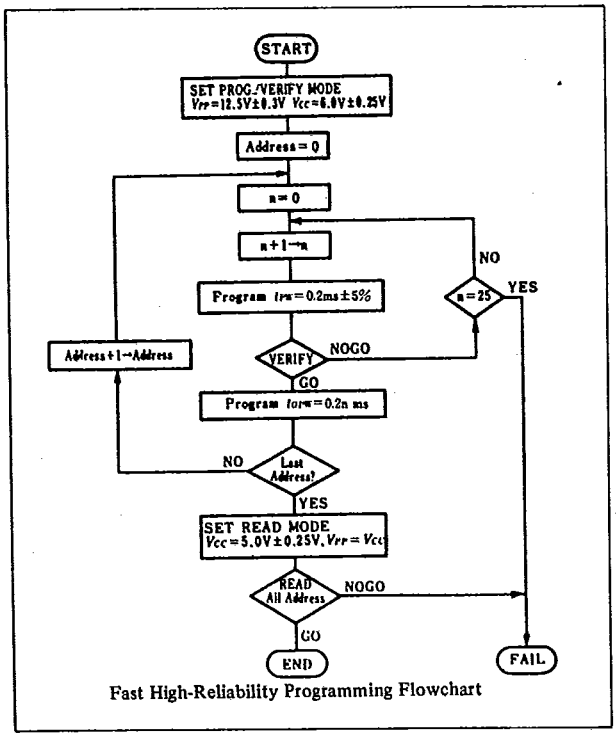


Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	–	–	10	pF	V_{in} = 0V
Output Capacitance	C_{out}	–	–	15	pF	V_{out} = 0V

Fast High-Reliability Programming

This device can be applied the Fast High-Reliability Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

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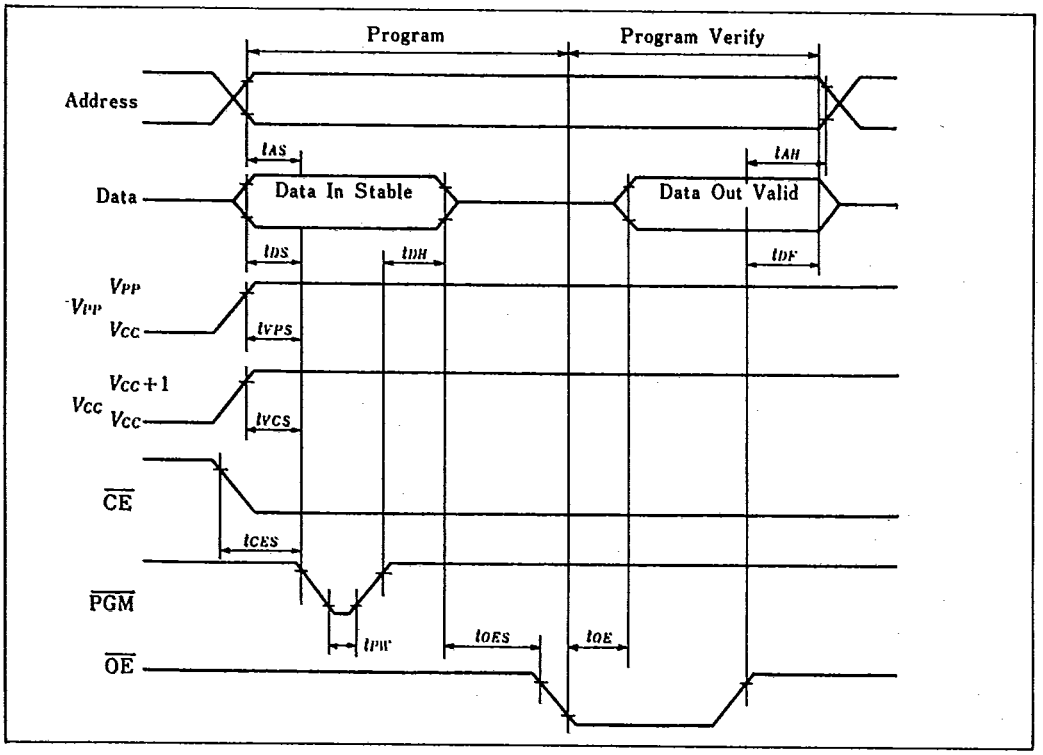
AC Programming Characteristics
($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	µs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	µs	
Data Setup Time	t_{DS}	2	–	–	µs	
Address Hold Time	t_{AH}	0	–	–	µs	
Data Hold Time	t_{DH}	2	–	–	µs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	µs	
V_{CC} Setup Time	t_{VCS}	2	–	–	µs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.2	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	µs	
Data Valid from OE	t_{OE}	0	–	150	ns	

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

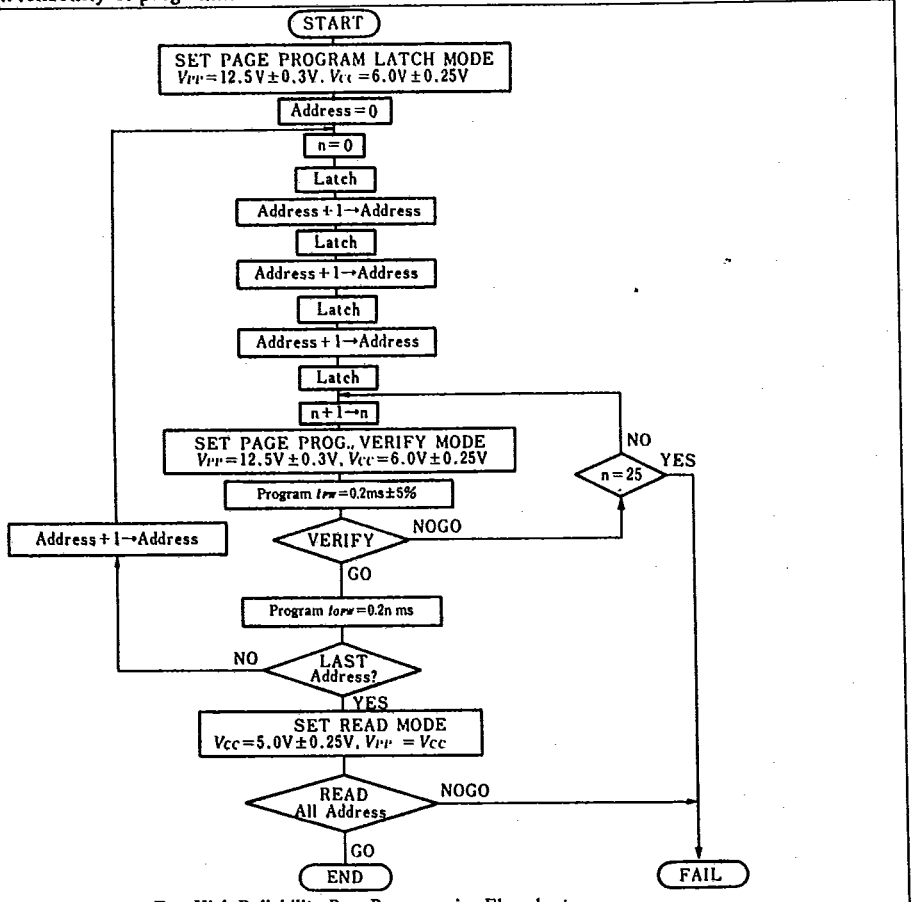
Switching Characteristics

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



Fast High-Reliability Page Programming

This device can be applied the Fast High-Reliability Page Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

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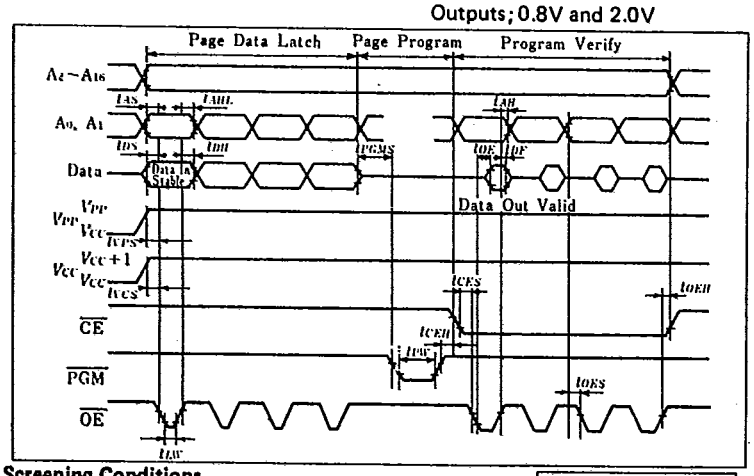
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	µs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	µs	
Data Setup Time	t_{DS}	2	–	–	µs	
Address Hold Time	t_{AH}	0	–	–	µs	
	t_{AHL}	2	–	–	µs	
Data Hold Time	t_{DH}	2	–	–	µs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	µs	
V_{CC} Setup Time	t_{VCS}	2	–	–	µs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	µs	
Data Valid from $\overline{OE}$	t_{OE}	0	–	150	ns	
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}	1	–	–	µs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	–	–	µs	
$\overline{CE}$ Hold Time	t_{CEH}	2	–	–	µs	
$\overline{OE}$ Hold Time	t_{OEH}	2	–	–	µs	

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

Switching Characteristics

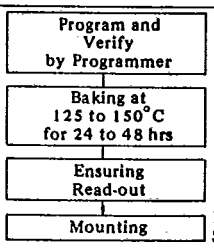
Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



Recommended Screening Conditions

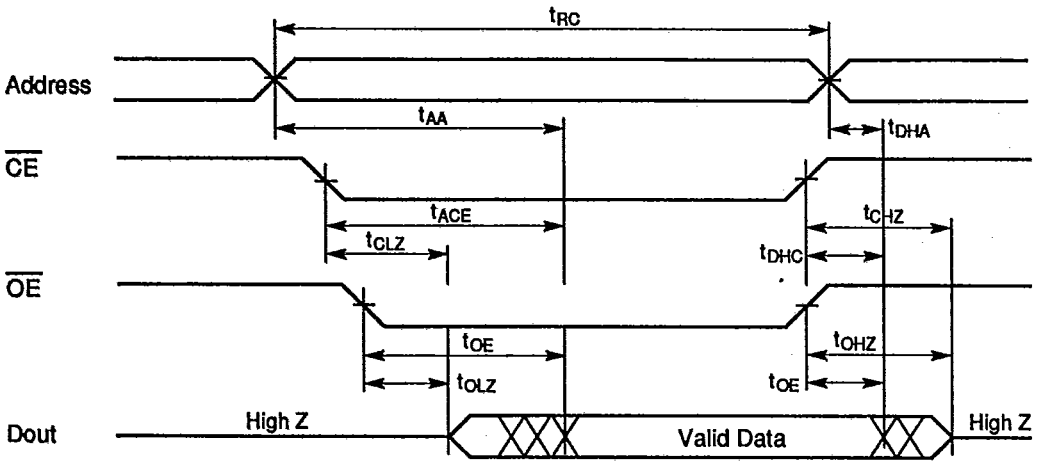
Before mounting, please make the screening (baking without bias) shown in the right.



Recommended Screening conditions

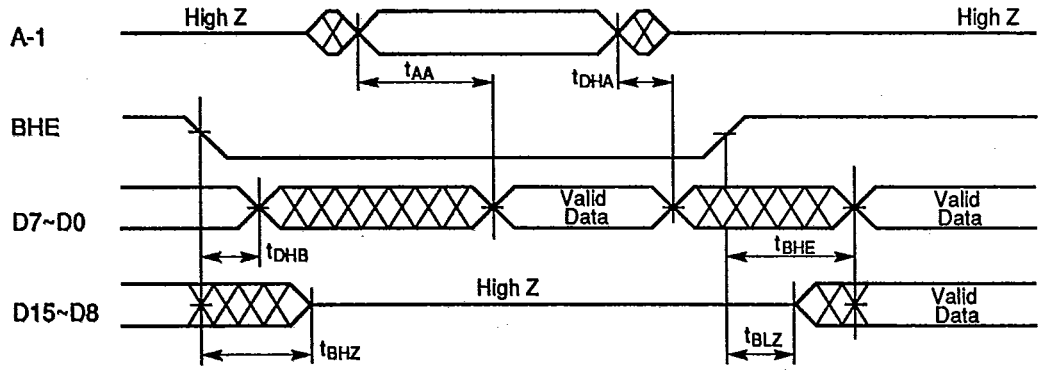
■ TIMING WAVEFORM

• Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}') (1)



NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

• Word Mode, Byte Mode Switch (2)



NOTES:
1. $\overline{CE}$ and $\overline{OE}$ are enable $A_{19} \sim A_0$ are valid.
2. D_{15}/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not apply to them.