

192 kHz Stereo DAC with 2 Vrms Line Out

Features

- ◆ Multi-bit Delta-Sigma Modulator
- ◆ 24-Bit Resolution
- ◆ Supports Sample Rates up to 192 kHz
- ◆ 106 dB A-wt Dynamic Range
- ◆ -93 dB THD+N
- ◆ Integrated Line Driver
- ◆ 2 Vrms Output into 5 kΩ AC Load
- ◆ Analog Low-Pass Filter
- ◆ Stereo Mutes with Auto-Mute Function
- ◆ Low Clock-Jitter Sensitivity
- ◆ Low-Latency Digital Filtering
- ◆ Popguard® Technology for Control of Clicks and Pops
- ◆ Single-Ended Outputs
- ◆ +3.3 V Core, +9 to 12 V Analog, and +1.5 to 3.3 V Interface Power Supplies
- ◆ Low Power Consumption
- ◆ 20-pin TSSOP, Lead-Free Assembly

Description

The CS4352 is a complete stereo digital-to-analog system including digital interpolation, fifth-order multi-bit delta-sigma digital-to-analog conversion, digital de-emphasis, analog filtering, and on-chip 2 Vrms line-level driver. The advantages of this architecture include ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, high tolerance to clock jitter, and a minimal set of external components.

The CS4352 is available in a 20-pin TSSOP package in both Commercial grade (-40°C to +85°C) and Automotive grade (-40°C to +105°C). The CDB4352 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please see ["Ordering Information" on page 20](#) for complete details.

These features are ideal for cost-sensitive, 2-channel audio systems including video game consoles, DVD players, A/V receivers, set-top boxes, digital TVs and DVD Recorders, mini-component systems, and mixing consoles.

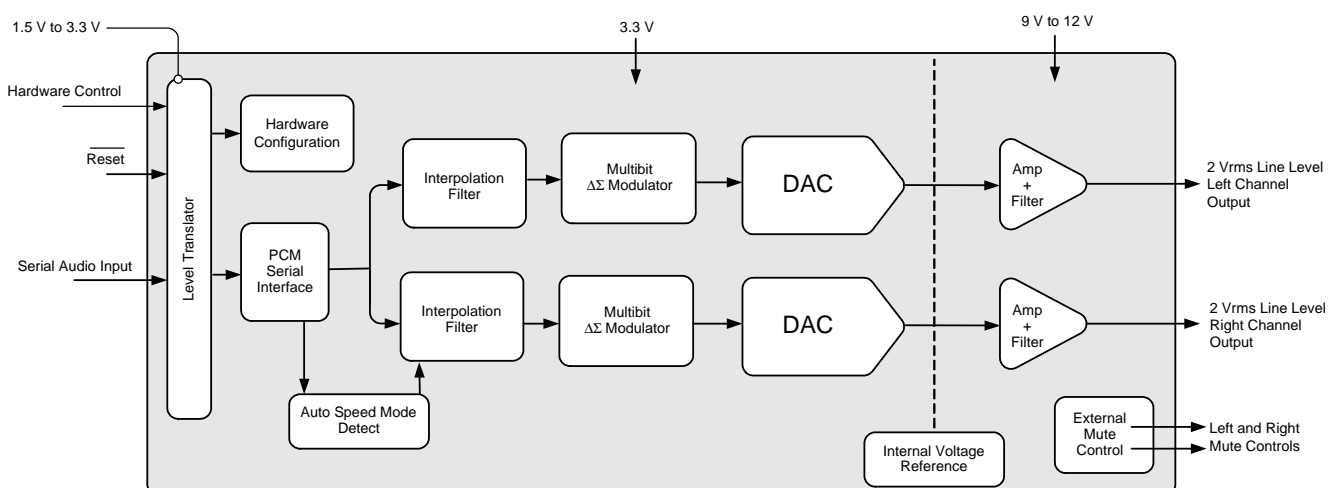


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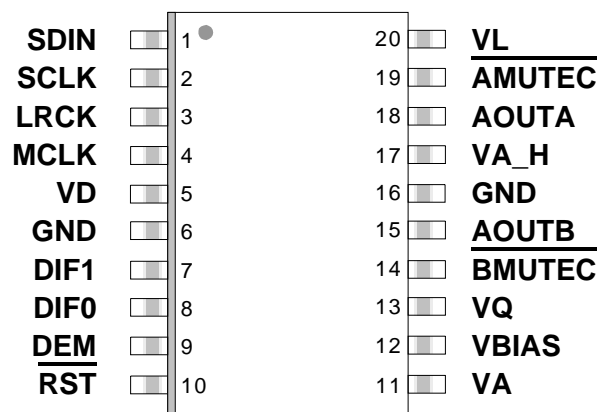
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1. PIN DESCRIPTIONS



| Pin Name | Pin # | Pin Description |
|----------------------------|---------|---|
| SDIN | 1 | Serial Audio Data Input (<i>Input</i>) - Input for two's complement serial audio data. |
| SCLK | 2 | Serial Clock (<i>Input</i>) - Serial clock for the serial audio interface. |
| LRCK | 3 | Left / Right Clock (<i>Input</i>) - Determines which channel, Left or Right, is currently active on the serial audio data line. |
| MCLK | 4 | Master Clock (<i>Input</i>) - Clock source for the delta-sigma modulator and digital filters. |
| VD | 5 | Digital Power (<i>Input</i>) - Positive power supply for the digital section. |
| GND | 6 16 | Ground (<i>Input</i>) - Ground reference. |
| DIF0 | 8 | Digital Interface Format (<i>Input</i>) - Defines the required relationship between the Left/Right Clock, Serial Clock, and Serial Audio Data. |
| DIF1 | 7 | |
| DEM | 9 | De-emphasis (<i>Input</i>) - Selects the standard 15 μ s/50 μ s digital de-emphasis filter response for 44.1 kHz sample rates |
| $\overline{\text{RST}}$ | 10 | Reset (<i>Input</i>) - Powers down the device and resets all internal registers to their default settings when enabled. |
| VA | 11 | Low Voltage Analog Power (<i>Input</i>) - Positive power supply for the analog section. |
| VBIAS | 12 | Positive Voltage Reference (<i>Output</i>) - Positive reference voltage for the internal DAC. |
| VQ | 13 | Quiescent Voltage (<i>Output</i>) - Filter connection for internal quiescent voltage. |
| VA_H | 17 | High Voltage Analog Power (<i>Input</i>) - Positive power supply for the analog section. |
| VL | 20 | Serial Audio Interface Power (<i>Input</i>) - Positive power for the serial audio interface |
| $\overline{\text{BMUTEC}}$ | 14 | Mute Control (<i>Output</i>) - Control signal for optional mute circuit. |
| $\overline{\text{AMUTEC}}$ | 19 | |
| AOUTB | 15 | Analog Outputs (<i>Output</i>) - The full-scale analog line output level is specified in the Analog Characteristics table. |
| AOUTA | 18 | |

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to ground.)

| Parameters | | Symbol | Min | Typ | Max | Units |
|---|---------------------------|------------|------|-----|------|-------|
| DC Power Supply | High Voltage Analog power | V_{A_H} | 8.40 | 9 | 12.6 | V |
| | Low Voltage Analog power | V_A | 3.13 | 3.3 | 3.47 | V |
| | Digital power | V_D | 3.13 | 3.3 | 3.47 | V |
| | Interface power | V_L | 1.43 | 1.5 | 3.47 | V |
| Ambient Operating Temperature (power applied) | -CZZ | T_A | -40 | - | +85 | °C |
| | -DZZ | | -40 | - | +105 | °C |

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

| Parameters | | Symbol | Min | Max | Units |
|---|---------------------------|------------|------|-------------|-------|
| DC Power Supply | High Voltage Analog power | V_{A_H} | -0.3 | 14.0 | V |
| | Low Voltage Analog power | V_A | -0.3 | 3.63 | V |
| | Digital power | V_D | -0.3 | 3.63 | V |
| | Interface power | V_L | -0.3 | 3.63 | V |
| Input Current, Any Pin Except Supplies | | I_{in} | - | ±10 | mA |
| Digital Input Voltage | Digital Interface | V_{IN-L} | -0.3 | $V_L + 0.4$ | V |
| Ambient Operating Temperature (power applied) | | T_A | -55 | +125 | °C |
| Storage Temperature | | T_{stg} | -65 | +150 | °C |

Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS - COMMERCIAL (-CZZ)

Test conditions (unless otherwise specified): $T_A = 25\text{ }^\circ\text{C}$, $V_{A_H} = 9\text{ V}$, $V_A = 3.3\text{ V}$, $V_D = 3.3\text{ V}$, $\text{GND} = 0\text{ V}$; $V_{\text{BIAS+}}$ and V_Q capacitors as shown in [Figure 2 on page 10](#); input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth 10 Hz to 20 kHz.

| Parameter | Symbol | Min | Typ | Max | Unit | |
|---|---------------------|--------|------|------|-----------------------|----|
| All Speed Modes | | | | | | |
| $F_s = 48, 96, \text{ and } 192\text{ kHz}$ | | | | | | |
| Dynamic Range (Note 1) | 24-bit A-Weighted | 100 | 106 | - | dB | |
| | unweighted | 97 | 103 | - | dB | |
| | 16-bit A-Weighted | - | 98 | - | dB | |
| | unweighted | - | 95 | - | dB | |
| Total Harmonic Distortion + Noise | (Note 1) | | - | - | - | |
| | 24-bit | 0 dB | - | -93 | -89 | dB |
| | | -20 dB | - | -83 | -77 | dB |
| | | -60 dB | - | -43 | -37 | dB |
| | 16-bit | 0 dB | - | -93 | - | dB |
| | | -20 dB | - | -75 | - | dB |
| -60 dB | | - | -35 | - | dB | |
| THD+N | | | | | | |
| Idle Channel Noise / Signal-to-noise ratio | (A-wt) | - | 106 | - | dB | |
| Interchannel Isolation | (1 kHz) | - | 99 | - | dB | |
| Analog Output - All Modes | | | | | | |
| Full Scale Output Voltage | | 1.84 | 2.00 | 2.11 | V _{rms} | |
| Common Mode Voltage | V_Q | - | 4 | - | V _{dc} | |
| Max Current draw from an AOUT pin | I_{OUTmax} | - | 575 | - | μA | |
| Max Current draw from VQ | I_{Qmax} | - | 1 | - | μA | |
| Interchannel Gain Mismatch | | - | 0.1 | - | dB | |
| Gain Drift | | - | 100 | - | ppm/ $^\circ\text{C}$ | |
| Output Impedance | Z_{OUT} | - | 50 | - | Ω | |
| AC-Load Resistance | R_L | 5 | - | - | k Ω | |
| Load Capacitance | C_L | - | - | 100 | pF | |

Notes:

- One-half LSB of triangular PDF dither is added to data.

DAC ANALOG CHARACTERISTICS - AUTOMOTIVE (-DZZ)

Test conditions (unless otherwise specified): $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{A_H} = 9\text{ V}$, $V_A = 3.3\text{ V}$, $V_D = 3.3\text{ V}$, $\text{GND} = 0\text{ V}$; $V_{\text{BIAS+}}$ and V_Q capacitors as shown in [Figure 2 on page 10](#); input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth 10 Hz to 20 kHz.

| Parameter | Symbol | Min | Typ | Max | Unit | |
|--|---------------------|--------|------|------|-------------------------|----|
| All Speed Modes $F_s = 48, 96, \text{ and } 192\text{ kHz}$ | | | | | | |
| Dynamic Range (Note 2) | 24-bit A-Weighted | 96 | 106 | - | dB | |
| | unweighted | 93 | 103 | - | dB | |
| | 16-bit A-Weighted | - | 98 | - | dB | |
| | unweighted | - | 95 | - | dB | |
| Total Harmonic Distortion + Noise (Note 2) | 24-bit | 0 dB | - | - | dB | |
| | | -20 dB | - | -93 | -89 | dB |
| | | -60 dB | - | -83 | -73 | dB |
| | 16-bit | 0 dB | - | -43 | -33 | dB |
| | | -20 dB | - | -93 | - | dB |
| | | -60 dB | - | -75 | - | dB |
| THD+N | - | -35 | - | dB | | |
| Idle Channel Noise / Signal-to-noise ratio (A-wt) | | - | 106 | - | dB | |
| Interchannel Isolation (1 kHz) | | - | 99 | - | dB | |
| Analog Output - All Modes | | | | | | |
| Full Scale Output Voltage | | 1.81 | 2.00 | 2.17 | V _{rms} | |
| Common Mode Voltage | V_Q | - | 4 | - | V _{dc} | |
| Max Current draw from an AOUT pin | I_{OUTmax} | - | 575 | - | μA | |
| Max Current draw from VQ | I_{Qmax} | - | 1 | - | μA | |
| Interchannel Gain Mismatch | | - | 0.1 | - | dB | |
| Gain Drift | | - | 100 | - | ppm/ $^{\circ}\text{C}$ | |
| Output Impedance | Z_{OUT} | - | 50 | - | Ω | |
| AC-Load Resistance | R_L | 5 | - | - | k Ω | |
| Load Capacitance | C_L | - | - | 100 | pF | |

Notes:

- One-half LSB of triangular PDF dither is added to data.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(The filter characteristics have been normalized to the sample rate (F_s) and can be referenced to the desired sample rate by multiplying the given characteristic by F_s . Amplitude vs. frequency plots of the data in the table below are available in “Digital Filter Response Plots” on page 16.)

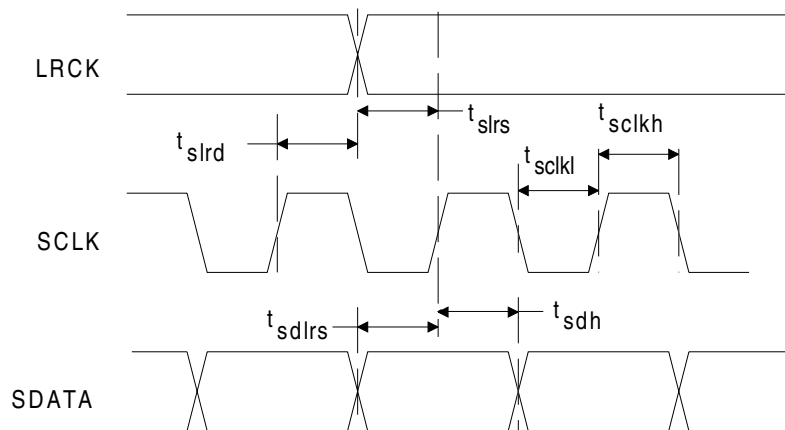
| Parameter | Min | Typ | Max | Unit | |
|---|--------------------|------------|----------------|------------|-------|
| Combined Digital and On-chip Analog Filter Response - Single-Speed Mode - 48 kHz | | | | | |
| Passband (Note 3) | to -0.01 dB corner | 0 | - | .454 | F_s |
| | to -3 dB corner | 0 | - | .499 | F_s |
| Frequency Response 10 Hz to 20 kHz | -0.01 | - | +0.01 | dB | |
| StopBand | 0.547 | - | - | F_s | |
| StopBand Attenuation (Note 4) | 102 | - | - | dB | |
| Total Group Delay (F_s = Output Sample Rate) | - | 9.4/ F_s | - | s | |
| Intra-channel Phase Deviation | - | - | $\pm 0.56/F_s$ | s | |
| Inter-channel Phase Deviation | - | - | 0 | s | |
| De-emphasis Error (Note 5)(Relative to 1 kHz) | $F_s = 44.1$ kHz | - | - | ± 0.14 | dB |
| Combined Digital and On-chip Analog Filter Response - Double-Speed Mode - 96 kHz | | | | | |
| Passband (Note 3) | to -0.01 dB corner | 0 | - | .430 | F_s |
| | to -3 dB corner | 0 | - | .499 | F_s |
| Frequency Response 10 Hz to 20 kHz | -0.01 | - | 0.01 | dB | |
| StopBand | .583 | - | - | F_s | |
| StopBand Attenuation (Note 4) | 80 | - | - | dB | |
| Total Group Delay (F_s = Output Sample Rate) | - | 4.6/ F_s | - | s | |
| Intra-channel Phase Deviation | - | - | $\pm 0.03/F_s$ | s | |
| Inter-channel Phase Deviation | - | - | 0 | s | |
| Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode - 192 kHz | | | | | |
| Passband (Note 3) | to -0.01 dB corner | 0 | - | .105 | F_s |
| | to -3 dB corner | 0 | - | .490 | F_s |
| Frequency Response 10 Hz to 20 kHz | -0.01 | - | 0.01 | dB | |
| StopBand | .635 | - | - | F_s | |
| StopBand Attenuation (Note 4) | 90 | - | - | dB | |
| Total Group Delay (F_s = Output Sample Rate) | - | 4.7/ F_s | - | s | |
| Intra-channel Phase Deviation | - | - | $\pm 0.01/F_s$ | s | |
| Inter-channel Phase Deviation | - | - | 0 | s | |

Notes:

3. Response is clock-dependent and will scale with F_s .
4. For Single-Speed Mode, the Measurement Bandwidth is from stopband to 3 F_s .
For Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 F_s .
For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 F_s .
5. De-emphasis is available only in Single-Speed Mode.

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

| Parameters | Symbol | Min | Max | Units | |
|--------------------------------------|-------------------|------------|----------------------|-------|-----|
| MCLK Frequency | | 1.024 | 48.0 | MHz | |
| MCLK Duty Cycle | | 45 | 55 | % | |
| Input Sample Rate (Auto selection) | Single-Speed Mode | F_s | 4 | 54 | kHz |
| | Double-Speed Mode | F_s | 84 | 108 | kHz |
| | Quad-Speed Mode | F_s | 170 | 216 | kHz |
| LRCK Duty Cycle | | 40 | 60 | % | |
| SCLK Pulse Width Low | t_{sckl} | 20 | - | ns | |
| SCLK Pulse Width High | t_{sckh} | 20 | - | ns | |
| SCLK Period | Single-Speed Mode | t_{sckw} | $\frac{1}{(128)F_s}$ | - | - |
| | Double-Speed Mode | t_{sckw} | $\frac{1}{(64)F_s}$ | - | - |
| | Quad-Speed Mode | t_{sckw} | $\frac{2}{MCLK}$ | - | - |
| SCLK rising to LRCK edge delay | t_{slrd} | 20 | - | ns | |
| SCLK rising to LRCK edge setup time | t_{slrs} | 20 | - | ns | |
| SDIN valid to SCLK rising setup time | t_{sdls} | 20 | - | ns | |
| SCLK rising to SDIN hold time | t_{sdh} | 20 | - | ns | |


Figure 1. Serial Input Timing

DIGITAL CHARACTERISTICS

| Parameters | Symbol | Min | Typ | Max | Units | |
|----------------------------------|----------------------|----------|------------|----------|---------------|---|
| High-Level Input Voltage | $V_L = 3.3\text{ V}$ | V_{IH} | 2.0 | - | - | V |
| | $V_L = 2.5\text{ V}$ | V_{IH} | 1.7 | - | - | V |
| | $V_L = 1.5\text{ V}$ | V_{IH} | 1.05 | - | - | V |
| Low-Level Input Voltage | $V_L = 3.3\text{ V}$ | V_{IL} | - | - | 0.8 | V |
| | $V_L = 2.5\text{ V}$ | V_{IL} | - | - | 0.7 | V |
| | $V_L = 1.5\text{ V}$ | V_{IL} | - | - | 0.38 | V |
| Input Leakage Current | I_{in} | - | - | ± 10 | μA | |
| Input Capacitance | | - | 8 | - | pF | |
| Maximum MUTE C Drive Current | | - | 2 | - | mA | |
| MUTE C High-Level Output Voltage | V_{OH} | - | V_{A_H} | - | V | |
| MUTE C Low-Level Output Voltage | V_{OL} | - | 0 | - | V | |

POWER AND THERMAL CHARACTERISTICS

| Parameters | Symbol | Min | Typ | Max | Units | |
|--|--|------------------|-----|------|-------|---------------|
| Power Supplies | | | | | | |
| Power Supply Current (Note 6) | normal operation, $V_{A_H} = 12\text{ V}$ | I_{A_H} | - | 12 | 21 | mA |
| | $V_{A_H} = 9\text{ V}$ | I_{A_H} | - | 10 | 16 | mA |
| | $V_A = 3.3\text{ V}$ | I_A | - | 3 | 4 | mA |
| | $V_D = 3.3\text{ V}$ | I_D | - | 12 | 16 | mA |
| | Interface current $V_L = 3.3\text{ V}$ | I_L | - | 0.02 | 0.09 | mA |
| | power-down state, all supplies (Note 7) | I_{pd} | - | 380 | - | μA |
| Power Dissipation (all supplies) $V_{A_H} = 12\text{ V}$ | (Note 6) | | | | | |
| | normal operation | | - | 121 | 158 | mW |
| | power-down (Note 7) | | - | 1 | - | mW |
| | $V_{A_H} = 9\text{ V}$ | normal operation | | - | 91 | 122 |
| power-down (Note 7) | | | - | 1 | - | mW |
| Power Supply Rejection Ratio (Note 8) | (1 kHz) | PSRR | - | 60 | - | dB |
| | (60 Hz) | | - | 60 | - | dB |

Notes:

- Current consumption increases with increasing FS and increasing MCLK. Typ and Max values are based on highest FS and highest MCLK. Variance between speed modes is small.
- Power down mode is defined as $\overline{\text{RST}}$ pin = Low with all clock and data lines held static low. All digital inputs have a weak pull-down which is only present during reset. Opposing this pull-down will slightly increase the power-down current (pull-down is equivalent to a 50 k Ω resistor per pin).
- Valid with the recommended capacitor values on VQ and V_{BIAS} as shown in the typical connection diagram in Section 3.

3. TYPICAL CONNECTION DIAGRAM

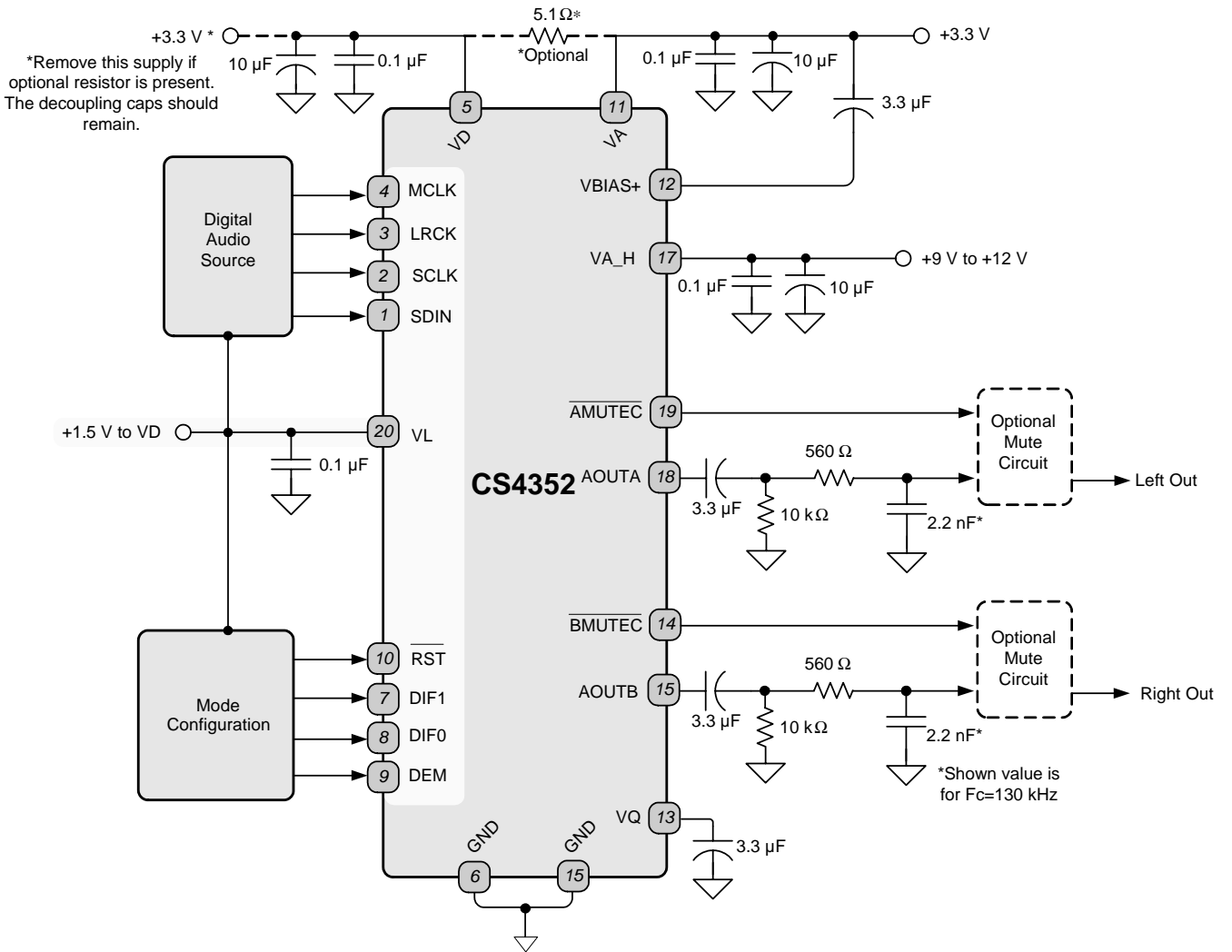


Figure 2. Typical Connection Diagram

4. APPLICATIONS

4.1 Sample Rate Range/Operational Mode Detect

The device operates in one of three operational modes. The allowed sample rate range in each mode is auto-detected.

The CS4352 will auto-detect the correct mode when the input sample rate (F_s), defined by the LRCK frequency, falls within one of the ranges illustrated in [Table 1](#). Sample rates outside the specified range for each mode are not supported.

| Input Sample Rate (F_s) | Mode |
|-----------------------------|-------------------|
| 4 kHz - 54 kHz | Single-Speed Mode |
| 84 kHz - 108 kHz | Double-Speed Mode |
| 170 kHz - 216 kHz | Quad-Speed Mode |

Table 1. CS4352 Auto-Detect

4.2 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The left/right clock, defined also as the input sample rate (F_s), must be synchronously derived from the MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in [Tables 2-4](#).

Refer to [Section 4.3](#) for the required SCLK timing associated with the selected Digital Interface Format and to ["Switching Specifications - Serial Audio Interface"](#) on [page 8](#) for the maximum allowed clock frequencies.

| Sample Rate (kHz) | MCLK (MHz) | | | | |
|-------------------|------------|---------|---------|---------|---------|
| | 256x | 384x | 512x | 768x | 1024x |
| 32 | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 |
| 44.1 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | 45.1584 |
| 48 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 |

Table 2. Single-Speed Mode Standard Frequencies

| Sample Rate (kHz) | MCLK (MHz) | | | | |
|-------------------|------------|---------|---------|---------|---------|
| | 128x | 192x | 256x | 384x | 512x |
| 88.2 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | 45.1584 |
| 96 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 |

Table 3. Double-Speed Mode Standard Frequencies

| Sample Rate (kHz) | MCLK (MHz) | | |
|-------------------|------------|---------|---------|
| | 128x | 192x | 256x |
| 176.4 | 22.5792 | 33.8688 | 45.1584 |
| 192 | 24.5760 | 36.8640 | 49.1520 |

Table 4. Quad-Speed Mode Standard Frequencies

4.3 Digital Interface Format

The device will accept audio samples in 1 of 4 digital interface formats, as illustrated in [Table 5](#).

The desired format is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between the LRCK, SCLK and SDIN, see [Figures 3-5](#). For all formats, SDIN is valid on the rising edge of SCLK. Also, SCLK must have at least 32 cycles per LRCK period in format 2 and 48 cycles per LRCK period in format 3.

For more information about serial audio formats, refer to Cirrus Logic Application Note AN282: *The 2-Channel Serial Audio Interface: A Tutorial*, available at www.cirrus.com.

| DIF1 | DIF0 | DESCRIPTION | FORMAT | FIGURE |
|------|------|-------------------------------------|--------|--------|
| 0 | 0 | I ² S, up to 24-bit Data | 0 | 3 |
| 0 | 1 | Right-Justified, 24-bit Data | 1 | 4 |
| 1 | 0 | Left-Justified, up to 24-bit Data | 2 | 5 |
| 1 | 1 | Right-Justified, 16-bit Data | 3 | 4 |

Table 5. Digital Interface Format

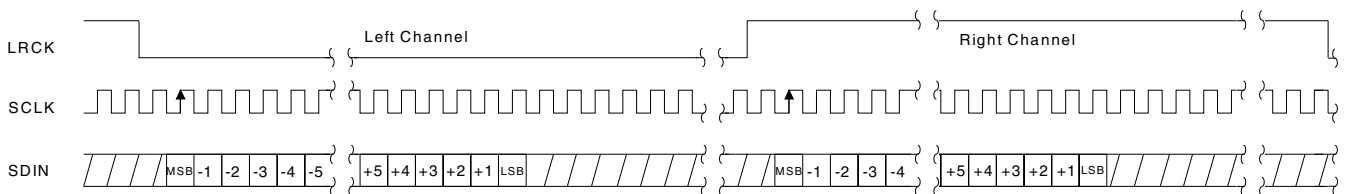


Figure 3. I²S, up to 24-Bit Data

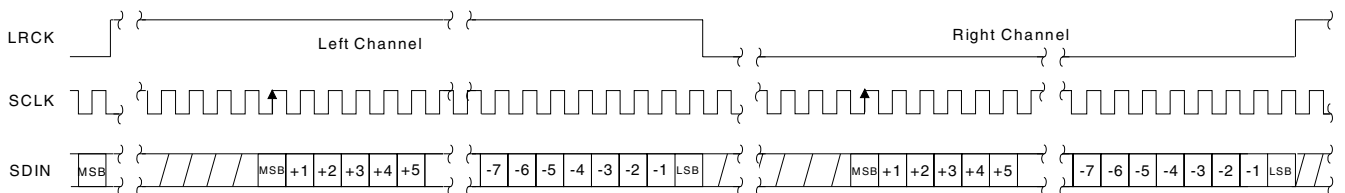


Figure 4. Right-Justified Data

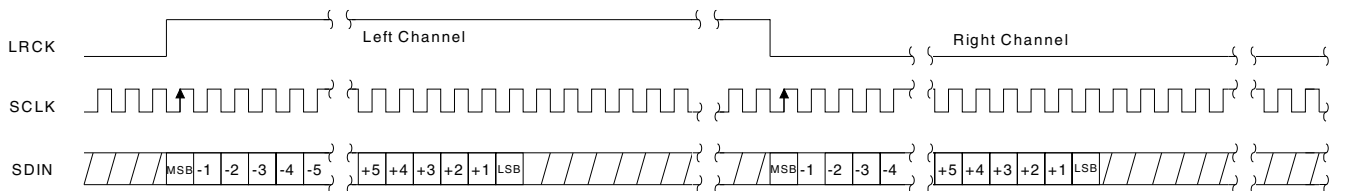


Figure 5. Left-Justified up to 24-Bit Data

4.4 De-Emphasis Control

The device includes on-chip digital de-emphasis. Figure 6 shows the de-emphasis curve for F_s equal to 44.1 kHz. The frequency response of the de-emphasis curve scales with changes in sample rate, F_s . The De-emphasis error will increase for sample rates other than 44.1 kHz.

When pulled to VL, the DEM pin activates the 44.1 kHz de-emphasis filter. When pulled to GND, the DEM pin turns off the de-emphasis filter.

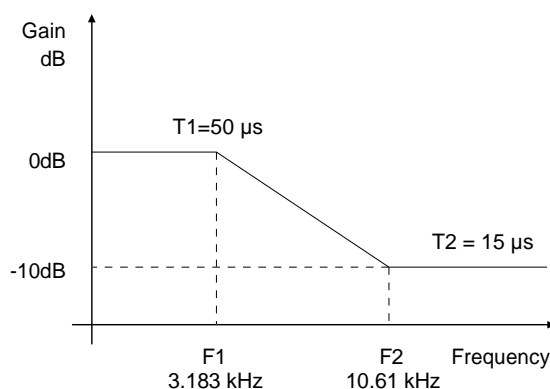


Figure 6. De-Emphasis Curve

Note: De-emphasis is only available in Single-Speed Mode.

4.5 Recommended Power-Up Sequence

1. Hold \overline{RST} low until the power supplies and configuration pins are stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in Section 4.2. In this state, VQ will remain low and VBIAS will be connected to VA.
2. Bring \overline{RST} high. The device will remain in a low power state with VQ low and will initiate the power-up sequence after approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode).

4.6 Grounding and Power Supply Arrangements

As with any high-resolution converter, the CS4352 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 2 shows the recommended power arrangements, with VA_H, VA, VD, and VL connected to clean supplies. If the ground planes are split between digital ground and analog ground, the GND pins of the CS4352 should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the VBIAS and VQ pins in order to avoid unwanted coupling into the DAC.

4.6.1 Capacitor Placement

Decoupling capacitors should be placed as close to the DAC as possible, with the low-value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin.

Note: All decoupling capacitors should be referenced to analog ground.

The CDB4352 evaluation board demonstrates the optimum layout and power supply arrangements.

4.7 Popguard Transient Control

The CS4352 uses a novel technique to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended, single-supply converters. It is activated inside the DAC when the $\overline{\text{RST}}$ pin is toggled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

4.7.1 Power-Up

When the device is initially powered-up, the audio outputs, AOUTA and AOUTB, are clamped to GND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing audible power-up transients.

4.7.2 Power-Down

To prevent audible transients at power-down, the device must first enter its power-down state. When this occurs, audio output ceases, and the internal output buffers are disconnected from AOUTA and AOUTB. In their place, a soft-start current sink is substituted that allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off, and the system is ready for the next power-on.

4.7.3 Discharge Time

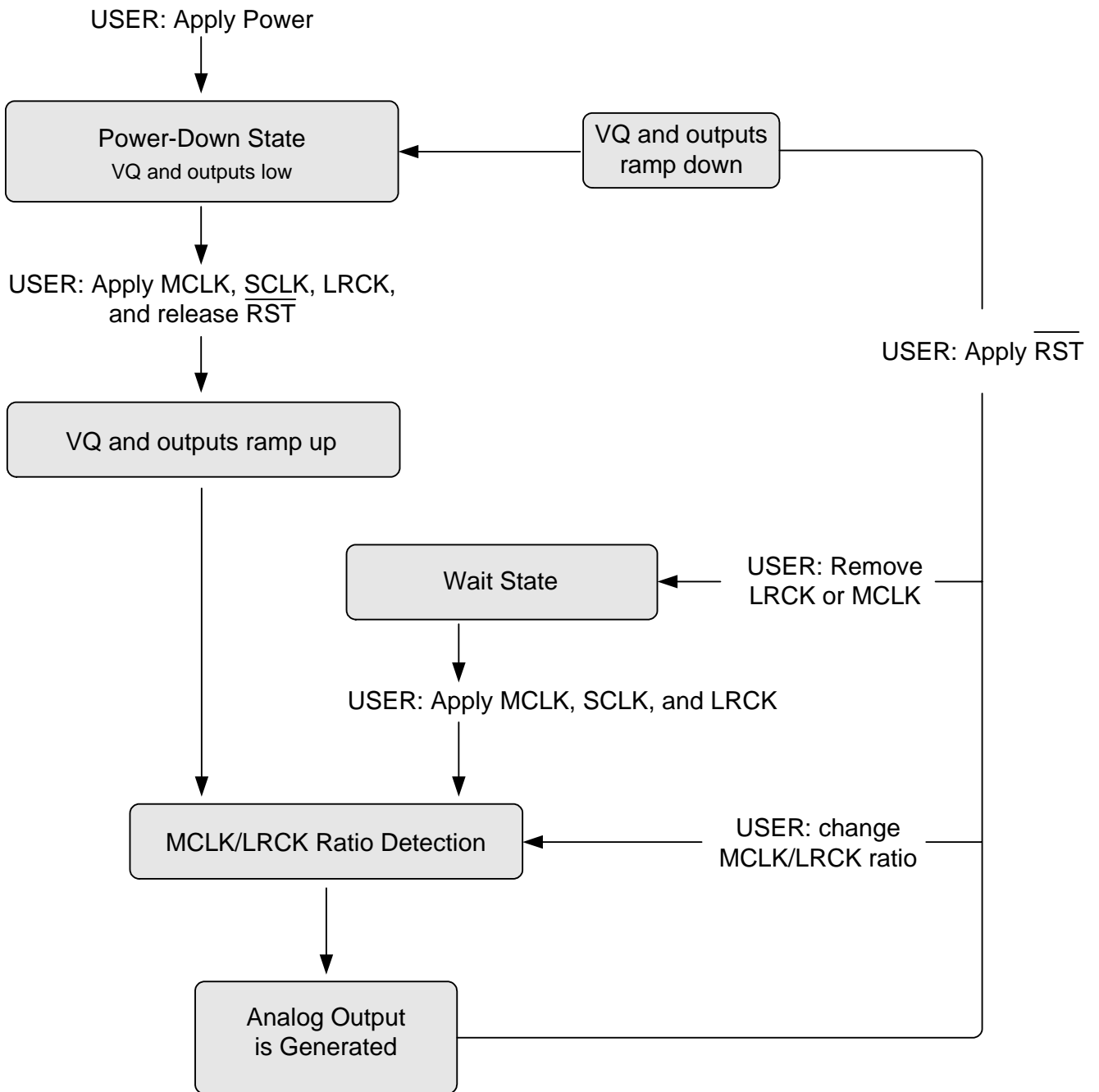
To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning on the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 3.3 μF capacitor, the minimum power-down time will be approximately 0.4 seconds.

4.8 Mute Control

The Mute Control pins go active during power-up initialization, reset, muting, or if the MCLK to LRCK ratio is incorrect. These pins are intended to be used as control for external mute circuits to prevent the clicks and pops that can occur in any single-ended, single-supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. Please see the CDB4352 data sheet for a suggested mute circuit for dual-supply systems. Alternately, the FET muting circuit from the CS4351 data sheet may be used as well. This FET circuit must be placed in series after the RC filter; otherwise noise may occur during muting conditions. Further ESD protection will need to be taken into consideration for the FET used.

4.9 Initialization and Power-Down Sequence Diagram



5. DIGITAL FILTER RESPONSE PLOTS

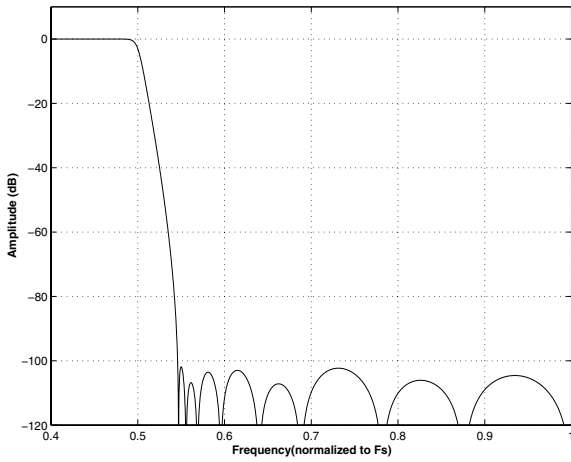


Figure 7. Single-Speed Stopband Rejection

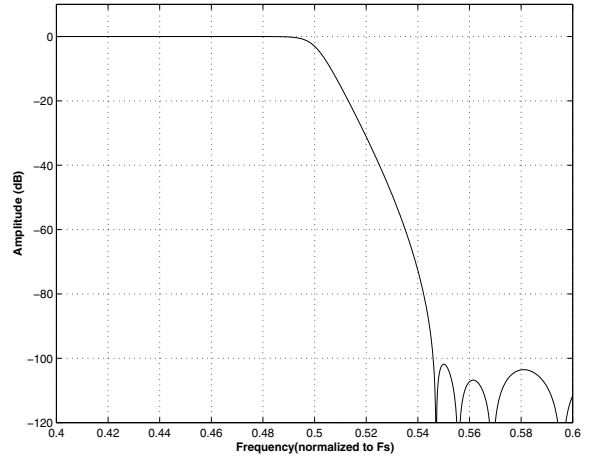


Figure 8. Single-Speed Transition Band

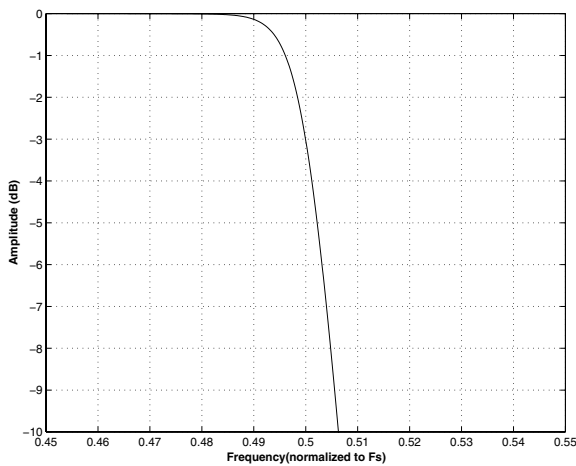


Figure 9. Single-Speed Transition Band (detail)

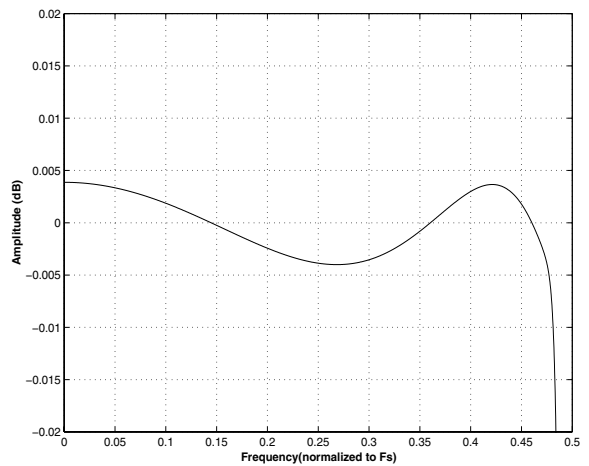


Figure 10. Single-Speed Passband Ripple

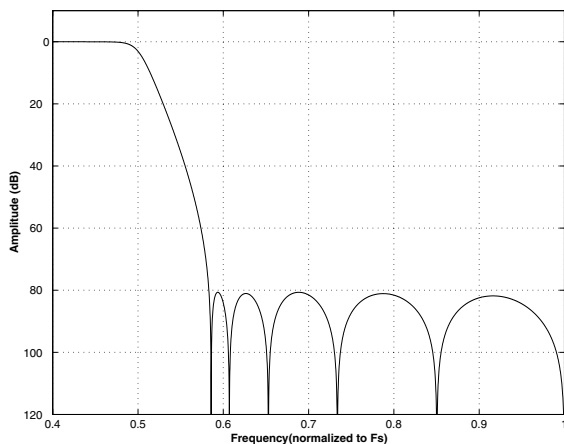


Figure 11. Double-Speed Stopband Rejection

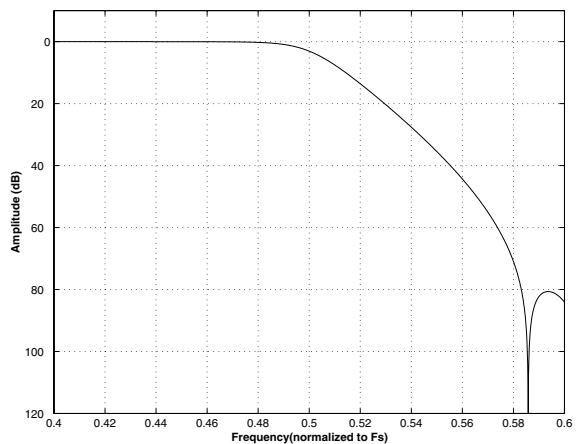
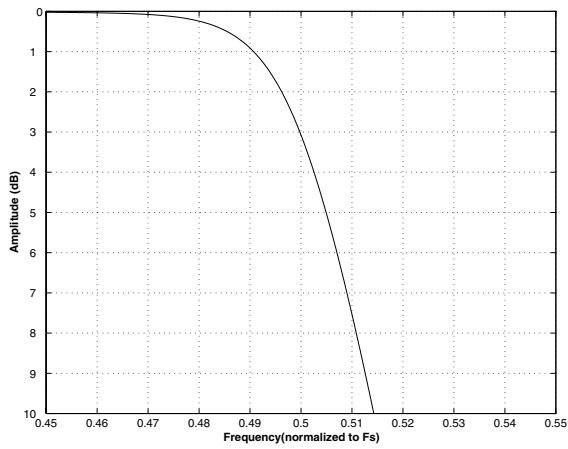
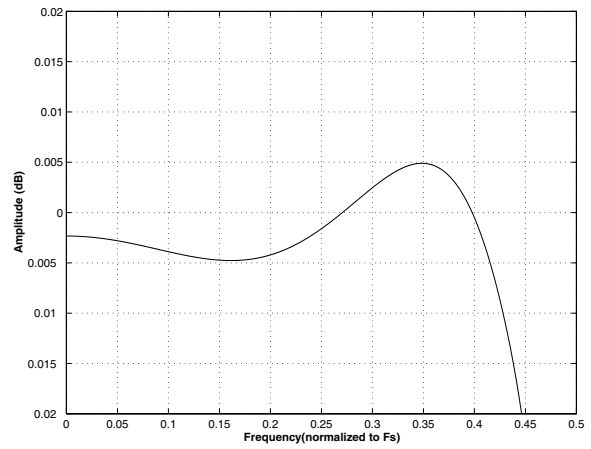
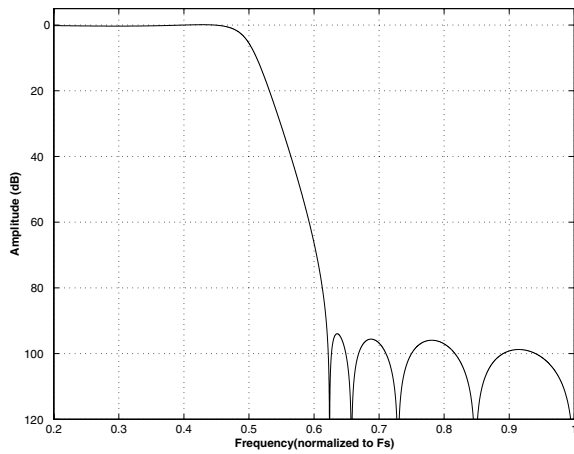
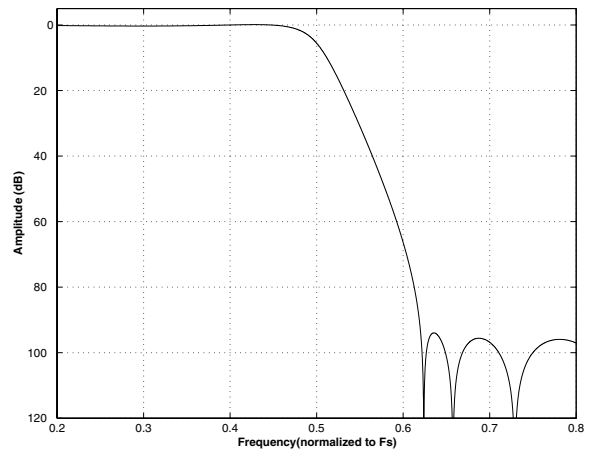
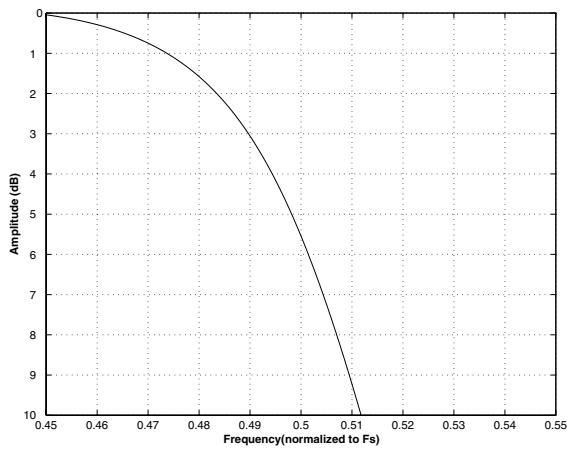
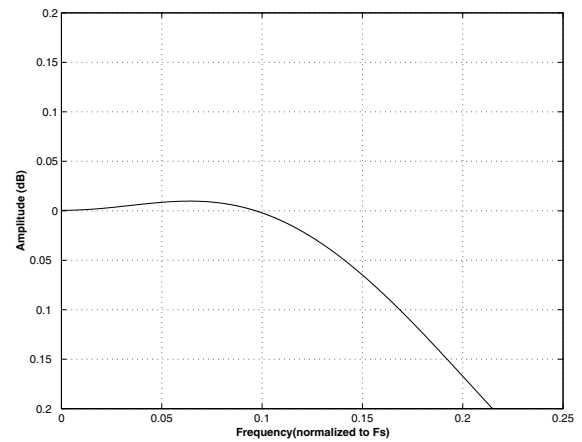


Figure 12. Double-Speed Transition Band


Figure 13. Double-Speed Transition Band (detail)

Figure 14. Double-Speed Passband Ripple

Figure 15. Quad-Speed Stopband Rejection

Figure 16. Quad-Speed Transition Band

Figure 17. Quad-Speed Transition Band (detail)

Figure 18. Quad-Speed Passband Ripple

6. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full-scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

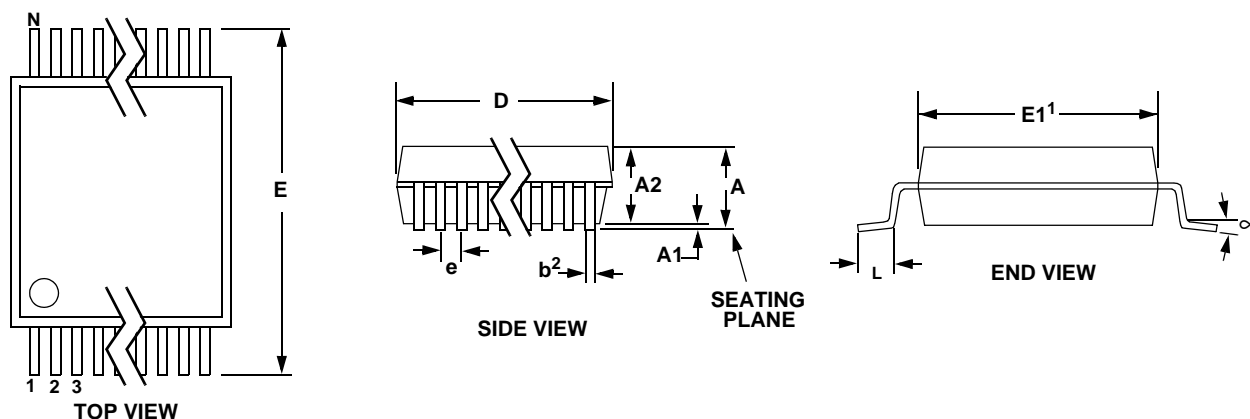
The change in gain value with temperature. Units in ppm/°C.

Intra-channel Phase Deviation

The deviation from linear phase within a given channel.

Inter-channel Phase Deviation

The difference in phase between channels.

7. PACKAGE DIMENSIONS
20L TSSOP (4.4 mm BODY) PACKAGE DRAWING


| DIM | INCHES | | | MILLIMETERS | | | NOTE |
|-----|---------|--------|-------|-------------|-------|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| A | -- | -- | 0.043 | -- | -- | 1.10 | |
| A1 | 0.002 | 0.004 | 0.006 | 0.05 | -- | 0.15 | |
| A2 | 0.03346 | 0.0354 | 0.037 | 0.85 | 0.90 | 0.95 | |
| b | 0.00748 | 0.0096 | 0.012 | 0.19 | 0.245 | 0.30 | 2,3 |
| D | 0.252 | 0.256 | 0.259 | 6.40 | 6.50 | 6.60 | 1 |
| E | 0.248 | 0.2519 | 0.256 | 6.30 | 6.40 | 6.50 | |
| E1 | 0.169 | 0.1732 | 0.177 | 4.30 | 4.40 | 4.50 | 1 |
| e | -- | -- | 0.026 | -- | -- | 0.65 | |
| L | 0.020 | 0.024 | 0.028 | 0.50 | 0.60 | 0.70 | |
| μ | 0° | 4° | 8° | 0° | 4° | 8° | |

JEDEC #: MO-153

Controlling Dimension is Millimeters.

1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

| Parameters | | Symbol | Min | Typ | Max | Units |
|----------------------------|-----------|---------------|-----|-----|-----|---------|
| Package Thermal Resistance | 20L TSSOP | θ_{JA} | - | 72 | - | °C/Watt |

8. ORDERING INFORMATION

| Product | Description | Package | Pb-Free | Grade | Temp Range | Container | Order # |
|---------|---|--------------|---------|------------|-----------------|------------------|---------------------------|
| CS4352 | 20-pin, 192 kHz Stereo DAC with 2 Vrms Line Out | 20-pin TSSOP | YES | Commercial | -40° to +85° C | Rail Tape & Reel | CS4352-CZZ CS4352-CZZR |
| | | | | Automotive | -40° to +105° C | Rail Tape & Reel | CS4352-DZZ CS4352-DZZR |
| CDB4352 | CS4352 Evaluation Board | | - | - | - | - | CDB4352 |

9. REVISION HISTORY

| Release | Changes |
|---------|--|
| PP1 | Lowered V_{A_H} minimum specification. Updated Idle channel noise specification to A-wt. Updated AOUT current draw specification. Updated V_{IL} for $V_L=1.5V$. |
| F1 | Updated performance specifications and limits based on statistical data. |
| F2 | Added Automotive grade specifications and ordering information. Updated Commercial grade idle channel noise specification. Lowered V_{IL} maximum specification. Updated power supply current specification. Updated MCLK maximum specification. |

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to www.cirrus.com.

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