Embedded

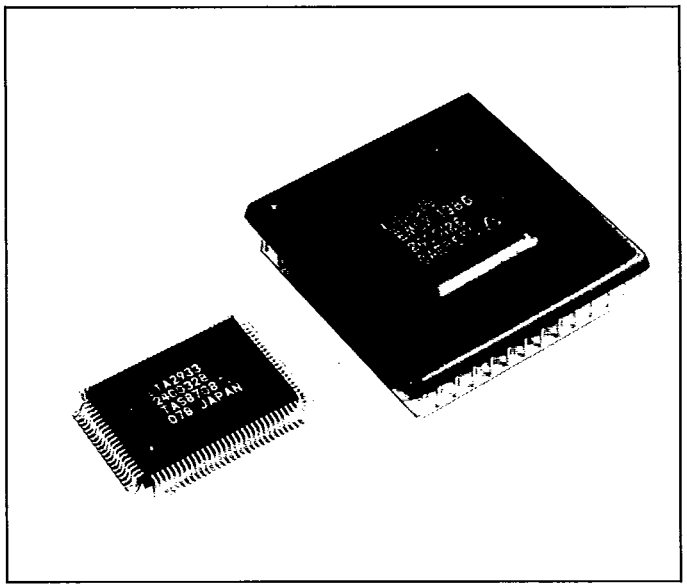
Storage

Technology

MERGED ARCHITECTURE CONTROLLER

2400126
2400328

EMULEX



MAC Chip

FEATURES

- Combines disk formatter and buffer controller functions in one VLSI chip
- Forty-three control, status, and parameter registers
- Interfaces easily to several popular microprocessors including the 68000, 80188, 80186 and 8031. The MAC interfaces directly to the 8031 with no additional circuitry.

Buffer Controller

- Directly controls up to 64K bytes of dynamic RAM (DRAM)
- Provides dynamic buffer memory timing and automatic refresh
- Checks and generates parity for buffer memory
- Connects the microprocessor bus directly to the buffer data bus, allowing microprocessor access to the buffer memory and external channels
- Decodes the microprocessor address for buffer memory and the I/O devices
- Using a priority scheme, allocates buffer memory between the four programmable DMA channels, the microprocessor port, and the refresh logic channel
- Supports automatic address reload for three of the four DMA channels

Disk Formatter

- Supports ST-506/412, ESDI, SMD, and SMD/E drive formats
- Supports disk data rates to 24 Megabits/second
- Supports hard and soft sector modes
- Five-byte data FIFO
- Internal ID field comparator
- Forty-eight-bit ECC for data fields
- CRC generator/checker for ID fields
- Disk read, write, and format functions implemented using a comprehensive command set
- Interfaces directly to disk drive electronics for embedded applications
- Halts disk write operations on power fail detect
- Supports variable length sectoring from 1 to 4096 bytes

DESCRIPTION

The MAC chip is an integral part of a sophisticated high performance controller architecture developed at Emulex.

The Merged Architecture Controller (MAC) chip combines buffer management and disk formatter functions in a single chip. These two functions comprise the heart of modern, microprocessor-based disk controllers. The availability of these functions in a single package allows designers to create controllers that take only a few square inches of printed circuit board space.

The MAC chip is implemented using CMOS technology. Figure 1 shows the major functional modules in the MAC.

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The disk formatter module, referred to as the DF2, is that part of the MAC chip which controls hard-disk format functions. It is compatible with the interface and format requirements of most 14, 8, 5¼ and 3½-inch disks operating in hard or soft sectored modes. It supports SMD, SMD-E, ESDI, and ST-506/412 type disks. The DF2 handles serial disk transfer at rates of up to 24M bits per second.

The buffer controller module, or BC2, which provides DMA control of local dynamic RAM has four programmable DMA channels (one of which is dedicated to the DF2). It also supports automatic refresh of buffer RAM. The BC2 provides a link between the microprocessor bus and the buffer data bus. This allows the microprocessor to access the buffer RAM, DF2 registers, host interface logic, and other VLSI devices on the buffer data bus.

A third module, the GLU module, provides various configuration and reset functions, including a watchdog timer.

The BC2 module is functionally compatible with the stand-alone version of the Emulex Buffer Controller 2. The DF2 design in the MAC is compatible with the stand-alone version of the Disk Formatter, but includes a number of additional features.

With some external logic the MAC chip can be controlled by a variety of microprocessors, including the 80188, 80186, and 68000. It interfaces directly to the Intel 8031 microprocessor with no additional circuitry.

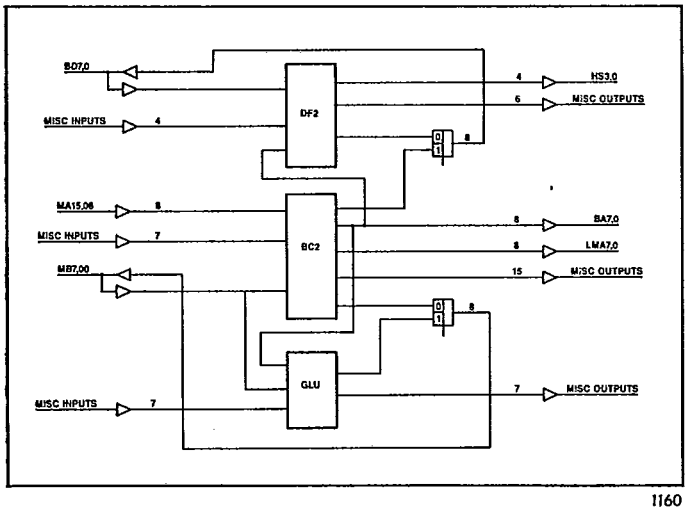

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Figure 1. MAC Chip Major Functional Blocks

SYSTEM ORGANIZATION

A typical disk controller block diagram is shown in Figure 2. An entire embedded SCSI-compatible disk controller design requires only the following parts:

Part	Qty
8031 Microprocessor	1
32K or 64K byte EPROM	1
64K X 4 DRAM	2
64K X 1 DRAM (parity) optional	1
SCSI Protocol Controller (ESP)	1
MAC Chip	1
Total	7

The Emulex controller architecture, of which the MAC chip is a part, uses two internal buses. By separating the microprocessor and buffer data buses, Emulex controllers are able to achieve superior performance using inexpensive components such as the 8031 microprocessor.

The BC2 module of the MAC makes this bus separation possible. It allows high speed DMA between the controller's buffer RAM and either the disk formatter or host interface without direct microprocessor intervention. This frees the microprocessor to decode a command from the host or to set up the disk drive for operation while data is being transferred into or out of the buffer RAM.

The microprocessor works with the DF2 portion of the MAC to handle all of the disk functions. The microprocessor controls head position, manages error correction, and monitors drive status. The DF2 is responsible for head selection, generation and comparison of ECCs, and transfer of serial NRZI data to and from the disk.

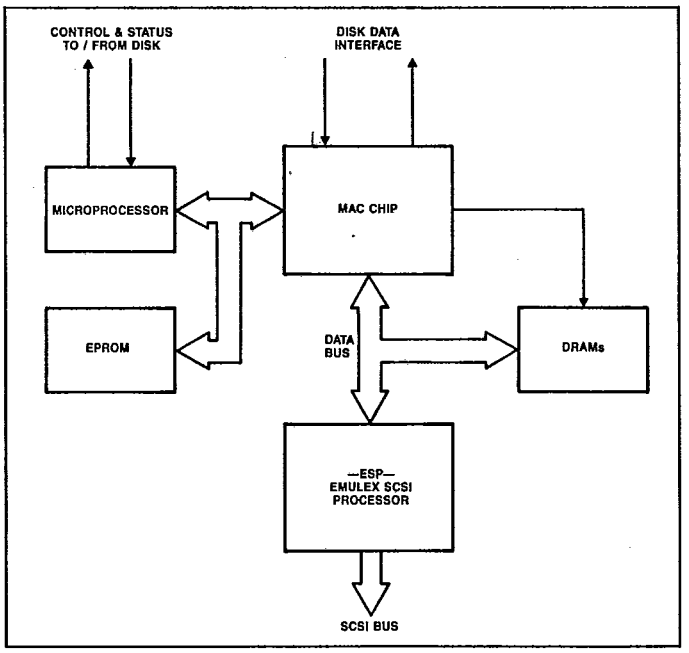

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Figure 2. Disk Controller

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PACKAGING

The MAC chip is available in two package types: a 100-pin gull-wing flat-pack for surface-mount applications and a 100-pin grid array (PGA) for through-hole mounting applications. The part numbers for the two packages are:

2400328	Gull-Wing Flat-Pack
2400126	Pin Grid Array

GLU MODULE

This module contains reset logic and the MAC Register, which is used to indicate reset status and to set some MAC chip configuration options. This module contains logic that is required for most controller applications and reduces the external logic required to design a controller around the MAC chip.

MAC Register

The MAC Register resides in the microprocessor address space. It is used to determine which reset condition caused an interrupt and for controller configuration. Figure 3 defines the MAC Register bits.

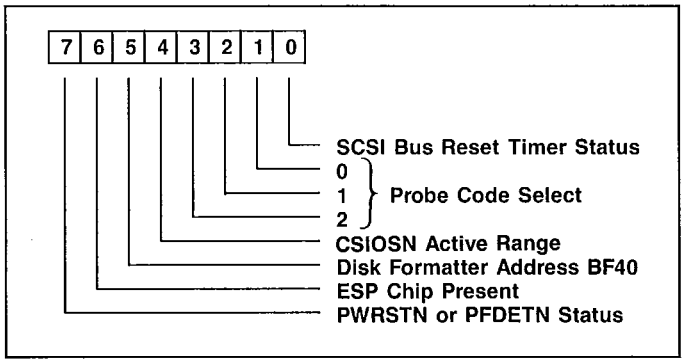

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Figure 3. MAC Register

1.6 Millisecond Timer

This serves as a 'watchdog' timer to ensure that the controller is initialized after a SCSI bus reset. The timer starts after the SCSI bus "reset" signal becomes inactive. It must be turned off by the microprocessor within 1.6 msec or the timer generates a hard reset on output pins RESETP and RESETG.

Reset Functions

The GLU Module contains logic for the propagation, control, and status of reset signals to the controller. There are three input signals that are used to initialize the MAC chip, which are passed on through one of several reset outputs. Figure 4 is a simplified illustration of the propagation paths for the signals through the GLU module. The table below defines the signals. See also Pin Descriptions.

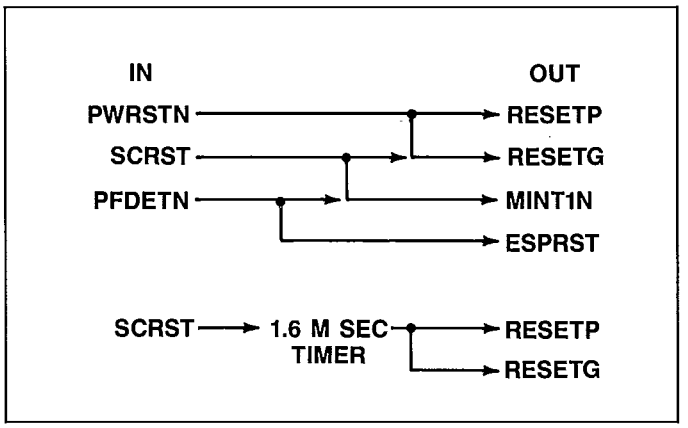

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Figure 4. Reset Propagation

Signal	Direction	Description
PWRSTN	IN	Main Reset Signal for MAC chip; initializes MAC chip. It is passed on as RESETP and RESETG.
SCRST	IN	SCSI Bus Reset Signal: Starts 1.6 msec watchdog timer on transition from true to false. Causes MINT1N interrupt.
PFDETN	IN	Power Fail/Detect: Interrupts the processor (MINT1N) and resets the SCSI protocol chip (if MAC Register, bit 6, is set).
RESETP	OUT	Reset Microprocessor: Can be held true by grounding DEBUGN for in-circuit emulator operation
RESETG	OUT	Reset General: Used to reset all controller logic except the microprocessor.
ESPRST	OUT	Reset SCSI Protocol Chip: Can be disabled by setting MAC Register, bit 6.

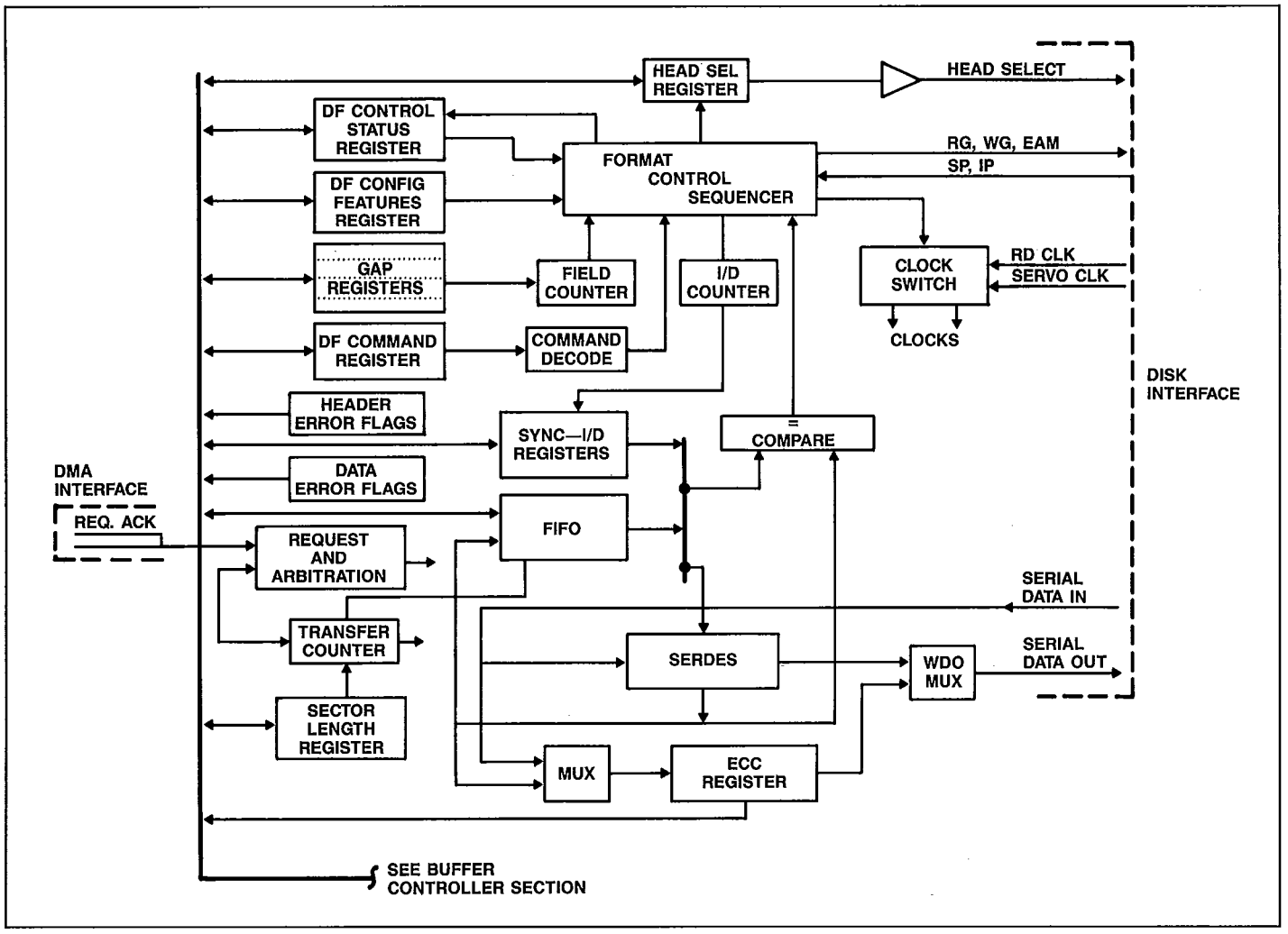

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Figure 5. Disk Formatter Block Diagram

DISK FORMATTER

The Disk Formatter Module provides a complete serial, read/write interface to ST-506/412, ESDI, SMD, and SMD-E drives. It resides on DMA channel 0, the highest priority DMA channel.

The DF2 can be configured to support a wide variety of media formats, which gives it the flexibility necessary to support high density disk drives.

Figure 5 is a detailed block diagram of the DF2. The major functional blocks include:

- The SERDES, which serializes and deserializes disk data
- The ECC Register, which generates and checks a 48-bit ECC for data fields and a 16-bit CRC for sector headers
- The Format Control Sequencer, which manages read, write, format and other commands in the sequence specified by the various configuration registers

Error Correction Capabilities

The MAC chip uses a 48-bit shift register (the ECC Register) to generate CRC and ECC fields for error detection and correction.

A sixteen-bit CRC code is used to detect errors in sector headers. The code used is the CRC-CCITT polynomial.

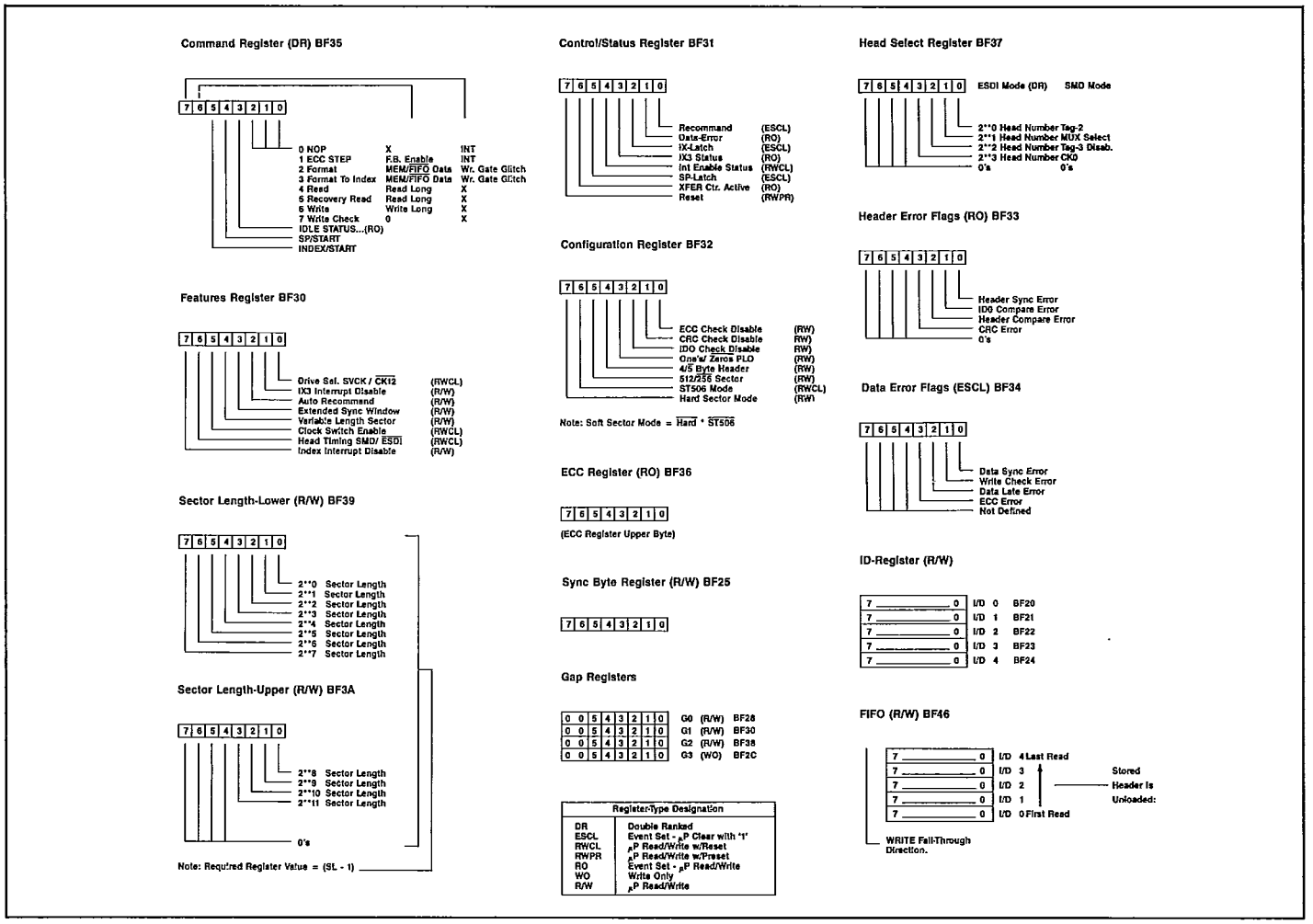

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Figure 6. Disk Formatter Registers

The MAC chip generates a 48-bit ECC code to allow both detection and correction of errors in data fields.

The controller's microprocesser uses the ECC code to correct single burst errors up to 19-bits span-width on 256-byte sectors or 15-bits on 4096-byte sectors.

DF2 Registers

Figure 6 shows the 21 DF2 registers that are accessible to the microprocessor. Values loaded into these registers control all operations of the disk interface.

The following paragraphs are general descriptions of the register functions. The absolute hex addresses (as defined by setting MAC Register, bit 5) of the registers are also shown in Figure 6.

Control and Status Register

This read/write register contains status and control information which allows the microprocessor to enable or disable interrupts, determine the cause of an interrupt, and reset the DF2 logic.

Configuration Register

This read/write register is used by the microprocessor to select various media format options and modes of operation. Including, sector mode (hard or soft), sector size, header size, PLO sync byte contents, and CRC/ECC check disable and header compare disable.

Header Error Register

This read-only register contains error bits associated with the header area of a sector. These include CRC, header compare, ID compare, and header sync errors.

Data Error Register

This read/clear register contains error bits associated with the data area of the sector, including ECC check, data late, write check, and data sync errors. If any error bit is set, the DF2 will cancel a pending command and ignore any new commands. The microprocessor must clear the error and reissue any commands that were pending. The conditions that set these bits also cause a Data Error Interrupt.

Command Register

This register is loaded with the next command to be executed by the DF2. The start of command execution is controlled by the value of bits 4 and 5:

Bits 5 4	Command Start Condition
0 0	Immediate
0 1	Sector Pulse
1 0	Index Pulse
1 1	Sector or Index Pulse

The microprocessor must clear the latched index pulse before issuing a command to start on index.

The DF2 implements the following commands:

Bits 2 1 0	Command
0 0 0	No Operation
0 0 1	ECC Step
0 1 0	Format
0 1 1	Format to Index
1 0 0	Read
1 0 1	Recovery Read
1 1 0	Write
1 1 1	Write Check

This register is double ranked. Data is always written to the first rank and read from the second rank. This allows the microprocessor to issue the next command while the current command is still executing.

ID Registers

The contents of these five registers hold the four or five bytes of the header. During read and write operations, the DF2 compares the contents of these registers with the corresponding bytes of the header read from the disk. During format operations, the DF2 writes the contents of these registers on the disk as the corresponding bytes of the header.

Sync Byte Register

This register defines the sync byte pattern used to detect the start of the header and data fields. The DF2 compares the contents of this register with the contents of the SERDES shift register to detect the occurrence of the sync pattern within the sync window. When executing a Format or Write command, the contents of this register are loaded into the shift register when writing the sync pattern.

FIFO Register

This register is the data FIFO. Writing into this pseudo-register loads the top of the FIFO. Reading this register unloads the bottom of the FIFO. The FIFO is accessed by the microprocessor during error correction sequences, and to read the header of a sector from the disk, when it did not compare to the ID registers.

Gap Registers

The four Gap Registers, known as G0, G1, G2, and G3, provide variable parameters for formatter gap timing. G0 defines the delay from command start to the assertion of Read Gate in hard sectored mode and the EAM delay time in soft sectored mode. G1 defines the length of the PLO sync area. G2 and G3 together define the start of the sync window and its length. The Gap Registers are 6 bits in length. The high-order 2 bits are zero when read. A Gap Register programmed with a binary number N counts N bytes with the exception of N equal to zero, which causes a count of 64 bytes.

ECC Register

This read-only register is the high-order eight bits of the ECC/CRC checker/generator. The ECC Register is loaded via the FIFO by using the Step command.

Head Select Register

This register has two different definitions, depending on whether the DF2 is configured for ESDI or SMD operation:

- In ESDI mode it is a 4-bit double-ranked register used for head selection. The head select output pins are updated while the sequencer is idle or between commands. The double ranking allows the microprocessor to preload the next head selection value without affecting the current operation.
- In SMD mode, this register is written to start a head select sequence; the data written has no effect. For this mode, the HSn pins become TAG2 Disable, Mux Select, TAG 3 and clock 0.

Sector Length Registers

These two read/write registers contain the 12-bit value used to define the number of bytes in the data field when variable length sectors are selected. The sector length is one byte longer than the value loaded into these registers.

Feature Register

This read/write register allows the microprocessor to select certain features or modes of operation, including head select mode, variable length sectors, and auto re-command mode.

BUFFER CONTROLLER

The buffer control module's basic function is to control data movement into and out of a dynamic RAM buffer memory, and to provide a connection between the two controller buses (the microprocessor bus and the buffer data bus). Figure 7 shows the internal organization of the BC2.

The BC2 supports four independent DMA channels, each with separate REQ/ACK signals to handle asynchronous data transfers. For DMA channel address management, the BC2 maintains separate 16-bit address pointer registers, limit registers, and reload registers. With the limit and reload registers, the microprocessor can create circular buffers on any modulo-256 byte boundary.

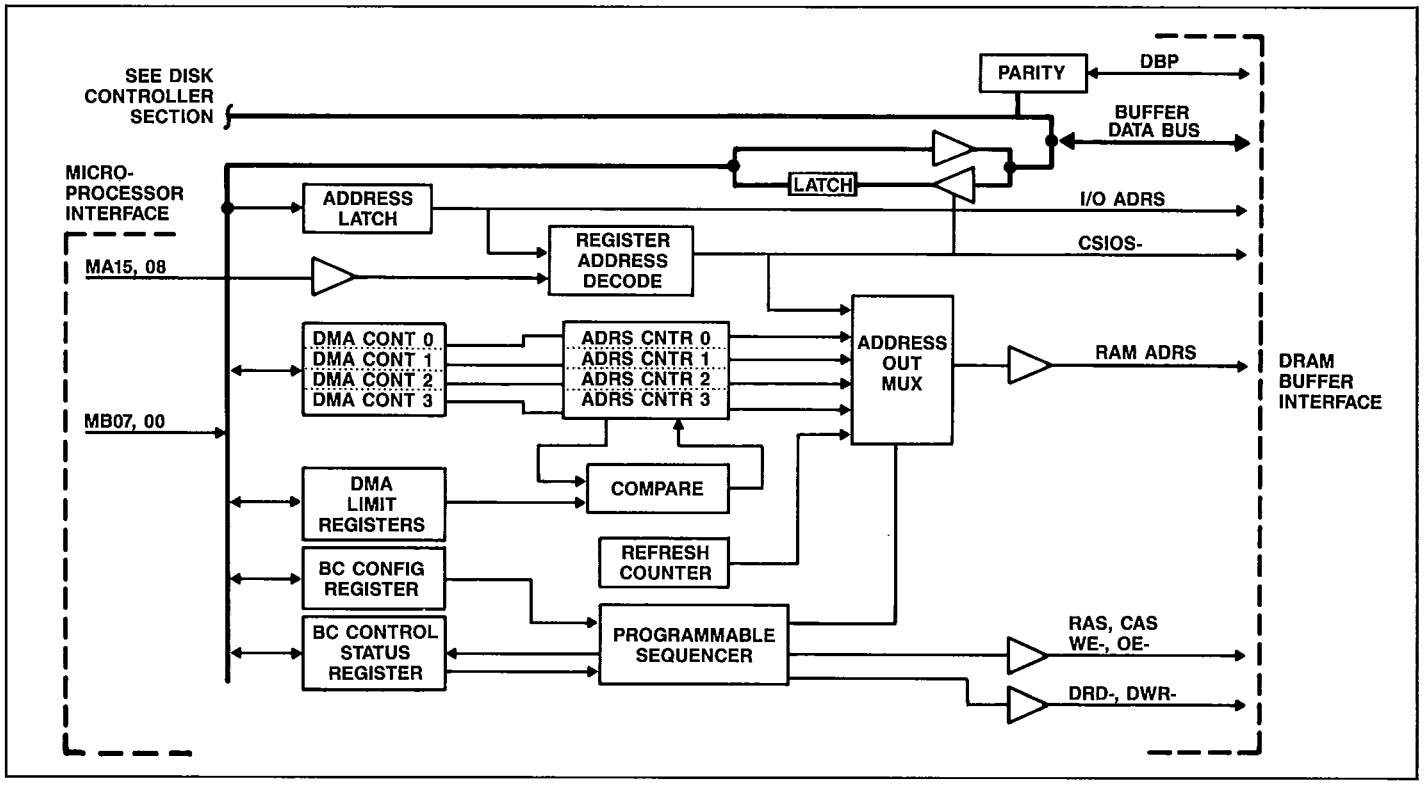

Figure 7. Buffer Controller Block Diagram

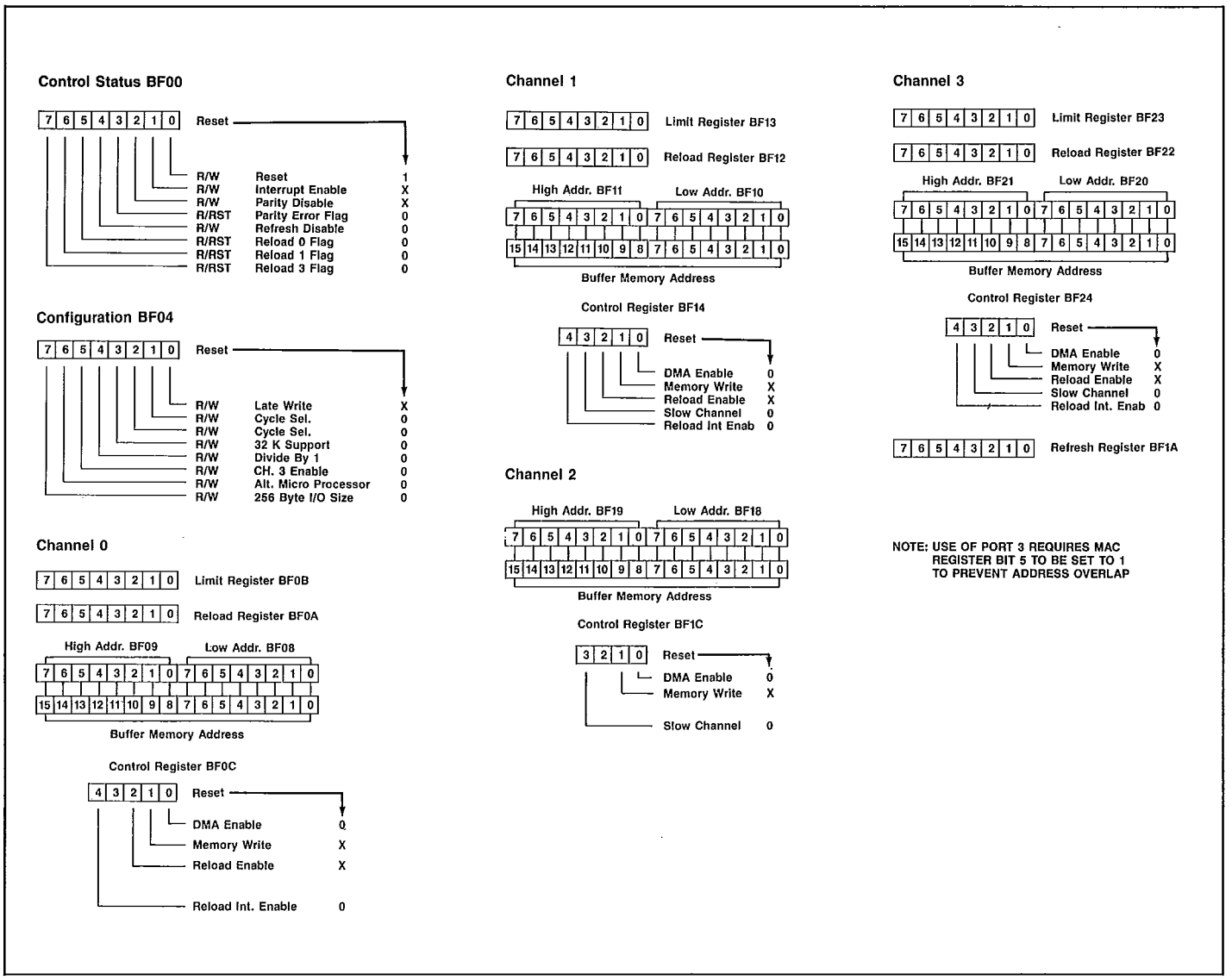

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Figure 8. Buffer Controller Registers

The BC2 interfaces to the eight-bit microprocessor bus and to the eight-bit buffer data bus. The microprocessor allows access to both buffer memory and the other devices on the buffer data bus. The BC2 outputs a multiplexed buffer address and directly controls signals RAS, CAS, BWEN and BOEN. This arrangement is suitable for directly addressing dynamic RAM memory chips.

Buffer Controller Registers

The BC2 contains the registers shown in Figure 8, which are used by the microprocessor to configure, control, and monitor DMA transfers between buffer RAM and external devices such as the Emulex SCSI Protocol Chip. A general description of the registers follows.

Control/Status Register

The Control and Status Register controls general BC2 functions. Three of the bits control parity generation and detection. Refresh can be disabled with the Refresh Disable bit. Another bit is used to reset the BC2 or indicate that it has been reset by the external RESET input. Additional bits allow the microprocessor to identify the DMA channel that interrupted on an address reload.

The microprocessor uses this register to configure the BC2 for operation in different controller environments.

Because the BC2 decodes the microprocessor's memory addresses, the BC2 determines how the processor's address space is mapped. Figure 9 shows the four address maps that are supported. Setting bit 7 selects a page size of 256 bytes instead of 4096. Also, setting bit 6 causes the I/O page of memory to start at F000 instead of B000. These mapping options allow the MAC to support microprocessors other than the 8031.

Bits 2 and 1 of this register select the clock divide factor. Combining the four divide factors with various clock speeds allows the MAC to support a wide range of DRAM cycle times. See the following table.

Bit 2	1	Divide Factor	External Clock Speed 24 MHz	20 MHz	16 MHz
0	0	10	416 ns	500 ns	625 ns
0	1	8	333 ns	400 ns	500 ns
1	0	6	250 ns	300 ns	375 ns
1	1	4			250 ns
			DRAM Cycle Time		

All four DMA channels use the cycle time established by this register. However, channels one, two, and three may be separately programmed to operate in 10-cycle mode by setting the slow-channel bit in the appropriate Channel Control Register. This feature allows the MAC to operate with devices such as floppy disk controller chips.

There are four sets of four registers which are used to configure and control the DMA channels. The register sets function identically; however, channel two (the lowest priority channel) does not support automatic reload, and channel zero (the highest priority channel) does not support the slow channel feature. The registers are discussed below. First, however, a general description of the DMA process:

To set up a DMA transfer, the microprocessor loads a DMA starting address into the buffer memory address counter (accessed via the High and Low Address Registers) and sets the DMA enable bit in the Port Control Register. The transfer is then controlled by the DMA device connected to that channel using the REQ/ACK signal pair. The DMA device contains the byte counter for the transfer.

If the reload feature is enabled, and if the buffer memory address equals the value in the limit register, the buffer memory address counter will be loaded with the value in the reload register.

Low and High Address Registers The microprocessor uses these read/write registers to load the 16-bit buffer memory address register, which contains the address pointer used by the BC2 to generate buffer addresses. During DMA, the buffer memory address register is incremented with every byte that is transferred.

Limit and Reload Registers These registers are used to implement the BC2's automatic address reload feature. The Limit Register contains the most significant byte of the limit address. The least significant byte is always FF. When the buffer memory address register equals the value specified in the Limit Register, it is loaded with the value in the Reload Register. The Reload Register contains the most significant byte of the reload address. The least significant byte of the new address will be 00.

This reload feature can be used to create large circular buffers without the microprocessor having to reload the buffer address. The buffers will be on modulo-256 byte boundaries.

Channel Control Register The microprocessor uses this register to select configurations specific to a DMA channel and to enable the DMA channel after configuring it.

Refresh Register

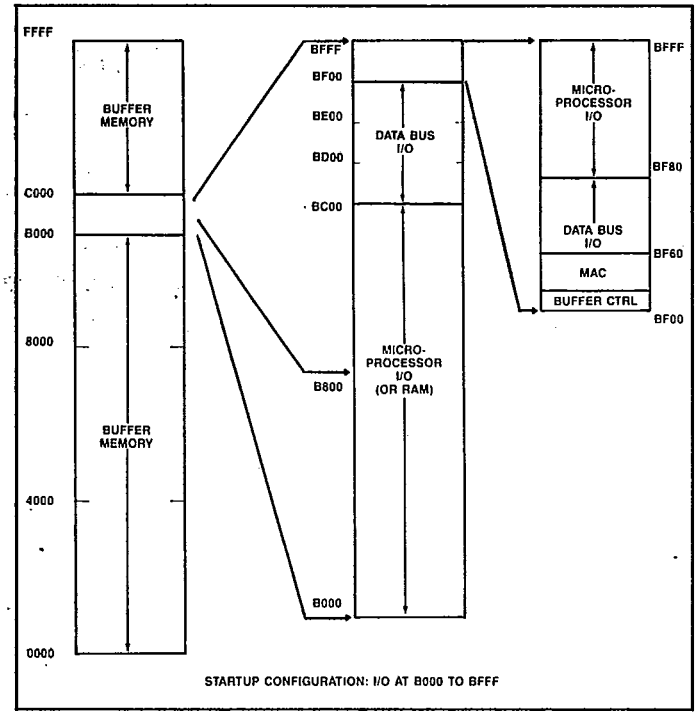
This read/write register allows the microprocessor access to the refresh address counter. This counter supplies the row address the BC2 uses for refresh cycles on the dynamic RAM buffer.

When the BC2 is initialized, this counter is set to FF. The counter is incremented after each refresh cycle. Refresh cycle period is obtained by dividing the 20/24 MHz clock by 1.8, which produces a 10.7 or 12.8 microsecond period, respectively.

The refresh channel has the lowest priority of the BC2's five channels. However, normal DMA activity will refresh buffer memory should the refresh channel be locked out by higher priority channels.

PORTS

The MAC chip has three basic ports: the microprocessor port, disk formatter port, and the buffer data port. These ports have some special features which are discussed below.



STARTUP CONFIGURATION: I/O AT B000 TO BFFF

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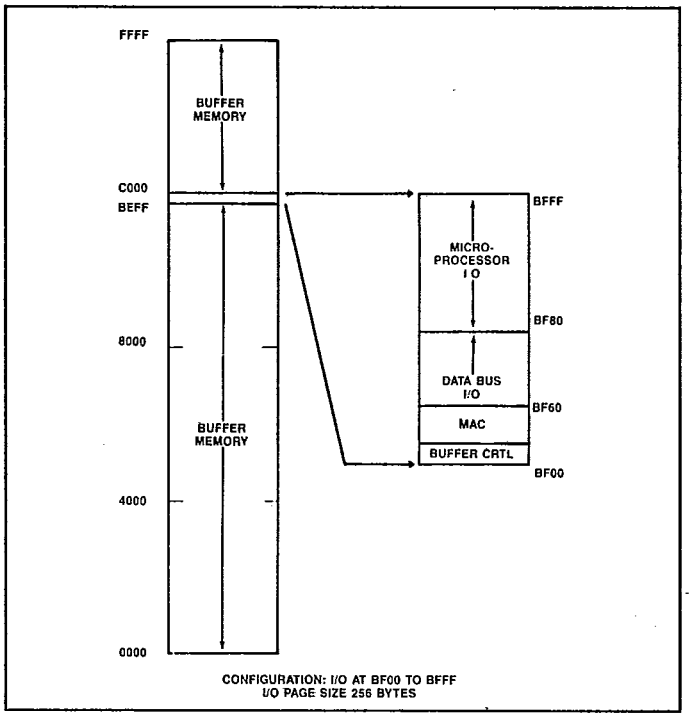

CONFIGURATION: I/O AT BF00 TO BFFF
I/O PAGE SIZE 256 BYTES

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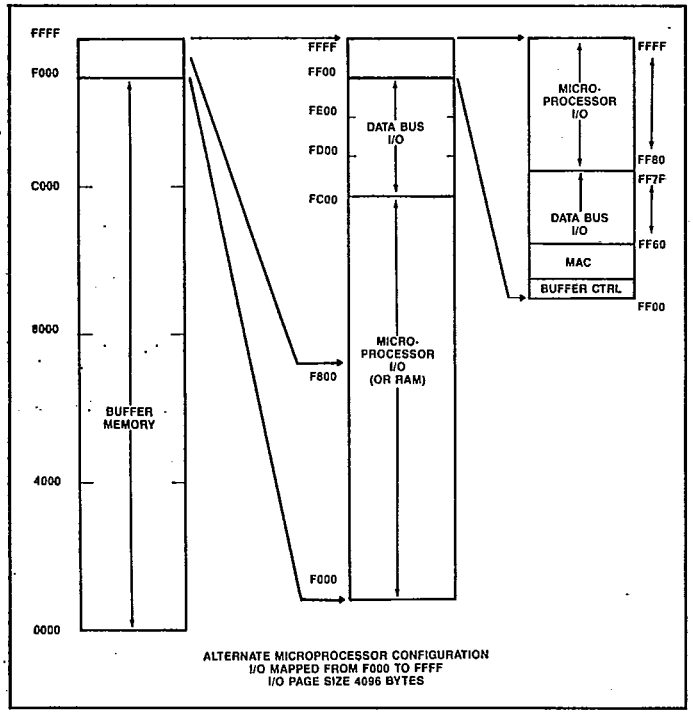

ALTERNATE MICROPROCESSOR CONFIGURATION
I/O MAPPED FROM F000 TO FFFF
I/O PAGE SIZE 4096 BYTES

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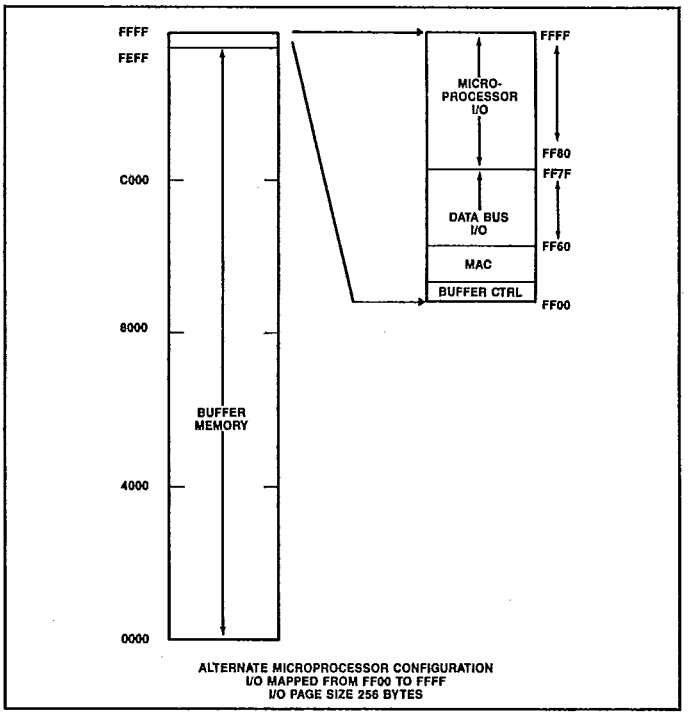

ALTERNATE MICROPROCESSOR CONFIGURATION
I/O MAPPED FROM FF00 TO FFFF
I/O PAGE SIZE 256 BYTES

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Figure 9. Controller Memory Allocation

Microprocessor Port

The MAC chip interfaces directly to the eight-bit multiplexed address and buffer data bus of the 8031 microprocessor. The microprocessor ALE signal controls an internal latch that holds the low-order address bits. The latched address is available on the LMA7-0 pins. Interfaces to non-multiplexed and 16-bit microprocessors can be implemented by the addition of external circuitries.

The MAC chip decodes the 8031's high-order address byte to distinguish between accesses to the I/O page or buffer memory. The MAC then generates the appropriate chip selects (I/O page) or multiplexed buffer address. This feature eliminates the requirement for discrete address decode logic and buffer memory address generation logic.

Data Buffer Port

The Data Buffer Port connects the MAC chip to the data buffer. It consists of an eight-bit buffer data bus, a 16-bit multiplexed address bus, RAS, CAS, CASCAM, BWEN, and BOEN signals. It interfaces directly to most families of dynamic RAMs, including both by-one (64K x 1) and by-four (64K x 4) configurations of DRAMs. Figure 10 illustrates MAC chip applications with these two different DRAM types.

The Data Buffer Port also includes the REQ and ACKN signal pairs for each DMA channel (except channel 0, which is dedicated to the DF2 and therefore internal to the MAC). Other VLSI devices in the controller use the REQ and ACKN signals to control data transfers between themselves and the buffer RAM.

BA07-BA00 RAM Address Lines: The table below shows what addresses are presented on the associated RAM address lines during the row address strobe (RASN) and column address strobe (CASN) times.

Output Pins	BA07	BA06	BA05	BA04	BA03	BA02	BA01	BA00
at RASN time :	A7	A6	A5	A4	A3	A2	A1	A0
at CASN time :	A15	A8	A13	A12	A11	A10	A9	A14

The four DMA channels, microprocessor accesses, and refresh functions are prioritized to resolve potential conflicts between VLSI devices that attempt to conduct DMA at the same time (i.e., two REQ signals received at the same time). The priority is as follows:

Function	Rank	Comment
Microprocessor	0	Highest
DMA Channel 0 (DF2)	1	
DMA Channel 1	2	
DMA Channel 3	3	
DMA Channel 2	4	
Refresh	5	

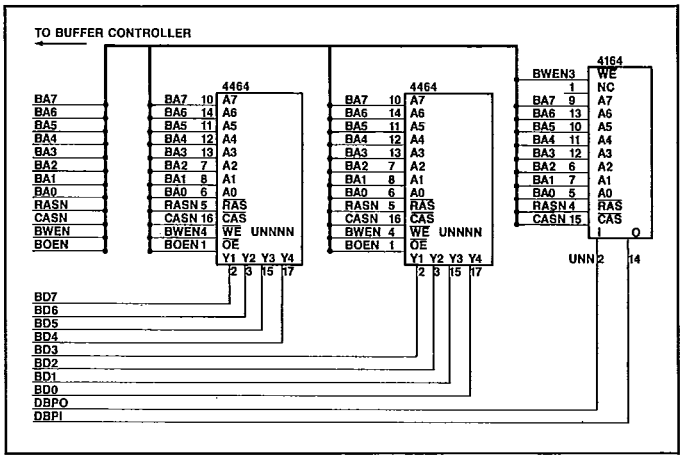

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Figure 10. 64K RAM Using 64K x 4 Parts

Disk Formatter Port

For embedded controller applications of the MAC chip, the disk interface signals can be connected directly to the drive electronics. When used in a stand-alone controller, additional control and status latches and interface drivers are usually required.

Serial input timing is derived from five disk signals: sector pulse (SP), index pulse (IP), servo clock (SVCLK), read clock (RCI), and read data (RDI). The DF2 generates serial output timing for the following disk signals: read gate (RG), write gate (WG), enable address mark (EAM), write clock out (WCO), write data (WDO), and head select (HS0-HS3).

Additional head select lines can be added by using a single, discrete read/write latch. The microprocessor would directly access the head select lines controlled by this latch.

PIN DESCRIPTION

The pin designations for the two packages in which the MAC is available are shown in Figures 12 and 13. A description of pin functions are in the table that follows.

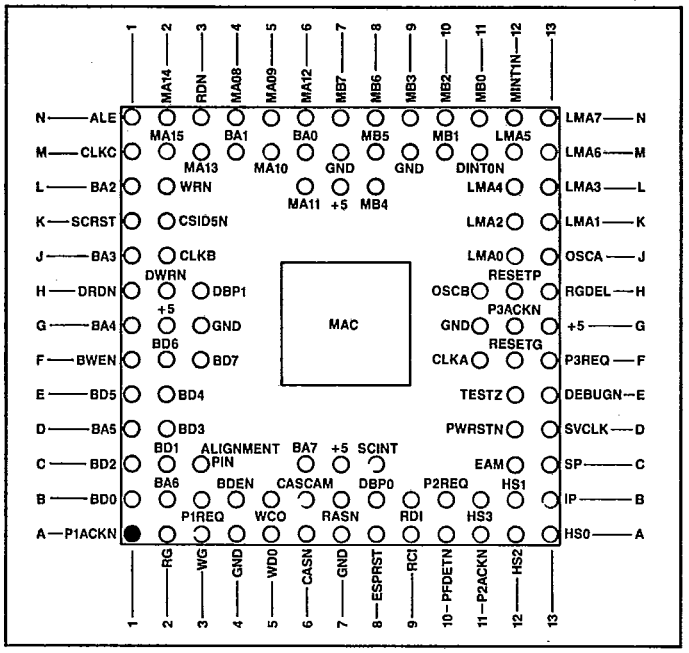

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Figure 12. Pin Grid Array

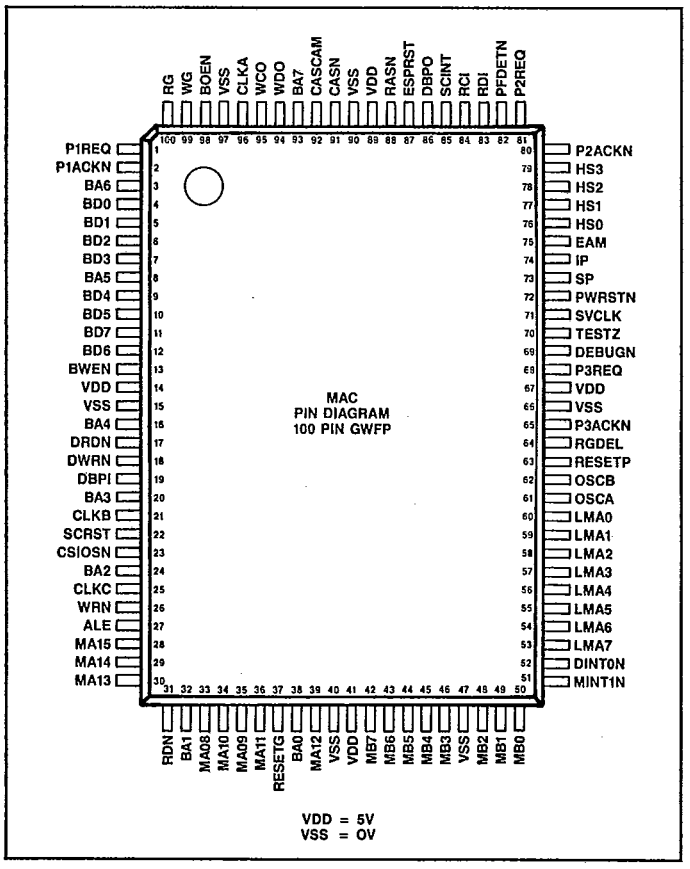

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Figure 13. Gull-wing Flat-Pack

Crystal Oscillator Input

The MAC provides for the use of a crystal oscillator or an external clock input. The crystal used should have the following parameters:

Crystal Type : AT Cut
Frequency : Fundamental
Mode : Series Resonant

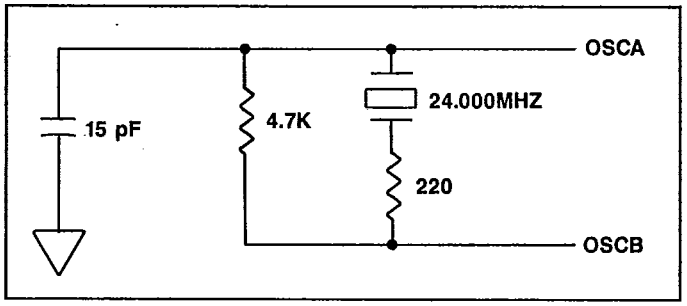

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Figure 14. Typical Crystal Oscillator Circuit

Signal	Pin No. Flat	Pin No. PGA	Dir.	Driver	Function
RDN	31	N03	I		µP Read Enable
WRN	26	L02	I		µP Write Enable
ALE	27	N01	I		µP ALE
MINT1N	51	N12	O	TTL2	µP Interrupt 1
DINTON	52	M11	O	TTL2	µP Interrupt 0
RESETP	63	H12	O	TTL2	µP Reset Out
MA15	28	M02	O	TTL4	µP Address Bus 15
MA14	29	N02	O	TTL4	µP Address Bus 14
MA13	30	M03	O	TTL4	µP Address Bus 13
MA12	39	N06	O	TTL4	µP Address Bus 12
MA11	36	L06	O	TTL4	µP Address Bus 11
MA10	34	M05	O	TTL4	µP Address Bus 10
MA09	35	N05	O	TTL4	µP Address Bus 09
MA08	33	N04	O	TTL4	µP Address Bus 08
MB7	42	N07	I/O	3state	µP Data/Address Bus 7
MB6	43	N08	I/O	3state	µP Data/Address Bus 6
MB5	44	M08	I/O	3state	µP Data/Address Bus 5
MB4	45	L08	I/O	3state	µP Data/Address Bus 4
MB3	46	N09	I/O	3state	µP Data/Address Bus 3
MB2	48	N10	I/O	3state	µP Data/Address Bus 2
MB1	49	M10	I/O	3state	µP Data/Address Bus 1
MB0	50	N11	I/O	3state	µP Data/Address Bus 0
LMA7	53	N13	O	TTL4	Latched µP Address 7
LMA6	54	M13	O	TTL4	Latched µP Address 6
LMA5	55	M12	O	TTL4	Latched µP Address 5
LMA4	56	L12	O	TTL4	Latched µP Address 4
LMA3	57	L13	O	TTL4	Latched µP Address 3
LMA2	58	K12	O	TTL4	Latched µP Address 2
LMA1	59	K13	O	TTL4	Latched µP Address 1
LMA0	60	J12	O	TTL4	Latched µP Address 0

(continued)

(continued)

Signal	Pin No. Flat	PGA	Dir.	Driver	Function
P1REQ	1	B03	I		Channel 1 REQ
P1ACKN	2	A01	O	TTL4	Channel 1 ACK
P2REQ	81	B10	I		Channel 2 REQ
P2ACKN	80	A11	O	TTL4	Channel 2 ACK
P3REQ	68	F13	I		Channel 3 REQ
P3ACKN	65	G12	O	TTL4	Channel 3 ACK
DRDN	17	H01	O	TTL4	Data Bus Read Enable
DWRN	18	H02	O	TTL4	Data Bus Write Enable
CSIOSN	23	K02	O	TTL4	Data Bus CSN - IOSN
DBPO	86	B08	I/O	3state	Data Bus Parity Out
DBPI	19	H03	I		Data Bus Parity In
BD7	11	F03	I/O	3state	Buffer Data Bus Bit 7
BD6	12	F02	I/O	3state	Buffer Data Bus Bit 6
BD5	10	E01	I/O	3state	Buffer Data Bus Bit 5
BD4	9	E02	I/O	3state	Buffer Data Bus Bit 4
BD3	7	D02	I/O	3state	Buffer Data Bus Bit 3
BD2	6	C01	I/O	3state	Buffer Data Bus Bit 2
BD1	5	C02	I/O	3state	Buffer Data Bus Bit 1
BD0	4	B01	I/O	3state	Buffer Data Bus Bit 0
RASN	88	B07	O	TTL12	Buffer Row Address Strobe
CASN	91	A06	O	TTL12	Buffer Column Address Strobe
CASCAM	92	B06	O	TTL8	Buffer CASB/ CAM/ Probe
BWEN	13	F01	O	TTL12	Buffer Write Enable
BOEN	98	B04	O	TTL8	Buffer Output Enable
BA7	93	C06	O	TTL8	Buffer Address 07 or 15
BA6	3	B02	O	TTL8	Buffer Address 06 or 08
BA5	8	D01	O	TTL8	Buffer Address 05 or 13
BA4	16	G01	O	TTL8	Buffer Address 04 or 12
BA3	20	J01	O	TTL8	Buffer Address 03 or 11
BA2	24	L01	O	TTL8	Buffer Address 02 or 10
BA1	32	M04	O	TTL8	Buffer Address 01 or 09
BA0	38	M06	O	TTL8	Buffer Address 00 or 14
RG	100	A02	O	TTL4	Read Gate Out
RGDEL	64	H13	I		Read Gate Delayed In
WG	99	A03	O	TTL4	Write Gate Out
EAM	75	C12	O	TTL4	Enable Address Mark
SP	73	C13	I		Sector Pulse
IP	74	B13	I		Index Pulse
RDI	83	B09	I		Serial Read Data In
RCI	84	A09	I		Serial Read Clock In
WDO	94	A05	O	TTL4	Serial Write Data Out
WCO	95	B05	O	TTL4	Serial Write Clock Out
SVCLK	71	D13	I		Servo Clock In
HS0	76	A13	O	TTL4	Head Select 0
HS1	77	B12	O	TTL4	Head Select 1
HS2	78	A12	O	TTL4	Head Select 2
HS3	79	B11	O	TTL4	Head Select 3
PWRSTN	72	D12	I		Power-On Reset
PFDETN	82	A10	I		Power-Fail/Detect
RESETG	37	F12	O	TTL4	General Reset Out
ESPRST	87	A08	O	TTL4	SCSI Chip Reset
SCINT	85	C08	I		SCSI Chip Interrupt
SCRST	22	K01	I		SCSI Bus Reset

(continued)

(continued)

Signal	Pin No. Flat	PGA	Dir.	Driver	Function
OSCA	61	J13	I		XTAL In (External Clock)
OSCB	62	H11	O	TTL4	XTAL Out
CLKA	96	F11	O	TTL4	Clock Div-1
CLKC	25	M01	O	TTL4	Clock Div-3
CLKB	21	J02	O	TTL4	Clock Div-2
TESTZ	70	E12	I		Test Enable
DEBUGN	69	E13	I		ICE Enable
V_{DD}	14	G02			+5 v
V_{DD}	41	L07			+5 v
V_{DD}	67	G13			+5 v
V_{DD}	89	C07			+5 v
V_{SS}	15	G03			GND
V_{SS}	40	M07			GND
V_{SS}	47	M09			GND
V_{SS}	66	G11			GND
V_{SS}	90	A07			GND
V_{SS}	97	A04			GND

Operating Characteristics

Absolute Maximum Ratings (Referenced to V_{SS})			
Symbol	**Parameter**	**Limits**	**Unit**
V_{DD}	DC Supply Voltage	-0.3 to +7.0	V
V_I	Input Voltage	-0.3 to V_{DD} +0.3	V
I_I	DC Input Current	±10	mA
T_{STG}	Storage Temperature Range (Ceramic)	-65 to +150	°C
T_{STG}	Storage Temperature Range (Plastic)	-40 to +125	°C
Recommended Operating Conditions			
Symbol	**Parameter**	**Range**	**Unit**
V_{DD}	DC Supply Voltage	5.0	V
T_A	Operating Ambient Temperature Range	0 to +70	°C
RCI, RDI, SVCLK	Serial Data Bit Rate	0 to 25	MHz
OSCA-OSCB	Rate	0 to 24	MHz

Embedded

Storage

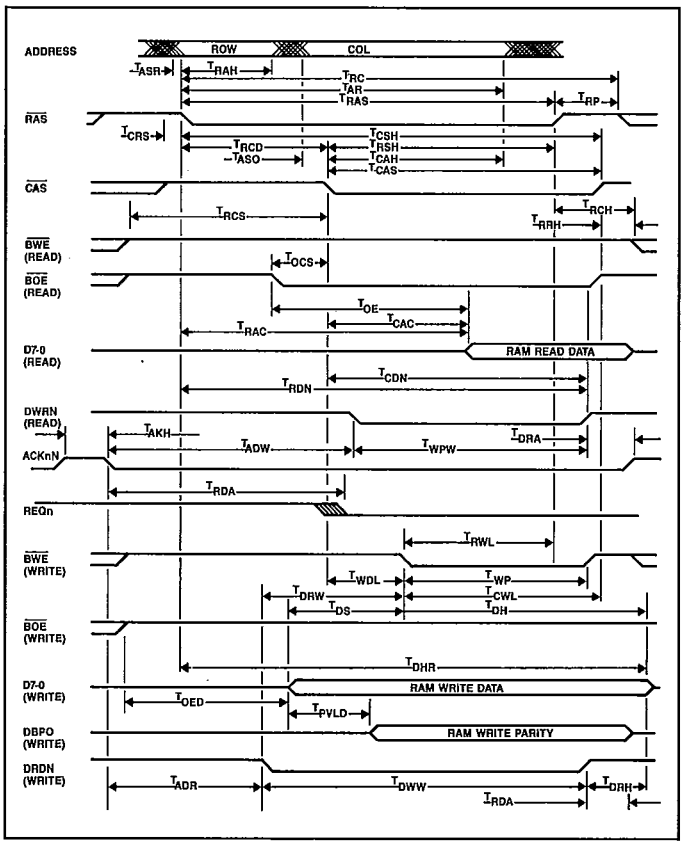
Technology

DC Electrical Characteristics

Specified at V_{DD} = 5V ±5% over the temperature of 0 to +70°C						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
V_{IL}	Low Level Input Voltage			0.8	V	
V_{IH}	High Level Input Voltage	2.0	1.7		V	
I_{IN}	Input Current	-10	+1	10	μA	V_{IN} = +5 Vdc
V_{OH}	High Level Output Voltage					Maximum Current (source)
	Type 3state	2.4	4.5		V	I_{OH} = -4.0 mA
	Type TTL2	2.4	4.5		V	I_{OH} = -2.0 mA
	Type TTL4	2.4	4.5		V	I_{OH} = -4.0 mA
	Type TTL8	2.4	4.5		V	I_{OH} = -8.0 mA
	Type TTL12	2.4	4.5		V	I_{OH} = -12.0 mA
V_{OL}	Low Level Output Voltage					Maximum Current (sink)
	Type 3state		0.2	0.4	V	I_{OL} = 4.0 mA
	Type TTL2		0.2	0.4	V	I_{OL} = 2.0 mA
	Type TTL4		0.2	0.4	V	I_{OL} = 4.0 mA
	Type TTL8		0.2	0.4	V	I_{OL} = 8.0 mA
	Type TTL12	2.4	0.2	0.4	V	I_{OL} = 12.0 mA
I_{OZ}	Tri-State Output Leakage Current	-10	±1	10	μA	V_{OH} = V_{SS} or V_{DD}
I_{OS}	Output Short[1] Circuit Current	25		90	mA	V_{DD} = Max, VO = V_{DD}
		-7		-28	mA	V_{DD} = Max, VO = 0V
I_{DD}	Quiescent Supply Current		100		mA	V_{IN} = +5Vdc RCI = 15 MHz OSCA = 24 MHz
C_{IN}	Input Capacitance		5		pF	Any Input[2]
C_{OUT}	Output Capacitance		7		pF	Any Output[2]

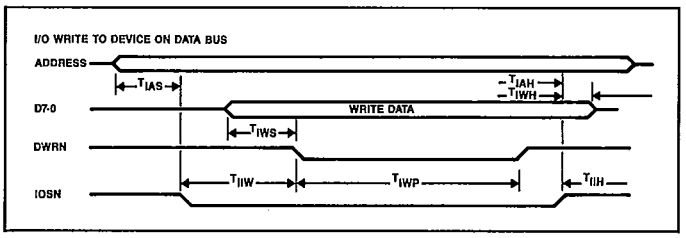
[1] Type TTL8 output. Output short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.

[2] Not applicable to bi-directional pins.



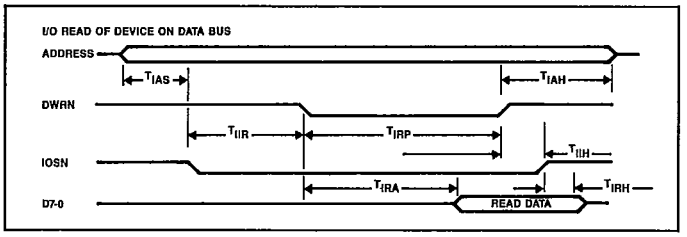
1166

Figure 15. Buffer Memory Read and Write Operation



1251A

Figure 16. I/O Write to Device on Data Bus

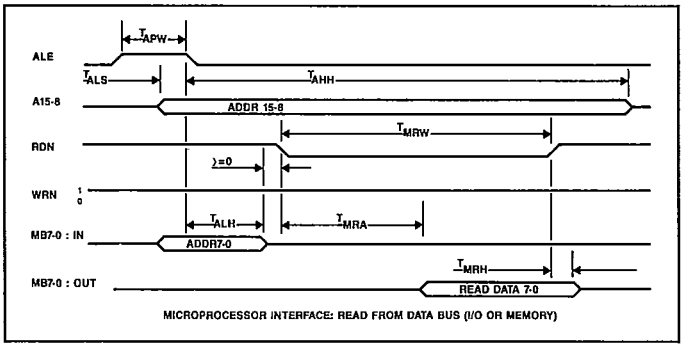


1251B

Figure 17. I/O Read of Device on Data Bus

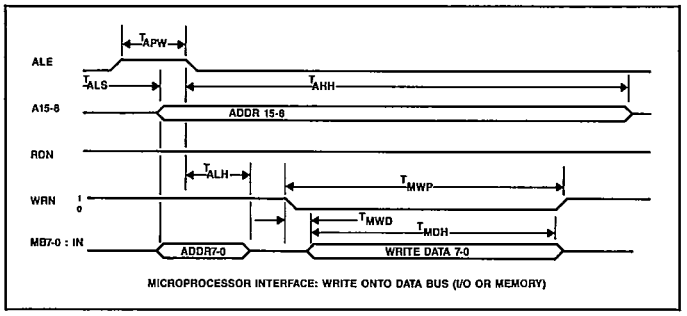
AC Timing

The following figures and the table of values that accompany them are illustrative of the MAC chip's AC timing characteristics. For definitive values, see the MAC Applications Manual or Specification.



1167A

Figure 18. Microprocessor Interface: Read from Data Bus (I/O or Buffer)



1167B

Figure 19. Microprocessor Interface: Write onto Data Bus (I/O or Buffer)

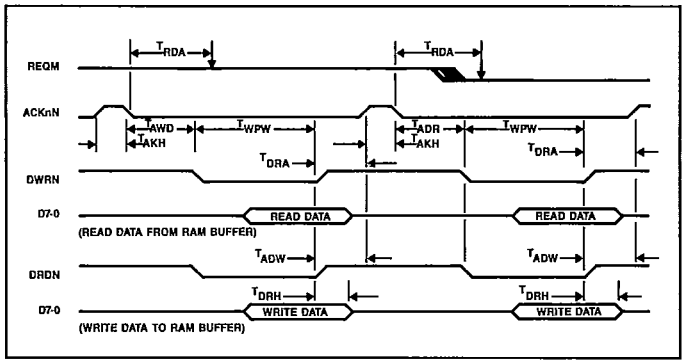


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Figure 20. DMA Read/Write Handshake Timing

MAC Chip Buffer Control Timing

Oscillator Frequncy	24.00	MHz
Duty Cycle	35/65	Per Cent
Cycle Time	6	
Transfer Rate	4.00	M Bytes/Sec
Conditions: 0 to 70°C, 4.75 to 5.25 V, 85 Pfd on all lines		

Symbol	Parameter	Min	Max	Units
T_{ADR}	ACKxN Active to DRDN Active	12	35	Nsec
T_{ADW}	DRDN (L-H) to ACKxN (L-H) (end)	12	33	Nsec
T_{AHH}	High Order Address Hold[1]	—	625	Nsec
T_{AKH}	Minimum ACKxN High (back to back)	9	29	Nsec
T_{ALH}	Address to ALE Hold	17	—	Nsec
T_{ALS}	Address to ALE Setup	2	—	Nsec
T_{APW}	ALE Pulse Width	14	—	Nsec
T_{AR}	Column Address Hold (reference RAS)	125	152	Nsec
T_{ASC}	Column Address Setup Time	10	29	Nsec
T_{ASR}	Row Address Setup Time	83	125	Nsec
T_{AWD}	ACKxN (H-L) to DWRN (H-L)	83	91	Nsec
T_{CAC}	Access from CAS	114	125	Nsec
T_{CAH}	Column Address Hold Time	83	111	Nsec
T_{CAS}	CAS Pulse Width	120	125	Nsec
T_{CDN}	CASN (H-L) to DWRN (L-H)	95	112	Nsec
T_{CRS}	CAS to RAS Setup Time	83	89	Nsec
T_{CSH}	CAS Hold Time	162	167	Nsec
T_{CWL}	BWEN to CASN Lead	95	115	Nsec
T_{CYC}	OSCA Cycle Time	0	24	Mhz
T_{DH}	Data in Hold (late write)	83	86	Nsec
T_{DHR}	Data in Hold Time (reference RAS)	133	154	Nsec
T_{DRA}	DWRN(L-H) to ACKxN (L-H) (end)	12	33	Nsec
T_{DRH}	Data Hold After DRDN (0-1)	0	12	Nsec
T_{DRW}	DRDN to BWEN (late write)	86	112	Nsec
T_{DS}	Data in Setup (late write)	86	112	Nsec
T_{DWW}	DRDN Pulse Width	173	196	Nsec
T_{IAH}	I/O Address Hold Time	—	71	Nsec
T_{IAS}	I/O Address Setup Time	—	125	Nsec
T_{IIH}	I/O Select Off After DWRN Off	11	29	Nsec
T_{IIR}	I/O Select On to DRDN On	49	71	Nsec
T_{IIW}	I/O Strobe to DWRN	95	115	Nsec
T_{IRH}	I/O Read, Read Data Hold Time	0	—	Nsec
T_{IRP}	I/O DRDN Pulse Width	162	167	Nsec
T_{IWH}	I/O Write Data Hold	12	—	Nsec
T_{IWP}	I/O DWRN Pulse Width	114	125	Nsec
T_{IWS}	I/O Write Data to DWRN	95	118	Nsec
T_{MRA}	Read Access (Data Bus)[1]	—	563	Nsec
T_{MRH}	Read Hold Data (Data Bus)	0	15	Nsec
T_{MRM}	RDN Width (Data Bus)[1]	625	No Limit	Nsec
T_{MWD}	WRN to Write Data (Data Bus)	—	71	Nsec
T_{MWH}	Write Data Hold (Data Bus)	—	563	Nsec
T_{MWP}	WRN Pulse Width (Data Bus)	—	625	Nsec
T_{OCH}	OSCA/OSCB Minimum High Time	12	—	Nsec
T_{OCL}	OSCA/OSCB Minimum Low Time	12	—	Nsec
T_{OCS}	OE Setup to CASN-Out Disable	129	143	Nsec

(continued)

MAC Chip Buffer Control Timing (continued)

Symbol	Parameter	Min	Max	Units
T_{OE}	Access Time from BOEN	125	162	Nsec
T_{OED}	BOEN high to Data In	42	45	Nsec
T_{RAC}	Access from RAS	144	167	Nsec
T_{RAH}	Row Address Hold Time	12	29	Nsec
T_{RAS}	RAS Pulse Width (low)	137	158	Nsec
T_{RC}	Read Cycle Time	250	250	Nsec
T_{RCD}	RAS to CAS Delay	40	44	Nsec
T_{RCH}	Read Command Hold Time (reference CAS)	95	108	Nsec
T_{RCS}	Read Command Setup Time	105	137	Nsec
T_{RDA}	Request Valid after PxACKN (1-0)	102	154	Nsec
T_{RDE}	DRDN to CASN (early write)	81	83	Nsec

MAC Chip Buffer Control Timing (continued)

Symbol	Parameter	Min	Max	Units
T_{RDN}	RASN (H-L) to DW/RN (L-H)	137	154	Nsec
T_{REF}	Refresh Period	2.69	2.77	Nsec
T_{RP}	RAS Precharge Time	91	112	Nsec
T_{RPW}	Reset Width (minimum 4 x OSCA)	167	---	Nsec
T_{RRH}	Read Command Hold Time (reference RAS)	125	131	Nsec
T_{RSH}	RAS Hold Time	99	120	Nsec
T_{RWL}	Write Command to RAS Lead	86	112	Nsec
T_{WDL}	CASN (H-L) to BW/EN (H-L)	5	29	Nsec
T_{WP}	BW/EN Pulse Width (late write)	54	74	Nsec
T_{WPW}	DW/RN Pulse Width	114	125	Nsec

[1] During these cycles the microprocessor clock is generated one out of five cycles to insure specifications listed.

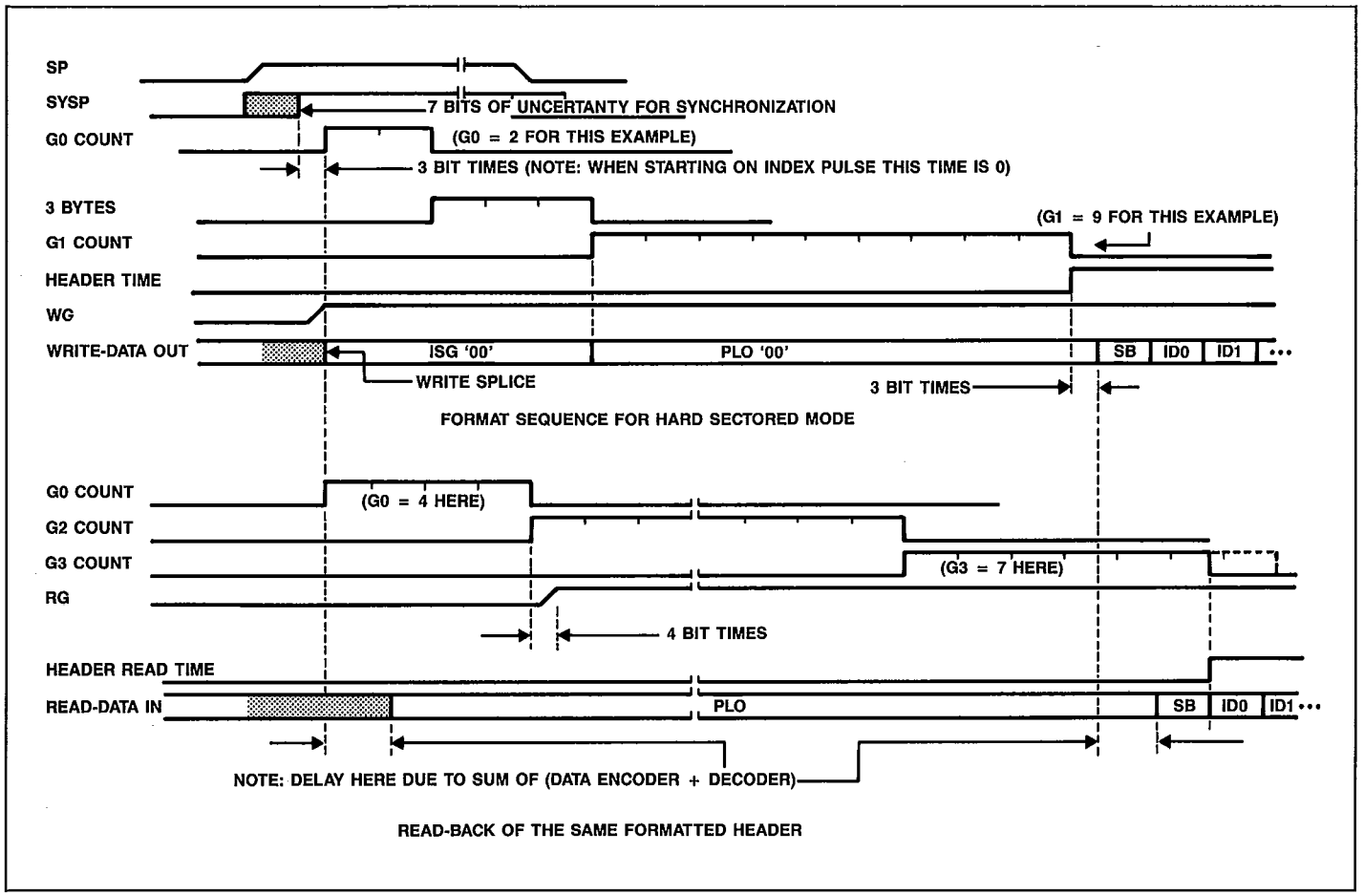

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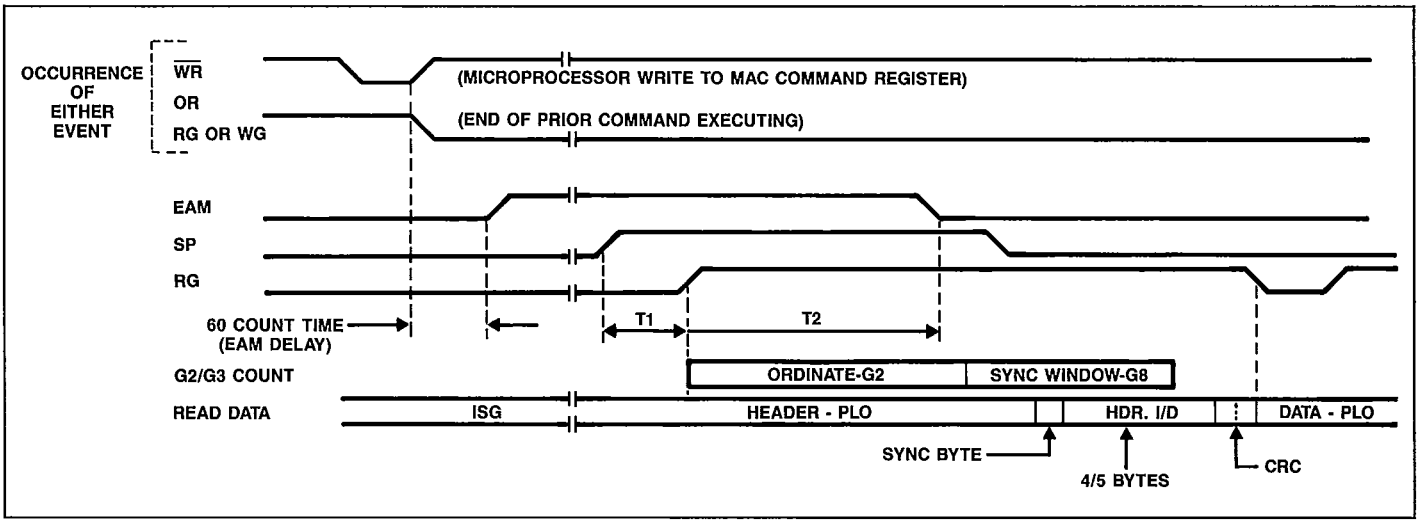
Figure 21. Hard Sector Read Timing

3372 C-07



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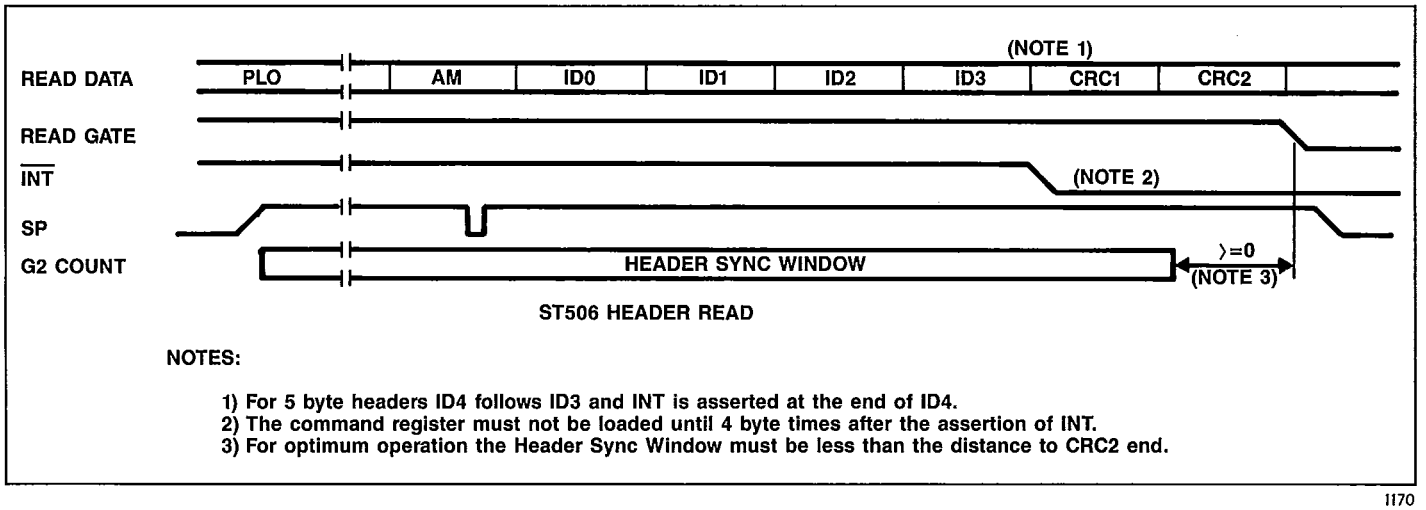
Symbol	Condition	Minimum	Maximum	Unit
T1	SP (Address Mark Found) to Read Gate Asserted	9	14	Bit Times
T2	Read Gate Asserted to SP Off	0	G2-2	Byte Times

Figure 22. Soft Sector Read Timing



ST506 HEADER READ

NOTES:

1) For 5 byte headers ID4 follows ID3 and INT is asserted at the end of ID4.
2) The command register must not be loaded until 4 byte times after the assertion of INT.
3) For optimum operation the Header Sync Window must be less than the distance to CRC2 end.

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Figure 23. ST-506 Sector Read Timing

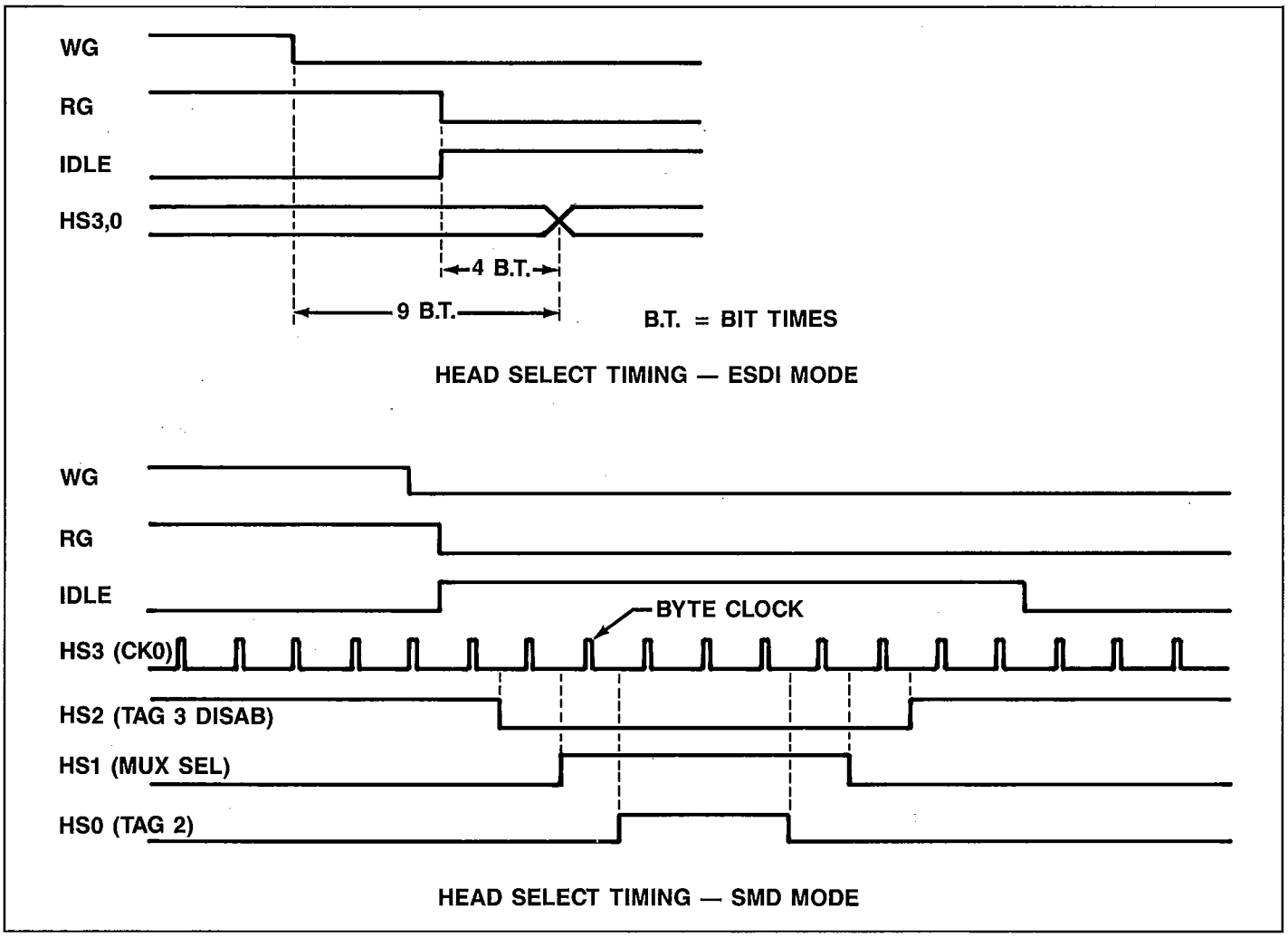

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Figure 24. Head Select Timing