MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

TP1940

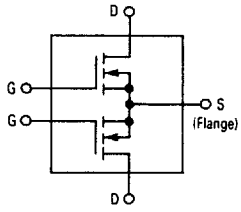
The RF MOSFET Line
RF Power Field-Effect Transistor
N-Channel Enhancement-Mode

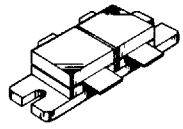
2

The high power, high gain and broadband performance of each device makes possible solid-state transmitters for FM broadcast above 5.0 kW fully solid state.

- Push-Pull Package for Broadband Circuits
- Low Thermal Resistance — 0.35°C/W Max
- Ruggedness Tested at Rated Output Power
- Nitride Passivation

300 W, 50 V, 108 MHz
N-CHANNEL
MOS BROADBAND
RF POWER FET





CASE 375-01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Drain-Gate Voltage	V_{DGO}	125	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain-Current — Continuous	I_D	40	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	500 2.85	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	°C/W

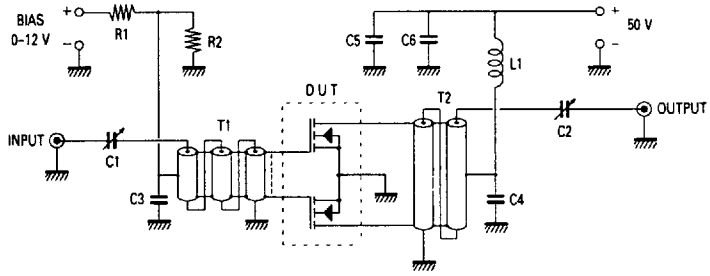
Handling and Packaging MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Each Side)					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 Vdc, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (Each Side)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	—	—	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS (Each Side)					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	225	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	20	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 300 W, I_{DQ} = 500 mA) (f = 108 MHz)	G_{ps}	20	22	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 300 W, f = 108 MHz)	η_D	60	70	—	%
Load Mismatch (V_{DD} = 50 V, P_{out} = 300 W, I_{DQ} = 500 mA) (VSWR 7.1 at all Phase Angles, f = 108 MHz)	ψ	No degradation in Output Power			



R1, R2	Resistor	1.0 kΩ 1/2 Watt	
C1	Capacitor	16 to 100 pF	GMC 70300
C2	Capacitor	95 to 350 pF	GMC 70800
C3, C4	Capacitor	1000 pF	UNELCO
C5	Capacitor	1000 pF	
C6	Capacitor	0.1 μF	
L1	8 Turns enameled Cu Wire (1.7 mm) ID 4 mm length 16 mm		
T1*	9-1 RF Transformer 25 Ω semi-rigid Co-Ax 2.3 mm O.D.		
T2	4-1 RF Transformer 25 Ω semi-rigid Co-Ax 3.2 mm O.D.		
*Loaded with ferrite toroid R.T.C. Type 4C6			
Circuit Board — 1/16", Epoxy Glass			

Figure 1. 108 MHz Test Circuit

2

TYPICAL CHARACTERISTICS

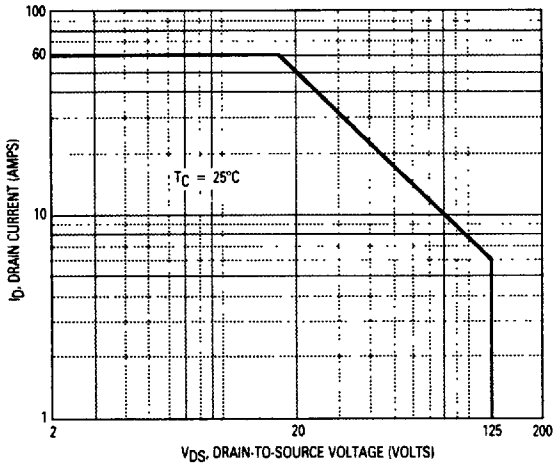


Figure 2. DC Safe Operating Area

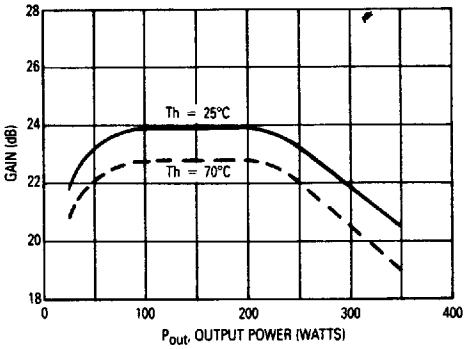


Figure 3. Power Gain versus Output Power

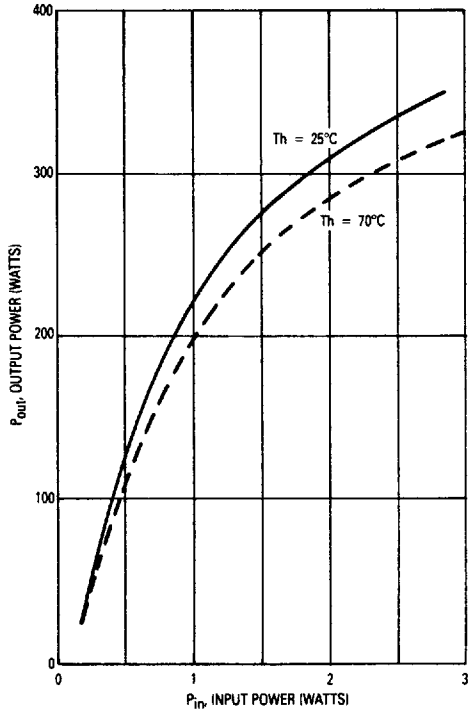


Figure 4. Output Power versus Input Power

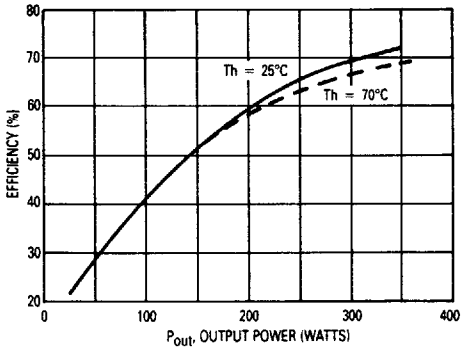


Figure 5. Efficiency versus Output Power

f MHz	Z_{IN} OHMS	Z_{OL}* OHMS
108	1.16 − j2.8	3.6 − j7.3

Note: Input and output impedance values given are measured from gate-to-gate and drain-to-drain respectively.

V_{DS} = 50 V, I_{DQ} = 500 mA, P_{out} = 300 Watts

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

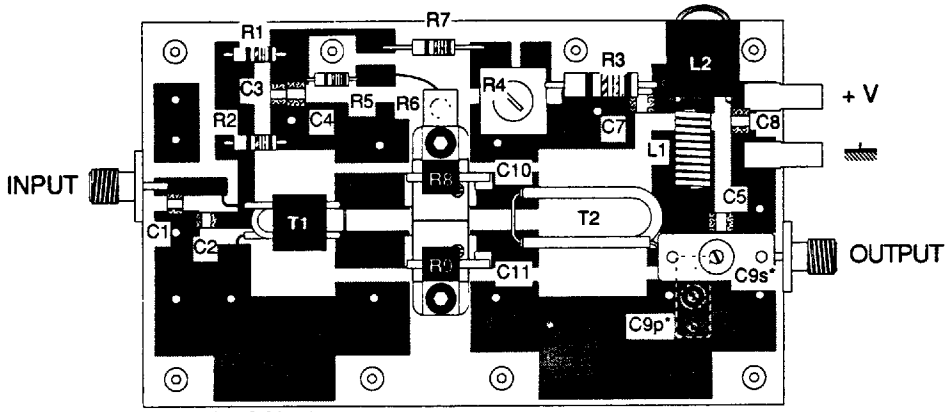
Figure 6. Series Equivalent Input/Output Impedance

P_{out} = 300 W, V_{DD} = 50 V
I_{DQ} = 2 x 200 mA

f (MHz)	OPTION 1 (With C9p and without C9s) G_A dB	η %	OPTION 2 (With C9s and without C9p) G_A dB	η %
108	19.2	62	18.3	65.4
9b	19.7	62.6	19.1	68
88	19.4	64	19.6	66.6

NOTE
1 Bias increases counter clockwise with R4
2 Bias set now for 200 mA at 50 V
3 Copper heat spreader must be mounted to or laid on top of a heatsink with thermal grease interface.
4 Drain efficiency can be increased by
a. Lowering drain idle current (power gain will be reduced by 1–2 dB
b Increasing the value of feedback resistors R8 & R9 This will change the gain versus frequency slope and input VSWR The value of C1 must be made higher
5 In addition of the normal cooling of the units, some air flow is recommended over the top side of the amplifier boards as well

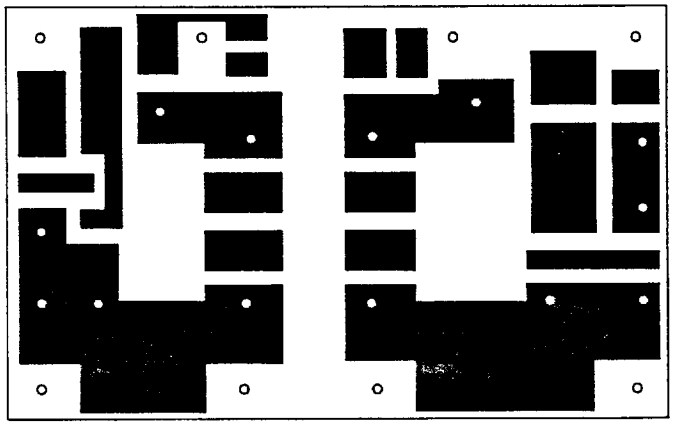
Figure 7. Typical Performance of Test Circuit



SCALE. 1.5 NOTE NOT TO SCALE

(C9s* : Option 1)
(C9p* : Option 2)

Figure 8. Test Circuit — Component Locations



SCALE. 1.1

Figure 9. Test Circuit — Photomaster