

# **Advance Information**

January 1995

## DESCRIPTION

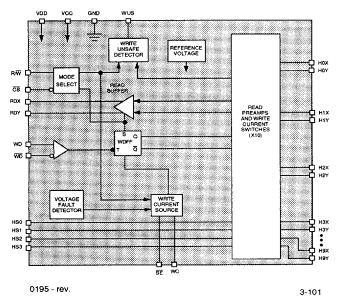
The SSI 32R2100R/2101R are BiCMOS monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, a high performance write driver, write current control, and data protection circuitry for up to 10 channels. The SSI 32R2100R/2101R option provides internal 250Ω damping resistors. Damping resistors are switched in during write mode and switched out during read mode. The SSI32R2100/2101 option does not provide damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance. The device also offers multiple channel "servo bank write" capability to assist in servo writing operations.

The SSI 32R2100R/2101R requires 5V and 12V power supplies. The SSI 32R2100R provides PECL write data input. The SSI 32R2101R provides TTL write data input.

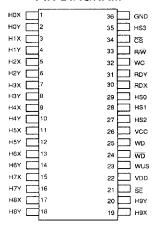
### **FEATURES**

- 5V ±10%, 12V ±10% supply
- Low power
  - PD = 235 mW read mode (Nom)
  - PD = 12 mW idle (Max)
- High Performance:
  - Read mode gain = 150, 250 V/V
  - Input noise =  $0.45 \text{ nV}/\sqrt{\text{Hz}}$  (Nom)
  - Input capacitance = 10 pF (Nom)
  - Write current range = 10-40 mA
  - Max write current rise/fall time = 7 ns (typical head)
  - Head voltage swing = 11 Vpp min
- · Servo bank-write capability
- Self switching damping resistance
- Write unsafe detection
- Power supply fault protection
- Head short to ground protection
- Differential ECL-like (32R2100R) or TTL (32R2101R) write data inputs

# 32R2100R BLOCK DIAGRAM



PIN DIAGRAM



SSI 32R2100R - 36-Lead, 10-Channel SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

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### CIRCUIT OPERATION

The SSI 32R2100R/2101R has the ability to address up to 10 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1, 2 and 3. The TTL inputs  $R/\overline{W}$ ,  $\overline{SE}$  and  $\overline{CS}$  have internal pull-up circuitry to prevent an accidental write condition. HS0, HS1, HS2 and HS3 have internal pulldown circuitry. Internal current limit circuitry will protect the IC from a head short to ground condition in any write mode.

**TABLE 1: Mode Select** 

CS	R/W	SE	Mode
0	0	1	Single Channel Write. See Table 2.
0	0	0	Servo/Bank Write. See Table 2.
0	1	X	Single Channel Read. See Table 2.
1	Х	Х	ldle.

**TABLE 2: Head Select\*** 

Head Selected (SE =1)	Head Selected (servo bank write) (SE = 0)	HS3	HS2	HS1	HS0
0	no heads selected	0	0	0	0
1	H0, H1	0	0	0	1
2	H2, H3	0	0	1	0
3	H0, H1, H2, H3	0	0	1	1
4	no heads selected	0	1	0	0
5	H4, H5	0	1	0	1
6	H6, H7,	0	1	1	0
7	H4, H5, H6, H7	0	1	1	1
8	no heads selected	1	0	0	0
9	H8, H9	1	0	0	1

<sup>\*</sup>Do not use invalid Head Select combinations.

#### WRITE MODE

Taking both  $\overline{\text{CS}}$  and R/W low selects write mode which configures the SSI 32R2100R/2101R as a current switch and activates the Write Unsafe (WUS) detector circuitry. On the 32R2100R, head current is toggled between the X and Y side of the selected head on each low to high transition of WD-WD. On the 32R2101R, head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding Read to Write transition or Idle to Write transition initializes the Write Data Flip-Flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \cdot \frac{Vwc}{Bwc} = \frac{K}{Rwc}$$

where Aw is the write current gain.

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$k, y = \frac{lw}{1 + Rh/Rd}$$

where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In write mode a 250 $\Omega$  damping resistor is switched in across the Hx, Hy ports (32R2100R/2101R only). Unselected heads are at ground potential.

## **SERVO WRITE MODE**

Taking SE low and R/W low activates servo write mode. This mode allows for writing to multiple channels at once, which is useful during servo formatting. In this mode, the bank of channels will be selected according to Table 2.

In order to properly activate servo write mode, the  $\overline{SE}$  pin must be pulled low at least 20 ns before  $R/\overline{W}$  is pulled low. This is a safety feature to prevent glitches on the  $\overline{SE}$  pin from affecting normal write mode.

#### POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode.

#### **HEAD SHORT TO GROUND PROTECTION**

The SSI 32R2100R/2101R provides a head short to ground protection circuit in any mode. In idle or read mode, or for an unselected head in write mode, current out of the head port will not exceed 3 mA. If a selected head in write mode is shorted to ground, the write current generator will turn off, and remain off until the user exits write mode and then returns to write mode.

#### WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in read mode
- Device not selected
- Device in servo write mode
- · No head current
- Open head
- · Head short to ground
- Power supply fault

To prevent false WUS flags, the head inductance and resistance should be less than 1  $\mu H$  and  $50\Omega$ , respectively.

**WDI frequency too low** is detected if the WDI frequency falls below 1 MHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

Device in read mode, Device in servo write mode and Device not selected will flag WUS if  $\overrightarrow{R/W}$  is high, if  $\overrightarrow{SE}$  is low, or  $\overrightarrow{CS}$  is high.

No head current will flag WUS if Rwc > 50 k $\Omega$ .

Head opened will flag WUS if Rh =  $\infty$ . To prevent false WUS flags, the open head detect is disabled when write data frequency is greater than 20 MHz.

**Head short to ground** is described in the preceding paragraph.

Upon entering write mode, WUS is valid within the specified  $R/\overline{W}$  timing.

After the low frequency fault condition is removed, one positive transition of WD-WD (32R2100R), or one negative transition of WDI (32R2101R) is required to clear WUS.

### **READ MODE**

The read mode configures the SSI 32R2100R/2101R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in idle or write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change

when switching from write to read mode. Note also that the write current source is deactivated for both the read and idle mode.

In read mode, unselected heads are at ground potential.

#### IDLE MODE

Taking  $\overline{\text{CS}}$  high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

In idle mode, all heads are at ground potential.

# PIN DESCRIPTION

CONTROL/STATUS († When more than one Read/Write device is used, signals can be wire OR'ed.)

NAME	TYPE	DESCRIPTION
CS	- 1	Chip Select Input. A logical low level enables the device.
R/W†	ı	Read/Write. A logical high level enables read mode. A logical low level enables write mode.
SĒ	ı	Servo Enable. A low level enables servo bank write mode. See Servo Enable section.
HS0, HS1, HS2, HS3	1	Head Select. Decoded address selects one of 10 channels. See Table 2.
WUS†	0	Write Unsafe. A high level indicates an unsafe writing condition. See WUS section.
WC†	ı	Write Current. Sets the write current through the recording head.

### **HEAD TERMINAL CONNECTIONS**

H0X-H9X I X,Y Head Connections H0Y-H9Y	
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### **DATA INPUT/OUTPUT**

WDI†	1	Write Data In. A negative transition of WDI changes the direction of current in the recording head. (32R2101R)
WD, WD†	ı	Differential Write Data In. A positive transition of WD-WD changes the direction of current in the recording head. (32R2100R)
RDX,RDY†	0	Differential Read Data Out. Emitter follower output.

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### **POWER**

VCC	l	5V power supply
VDD	ı	12V power supply
GND	1	Ground

# **ELECTRICAL SPECIFICATIONS**

Current maximums are currents with the highest absolute value.

### **ABSOLUTE MAXIMUM RATINGS**

Operation beyond the maximum ratings may damage the device.

PARAMETER			RATING
DC Supply Voltage		VCC	-0.3 to 6 Vdc
		VDD	-0.3 to 14.0 Vdc
Write Current		lw	100 mA
Digital Input Volt	age	Vin	-0.3 to VCC + 0.3V
Head Port Voltag	Head Port Voltage		-0.3 to VDD + 0.3V
WUS Pin Voltage	9	Vwus	-0.3 to VCC + 2V
Output Current	RDX,RDY	lo	-6 mA
wus		lwus	12 mA
Junction Operating Temperature		Tj	135°
Storage Temperature			-65 to 150°

## **RECOMMENDED OPERATING CONDITIONS**

DC Supply Voltage	VCC	5 ± 10%V
	VDD	12 ± 10%V
Ambient Operating Temperature	Ta	0° < Ta < 75°
Head Inductance	Lh	Lh < 1 μH
Head Resistance, Valid WUS	Rh	Rh < 50 Ω

# **TEST CONDITIONS**

Recommended operating conditions apply.

Write Current, Iw	20 mA
Head Inductance, Lh	1 μΗ
Head Resistance, Rh	30Ω
WD Frequency	5 MHz
WD, WD rise/fall time (32R2100/2100R)	1 ns
WDI rise/fall time (32R2101/2101R)	1 ns

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# **ELECTRICAL SPECIFICATIONS** (continued)

### **POWER DISSIPATION**

Recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Current	Read mode		- 46	75	mA
	Write mode		18 + C 2 lw	26 + 0.2 lw	mA
	Servo write mode 2 heads		21 + 0.4 lw	32 + 0.4 lw	mA
	Servo write mode 4 heads		27 + 0.8 lw	43 + 0.8 lw	mA
	Idle mode		0.3	0.7	mA
VDD Supply Current	Read mode		0.4	0.7	mA
	Write mode		8.5 + 1.1 lw	12 + 1.1 lw	mΑ
	Servo write mode 2 heads		15 + 2.2 lw	20 + 2.2 lw	mA
	Servo write mode 4 heads		31 + 4.4 lw	38 + 4.4 lw	mA
	Idle mode		0.4	0.6	mA
Power Dissipation	Read mode		235	424	mW
	Write mode		192 + 15.2 lw	301 + 15.6 lw	mW
	Servo write mode 2 heads		285 + 28.4 lw	400 + 28.4 lw	mW
	Servo write mode 4 heads	1	507 + 57 lw	671 + 57 lw	mW
	idle mode		6.3	12	mW

<sup>\*</sup>Limit servo mode supplies to  $4.5V \le VCC \le 5V$  and  $10.8V \le VDD \le 12V$ .

### **DIGITAL INPUTS**

Input High Voltage Vih		2			VDC
Input Low Voltage Vil				0.8	VDC
Input High Current lih HSX, CS, R/W, SE, WDI	Vih = 2V			100	μА
Input Low Current IiI HSX, CS, R/W, SE, WDI	Vil = 0.8V	-0.4			mA
WD/WD Input High Voltage Vih		2		Vcc-0.2	VDC
WD/WD Input Low Voltage Vil		Vih-2		Vih-0.3	VDC
WD/WD Input Voltage Difference		0.3		2	٧
WD/WD Input High Current	Vih = Vcc-0.75V		85	110	μΑ
WD/WD Input Low Current	Vih = Vcc-1.75V		70	100	μΑ

### DIGITAL OUTPUTS

İ	WUS Output Low Voltage	Vol	lol = 2 mA max			0.5	VDC
ı	WUS Output High Current	loh	Voh = Vcc	-100	0	100	μΑ

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### WRITE CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	МОМ	MAX	UNIT
Write Current Voltage Vwc			2		V
Write Current Gain Awc	Iw = Aw•Vwc/Rwc		25		mA/mA
Write Current Constant "K"	lw = K/Rwc	46	50	54	V
Differential Head Voltage Swing	Open Head, Iw = 20 mA	11	13		Vp-p
Head Differential Rd	32R2100R/2101R	200	250	300	Ω
Load Resistance	32R2100/2101	1000	1500	2000	Ω
WD Pulse Width	PWH	5			ns
	PWL	5			ns
Unselected Head Voltage				0.1	VDC
Unselected Head Current				0.2	mA
VCC Fault Voltage	lw ≤ 0.2 mA	3.9	4.1	4.3	. V
VDD Fault Voltage	lw ≤ 0.2 mA	8.5	9.3	10	V
Head Current HnX, HnY	VCC, VDD low voltage fault condition	-0.2		0.2	mA

### **SERVO WRITE CHARACTERISTICS**

Write Current Range		10		20	mA
Write Current Matching	Between channels		±10%		

### **READ CHARACTERISTICS**

Test conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

Differential Voltage Gain		Vin = 1 mVpp @1 MHz 32R2100RU/2101RU	120	150	180	V/V
		32R2100RW/2101RW	210	250	290	V/V
Voltage BW -1 dB -3 dB		$ Zs  < 5\Omega$ , Vin = 1 mVpp	45			MHz
			85			MHz
Input Noise Voltage		BW = 20 MHz, Lh = 0, Rh = 0		0.45	0.63	nV/√Hz
Input Noise Current		BW = 20 MHz, Lh = 0, Rh = 0		4	10	pA/√Hz
Differential Input Capacit	ance	Vin = 1 mVpp, f = 5 MHz		10	14	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz 32R2100/2101	500	750	1800	Ω
		32R2100R/2101R	500	750	1800	Ω

## READ CHARACTERISTICS (continued)

Test conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER	CONDITIONS	MIN	МОМ	MAX	UNIT
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2	3		mVp-p
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVp-p @ 5 MHz	50	60		dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCC	50	70		dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVpp	50	60		dB
Output Offset Voltage AV = 150	Lh = 0, Rh = 0	-150		150	mV
AV = 250	Lh = 0, Rh = 0	-250		250	m∨
Single Ended Output Resistance	f = 5 MHz		30		Ω
Output Current Peak to Peak	AC coupled load, RDX to RDY	3	6		mA
RDX, RDY Common Mode Output Voltage			Vcc-2.2	·	VDC

# **SWITCHING CHARACTERISTICS**

Test conditions apply unless otherwise specified.

R/W	Read to Write	R/W to 90% of write current			0.15	μs
	Write to Read	R/W to 90% of 100 mV Read signal envelope			0.20	μs
<u>cs</u>	Unselect to Select	CS to 90% of 100 mV 10 MHz Read signal envelope			0.20	μs
1	Select to Unselect	CS to 10% of write current			0.15	μs
HS0,1, 2, 3 to any Head		To 90% of 100 mV 10 MHz Read signal envelope			0.15	μs
wus	Safe to Unsafe (TD1)	Write mode, loss of WD transitions; Defines max WD period for WUS operation	0.6	2	3.6	μs
	Unsafe to Safe (TD2)	Fault cleared: from first WD transition		0.1	0.2	μs
WDI	Frequency Range	Valid WUS	1		100	MHz
Head (	Current	Lh = 0, Rh = 0				
	WD - WD to lx - ly (TD3)	50% to 50%		3	5	ns
-	WDI to Ix - Iy (TD3)	1.5V to 50%		4	6	ns
Asymmetry		WD has 1 ns rise/fall time			0.5	ns
	Rise/fall Time	10% to 90% points lw = 20 mA, Rh = 0, Lh = 0			3	ns
		lw = 20 mA, Rh = $20\Omega$ , Lh = $600$ nH			7	ns

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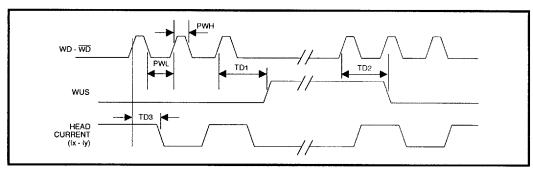


FIGURE 1: Write Mode Timing Diagram (32R2100R)

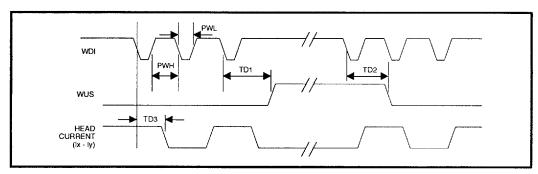


FIGURE 2: Write Mode Timing Diagram (32R2101R)

# PACKAGE PIN DESIGNATIONS

(Top View)

HOX 1	36 GND
H0Y2	35 HS3
H1X 🖂 3	34 🔲 🗟
H1Y4	33 R/W
H2X5	32 🔲 WC
H2Y6	31 RDY
нзх 🔲 7	30 RDX
H3Y = 8	29 HS0
H4X9	28 HS1
H4Y10	27 HS2
H5X 11	26 VCC
H5Y12	25 WD
H6X13	24 WD WD
H6Y14	23 WUS
H7X15	22 VDD
H7Y16	21 SE
H8X17	20 H9Y
H8Y 18	19 H9X

SSI 32R2100R 36-Lead, PECL Input 10-Channel SOM

HO	× 🗀	1	36		GND
H0	Y	2	35		HS3
H12	× 🗀	3	34		N/C
H1	Y	4	33		CS
H2	× 🗀	5	32		R/W
H2	Y	6	31		WC
H3	× 🗀	7	30		RDY
H3	Y	8	29		RDX
H4:	× 🗀	9	28		HS0
H4	Y	10	27		HS1
H5	× 🗀	11	26		HS2
H5	Y	12	25		VCC
H6	×	13	24		WDI
H6	Υ	14	23		wus
H7.	× 🗀	15	22		VDD
H7	Y	16	21		SE
H8:	× 🗀	17	20		H9Y
H8'	Y	18	19		H9X
				1	

SSI 32R2101R 36-Lead, TTL Input 10-Channel SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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