

54S181 Arithmetic Logic Unit

Military Logic Products

4-Bit Arithmetic Logic Unit

Product Specification

FEATURES

- Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations
- Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations
- Full lookahead carry for high-speed arithmetic operation on long words

DESCRIPTION

The 54S181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0 - S_3) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active High or active Low operands. The Function Table list these operations.

ORDERING INFORMATION

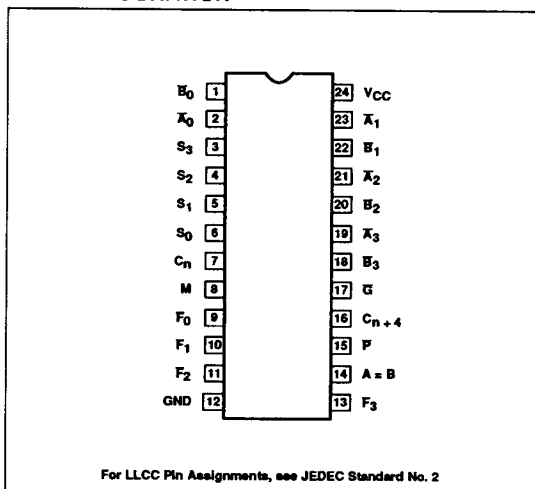
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54S181/BJA
24-Pin Ceramic FlatPack	54S181/BKA
28-Pin Ceramic LLCC	54S181/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

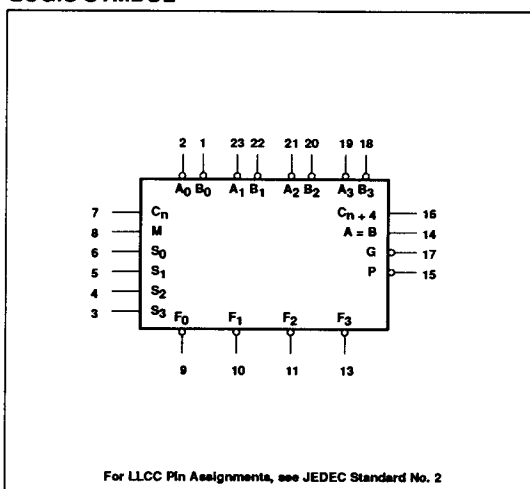
PINS	DESCRIPTION	54S
Mode	Input	1SUL
$\bar{A}$ or $\bar{B}$	Inputs	3SUL
S	Inputs	4SUL
Carry	Input	5SUL
F_0 - $F_3 = B, C_{n+4}$	Outputs	10SUL
$\bar{G}$	Output	10SUL
$\bar{P}$	Output	10SUL

NOTE: Where a 54S Unit Load (SUL) IS 50 μ A I_{IH} and -2.0mA I_{IL} .

PIN CONFIGURATION



LOGIC SYMBOL



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When the Mode Control Input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\bar{P}$ (Carry Propagate) and $\bar{G}$ (Carry Generate). $\bar{P}$ and $\bar{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with

the '182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The $A = B$ output from the device goes High when all four F outputs are High and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The $A = B$ output is open collector and can be wired-AND with other $A = B$ outputs to give a comparison for more than 4 bits. The $A = B$ signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

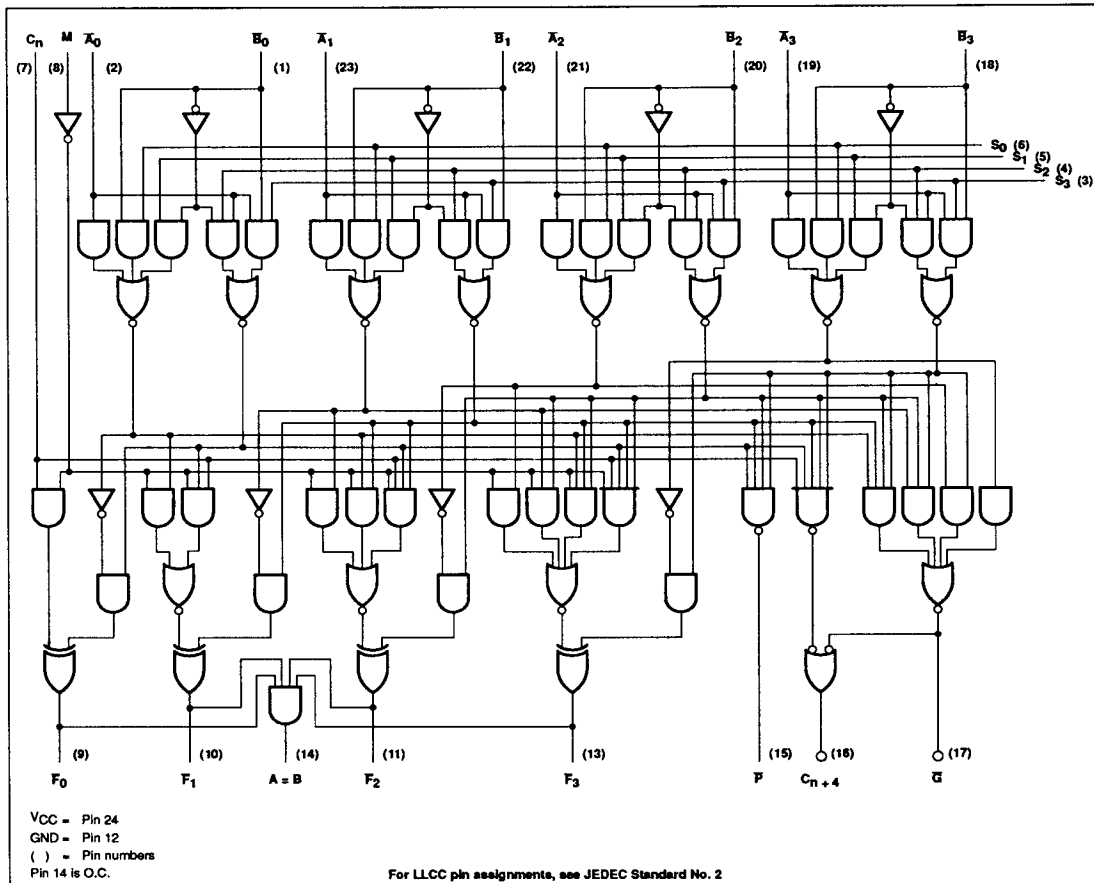
The Function Table lists the arithmetic operations that are performed without a carry in. An

incoming carry adds a one to each operation. Thus, select code LHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is not underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active Low inputs producing active Low outputs or with active High inputs producing active High outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

LOGIC DIAGRAM



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MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S ₃	S ₂	S ₁	S ₀	Logic (M = H)	Arithmetic ** (M = L) (C _n = H)
L	L	L	L	$\bar{A}$	A
L	L	L	H	$\bar{A} + \bar{B}$	A + B
L	L	H	L	$\bar{A}\bar{B}$	A + $\bar{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\bar{A}B$	A plus $\bar{A}B$
L	H	L	H	$\bar{B}$	(A + B) plus $\bar{A}B$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	$\bar{A}B$	$\bar{A}B$ minus 1
H	L	L	L	$\bar{A} + B$	A plus $\bar{A}B$
H	L	L	H	$\bar{A} \oplus \bar{B}$	A plus B
H	L	H	L	B	(A + $\bar{B}$) plus $\bar{A}B$
H	L	H	H	$\bar{A}B$	$\bar{A}B$ minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	$\bar{A} + \bar{B}$	(A + B) plus A
H	H	H	L	A + $\bar{B}$	(A + $\bar{B}$) plus A
H	H	H	H	A	A minus 1

MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S ₃	S ₂	S ₁	S ₀	Logic (M = H)	Arithmetic ** (M = L) (C _n = H)
L	L	L	L	$\bar{A}$	A minus 1
L	L	L	H	$\bar{A}\bar{B}$	$\bar{A}B$ minus 1
L	L	H	L	$\bar{A} + B$	$\bar{A}\bar{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\bar{A} + \bar{B}$	A plus (A + $\bar{B}$)
L	H	L	H	$\bar{B}$	$\bar{A}B$ plus (A + $\bar{B}$)
L	H	H	L	$\bar{A} \oplus \bar{B}$	A minus B minus 1
L	H	H	H	$\bar{A} + \bar{B}$	A + $\bar{B}$
H	L	L	L	$\bar{A}\bar{B}$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	$\bar{A}\bar{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	$\bar{A}\bar{B}$	$\bar{A}B$ plus A
H	H	H	L	$\bar{A}B$	$\bar{A}\bar{B}$ plus A
H	H	H	H	A	A

L = Low voltage

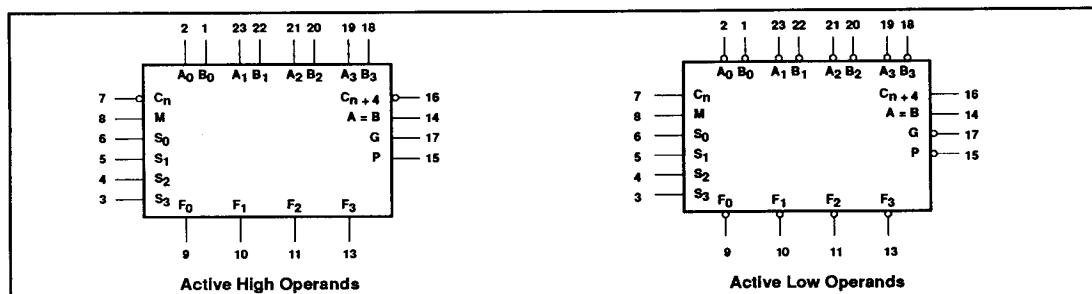
H = High voltage level

* = Each bit is shifted to the next more significant position.

** = Arithmetic operations expressed in 2s complement notation.

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ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	7.0	V
V _I	Input voltage range	-0.5 to +5.5	V
I _I	Input current range	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	V
T _{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			+0.8	V
I _{IK}	Input clamp current			+0.7	V
I _{OH}	High-level output current except A = B			-18	mA
I _{OL}	Low-level output current			-1000	μA
T _A	Operating free-air temperature range	-55		20	mA
				+125	°C

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SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 1$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 1	Apply GND	Apply 1	Apply GND	
t_{PLH} t_{PHL}	$\bar{A}_i$	B_i	None	Remaining $\bar{A}$ and B	C_n	F_i
t_{PLH} t_{PHL}	B_i	$\bar{A}_i$	None	Remaining $\bar{A}$ and B	C_n	F_i
t_{PLH} t_{PHL}	$\bar{A}_i$	B_i	None	None	Remaining $\bar{A}$ and B , C_n	P
t_{PLH} t_{PHL}	B_i	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and B , C_n	P
t_{PLH} t_{PHL}	$\bar{A}_i$	None	B_i	Remaining B	Remaining $\bar{A}$, C_n	G
t_{PLH} t_{PHL}	B_i	None	$\bar{A}_i$	Remaining B	Remaining $\bar{A}$, C_n	G
t_{PLH} t_{PHL}	$\bar{A}_i$	None	B_i	Remaining B	Remaining $\bar{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	B_i	None	$\bar{A}_i$	Remaining B	Remaining $\bar{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\bar{A}$	All B	Any F or $C_n + 4$

NOTE:

1. $2.7V \leq HI \leq V_{CC}$

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_0 = S_3 = 1$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 1	Apply GND	Apply 1	Apply GND	
t_{PLH} t_{PHL}	$\bar{A}_i$	None	B_i	Remaining $\bar{A}$	Remaining B , C_n	F_i
t_{PLH} t_{PHL}	B_i	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining B , C_n	F_i
t_{PLH} t_{PHL}	$\bar{A}_i$	None	B_i	None	Remaining $\bar{A}$ and B , C_n	P
t_{PLH} t_{PHL}	B_i	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and B , C_n	P
t_{PLH} t_{PHL}	$\bar{A}_i$	B_i	None	None	Remaining $\bar{A}$ and B , C_n	G
t_{PLH} t_{PHL}	B_i	None	$\bar{A}_i$	None	Remaining $\bar{A}$ and B , C_n	G
t_{PLH} t_{PHL}	$\bar{A}_i$	None	B_i	Remaining $\bar{A}$	Remaining B , C_n	$A = B$
t_{PLH} t_{PHL}	B_i	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining B , C_n	$A = B$
t_{PLH} t_{PHL}	$\bar{A}_i$	B_i	None	None	Remaining $\bar{A}$ and B , C_n	$C_n + 4$
t_{PLH} t_{PHL}	B_i	None	$\bar{A}_i$	None	Remaining $\bar{A}$ and B , C_n	$C_n + 4$
t_{PHL} t_{PHL}	C_n	None	None	All $\bar{A}$ and B	None	Any F or $C_n + 4$

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LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 1	Apply GND	Apply 1	Apply GND		
t_{PLH} t_{PHL}	$\bar{A}_i$	B_i	None	None	Remaining $\bar{A}$ and B, C_n	F_i	$S_1 = S_2 = M = 1$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	B_i	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and B, C_n	F_i	$S_1 = S_2 = M = 1$ $S_0 = S_3 = 0V$

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹		LIMITS			UNIT
				Min	Typ ²	Max	
V_{OH}	High-level output voltage	$V_{CC} = \text{Min},$ $V_{IH} = \text{Min},$ $V_{IL} = \text{Max},$ $I_{OH} = \text{Max}$	Any output except $A = B$	2.5	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{Min}, V_{IH} = \text{Min}, V_{IL} = \text{Max},$ $I_{OH} = \text{Max}$	+125°			0.5 0.45	V V
V_{IK}	Input clamp voltage	$V_{CC} = \text{Min}, I_I = I_{IK}$				-1.2	V
I_{IH2}	Input current at maximum input voltage	$V_{CC} = \text{Max},$ $V_I = 5.5V$	Mode input			1.0	mA
			$\bar{A}$ or $\bar{B}$ inputs			1.0	mA
			S inputs			1.0	mA
			Carry input			1.0	mA
I_{IH1}	High-level input current	$V_{CC} = \text{Max},$ $V_I = 2.7V$	Mode input			50	μA
			$\bar{A}$ or $\bar{B}$ inputs			150	μA
			S inputs			200	μA
			Carry input			250	μA
I_{IL}	Low-level input current	$V_{CC} = \text{Max},$ $V_I = 0.5V$	Mode input			-2	mA
			$\bar{A}$ or $\bar{B}$ inputs			-6	mA
			S inputs			-8	mA
			Carry input			-10	mA
I_{OH}	High-level output current	$V_{IH} = \text{Min}, V_I = \text{Max}, V_{OH} = 5.5V$	$A = B$ only			250	μA
I_{OS}	Short-circuit output current ⁴	$V_{CC} = \text{Max}$	Any output except $A = B$	-40		-100	mA
I_{CC}	Supply current ⁵ (total)	$V_{CC} = \text{Max}$	Note 5a		120	220	mA
			Note 5b		120	220	mA

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 15\text{pF}$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	$M = 0\text{V}$, Sum or Diff Mode see Waveform 2 and Tables I & II		10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to F outputs	$M = 0\text{V}$, Sum or Diff Mode see Waveform 2 and Tables I & II		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to G output	$M = S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to G output	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to P output	$M = S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to P output	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i inputs to F_i outputs	$M = S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		16.5 16.5	ns ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i inputs to F_i outputs	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		20 22	ns ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i inputs to F_i outputs	$M = 4.5\text{V}$, Logic Mode see Waveform 2 and Table III		20 22	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to C_{n+4} output	$M = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$, $S_1 = S_2 = 0\text{V}$ Sum Mode, see Waveform 1 and Table I		18.5 18.5	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to C_{n+4} outputs	$M = 0\text{V}$, $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 4 and Table II		23 23	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to $A = B$ output	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		23 30	ns ns

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}^6$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C _L = 50pF		
			Min	Max	
t _{PLH} t _{PHL}	Propagation delay C _n to C _{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		13.0 13.0	ns ns
t _{PLH} t _{PHL}	Propagation delay C _n to F outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		14.0 14.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A or B inputs to G output	M = S ₁ = S ₂ = 0V, S ₀ = S ₃ = 4.5V Sum Mode, see Waveform 2 and Table I		14.0 14.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A or B inputs to G output	M = S ₀ = S ₃ = 0V, S ₁ = S ₂ = 4.5V Diff Mode, see Waveform 3 and Table II		18.0 18.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A or B inputs to P output	M = S ₁ = S ₂ = 0V, S ₀ = S ₃ = 4.5V Sum Mode, see Waveform 2 and Table I		14.0 14.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A or B inputs to P output	M = S ₀ = S ₃ = 0V, S ₁ = S ₂ = 4.5V Diff Mode, see Waveform 3 and Table II		18.0 18.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A _i or B _i inputs to F _i outputs	M = S ₁ = S ₂ = 0V, S ₀ = S ₃ = 4.5V Sum Mode, see Waveform 2 and Table I		20.0 20.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A _i or B _i inputs to F _i outputs	M = S ₀ = S ₃ = 0V, S ₁ = S ₂ = 4.5V Diff Mode, see Waveform 3 and Table II		23.0 25.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A _i or B _i inputs to F _i outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		24.0 26.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A or B inputs to C _{n+4} output	M = 0V, S ₀ = S ₃ = 4.5V, S ₁ = S ₂ = 0V Sum Mode, see Waveform 1 and Table I		23.0 23.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A or B inputs to C _{n+4} outputs	M = 0V, S ₀ = S ₃ = 0V, S ₁ = S ₂ = 4.5V Diff Mode, see Waveform 4 and Table II		27.0 26.0	ns ns
t _{PLH} t _{PHL}	Propagation delay A or B inputs to A = B output	M = S ₀ = S ₃ = 0V, S ₁ = S ₂ = 4.5V Diff Mode, see Waveform 3 and Table II		27.0 33	ns ns

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AC ELECTRICAL CHARACTERISTICS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^6$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50\text{pF}$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		14.5 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to F outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		16.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to G output	M = $S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		16.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to G output	M = $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		20.0 20.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to F output	M = $S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		16.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to P output	M = $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		20.0 20.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A _i or B _i inputs to F _i outputs	M = $S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		23.0 23.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A _i or B _i inputs to F _i outputs	M = $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		26.0 28.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A _i or B _i inputs to F _i outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		26.0 28.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to C_{n+4} output	M = 0V, $S_0 = S_3 = 4.5\text{V}$, $S_1 = S_2 = 0\text{V}$ Sum Mode, see Waveform 1 and Table I		25.0 25.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to C_{n+4} outputs	M = 0V, $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 4 and Table II		29.0 29.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B inputs to A = B output	M = $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		29.0 36.0	ns ns

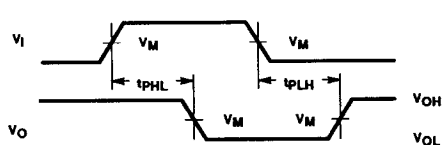
NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with the following conditions:
 - S_0 through S_3 , M, and A inputs are $\geq 4.0\text{V}$, other inputs grounded, all outputs open.
 - S_0 through S_3 and M inputs are $\geq 4.0\text{V}$, other inputs grounded, all outputs open.
- These parameters are guaranteed, but not tested.

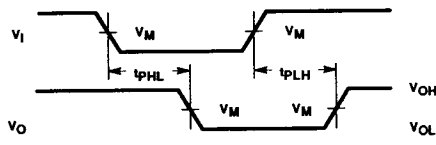
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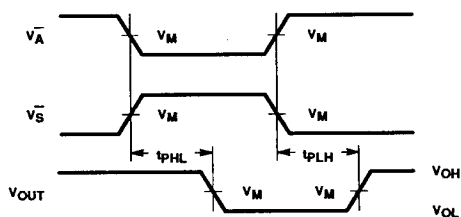
AC WAVEFORMS



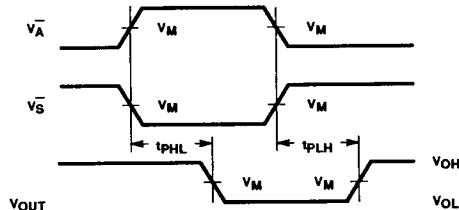
Waveform 1



Waveform 2



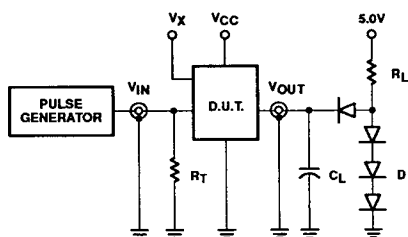
Waveform 3



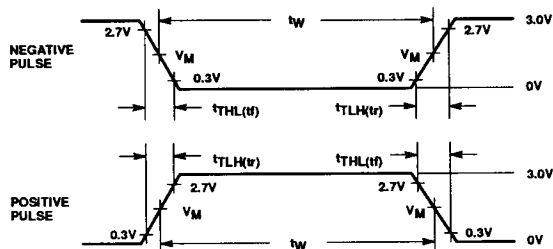
Waveform 4

NOTE: $V_M = 1.5V$

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280k Ω	1.5V	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$

DEFINITIONS:

- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- V_X = Unlocked pins must be held at $\leq 0.8V$, $\geq 2.7V$ or open per Function Table.