74F651A Octal transceiver/register, inverting (3-State)
74F652A Octal transceiver/register, non-inverting (3-State)

FEATURES

- Combines 74F245 and two 74F374 type functions in one chip
- High impedance base inputs for reduced loading (70µA in high and low states)
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- 3-State outputs
- Industrial temperature range available (–40°C to +85°C) for 74F652A

DESCRIPTION

The 74F651A and 74F652A transceivers/registers consist of bus transceiver circuits with 3–State outputs, D–type flip–flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes high. Output enable (OEAB, $\overline{OEBA}$) and select (SAB, SBA) pins are provided for bus management.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F651/74F652	110MHz	140mA
74F651A/74F652A	175MHz	110mA

ORDERING INFORMATION

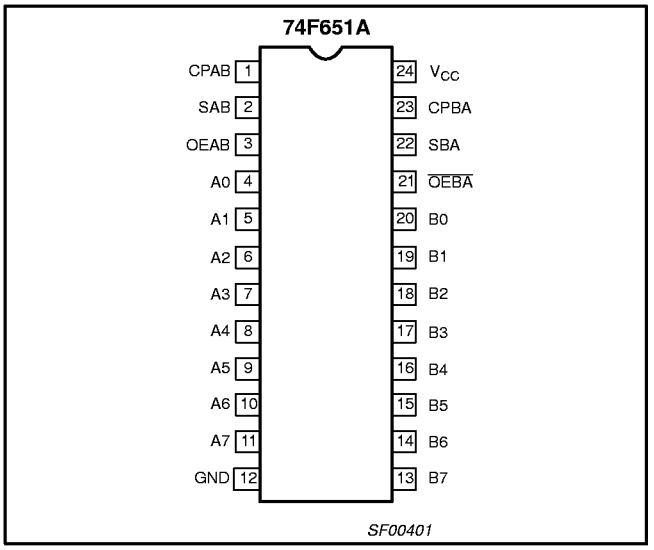
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
24–pin plastic slim DIP (300mil)	N74F651AN, N74F652AN	I74F652AN	SOT222-1
24–pin plastic SOL	N74F651AD, N74F652AD	I74F652AD	SOT137-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

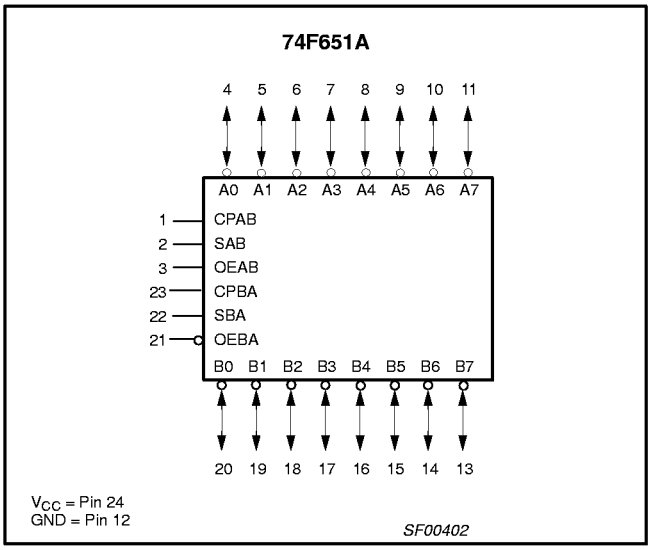
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7, B0 – B7	A, B inputs	3.5/0.116	70µA/70µA
CPAB, CPBA	A–to–B, B–to–A clock inputs	1.0/0.033	20µA/20µA
SAB, SBA	A–to–B, B–to–A select inputs	1.0/0.033	20µA/20µA
OEAB, $\overline{OEBA}$	A–to–B, B–to–A output enable inputs	1.0/0.033	20µA/20µA
A0 – A7, B0 – B7	A, B outputs for N74F651, N74F652	750/106.7	15mA/64mA
A0 – A7, B0 – B7	A, B outputs for N74F651A, N74F652A	750/80	15mA/48mA
A0 – A7, B0 – B7	A, B outputs for I74F652A	750/60	15mA/36mA

Note to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

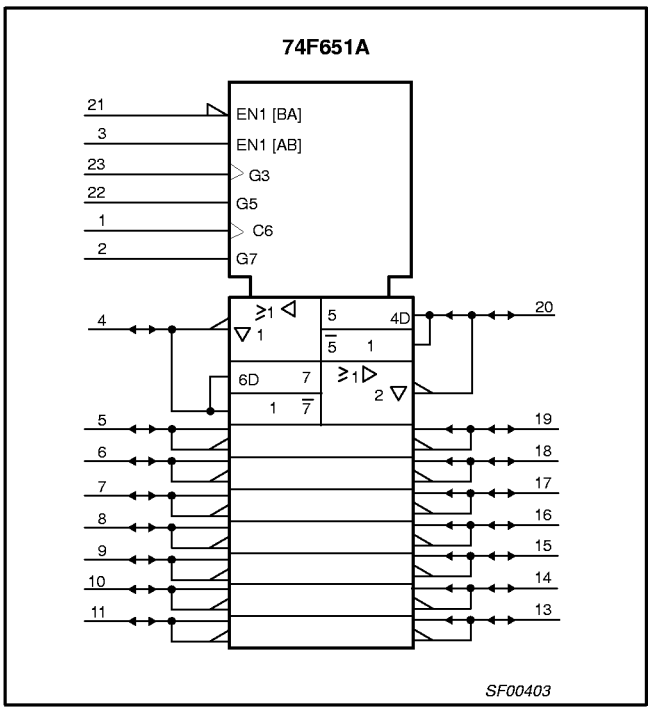
PIN CONFIGURATION



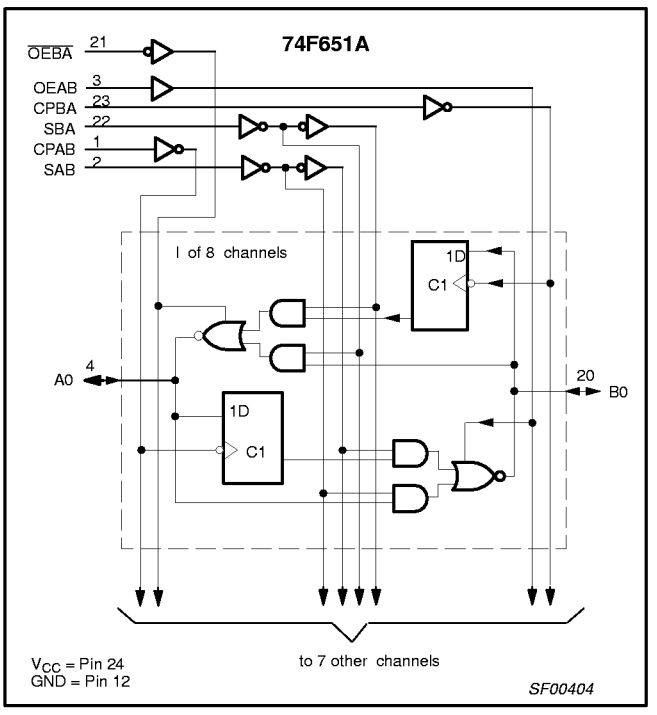
LOGIC SYMBOL



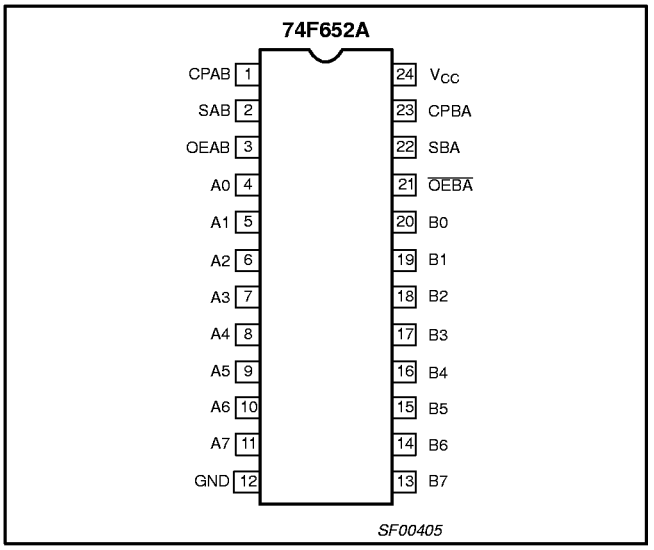
IEC/IEEE SYMBOL



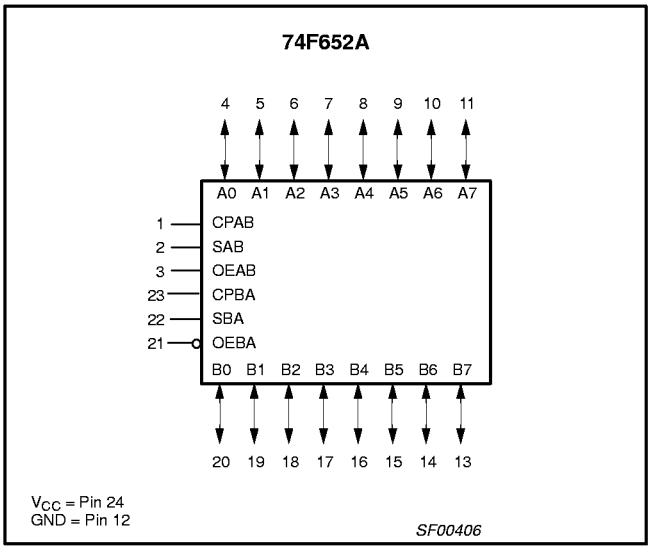
LOGIC DIAGRAM



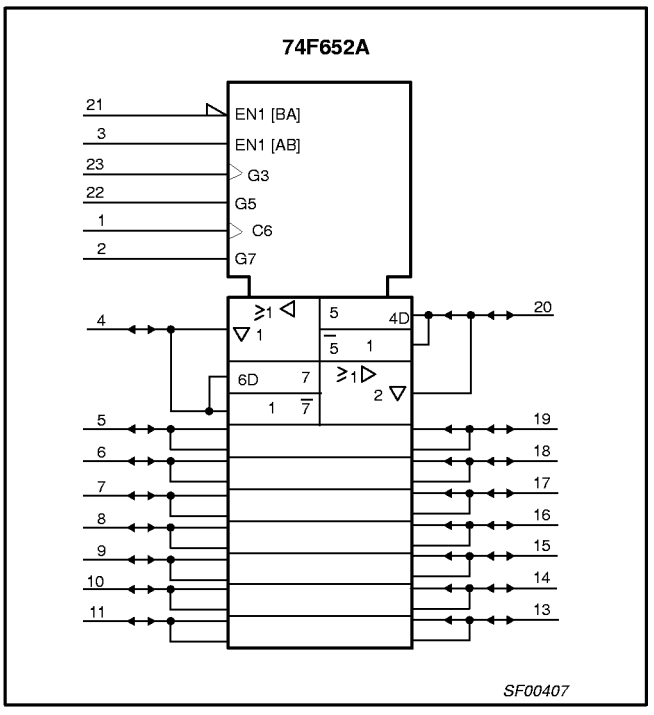
PIN CONFIGURATION



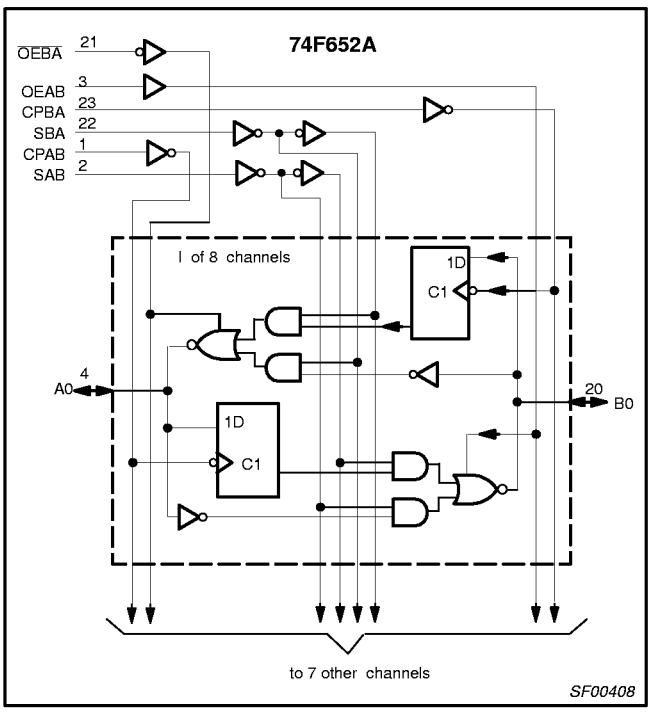
LOGIC SYMBOL



IEC/IEEE SYMBOL

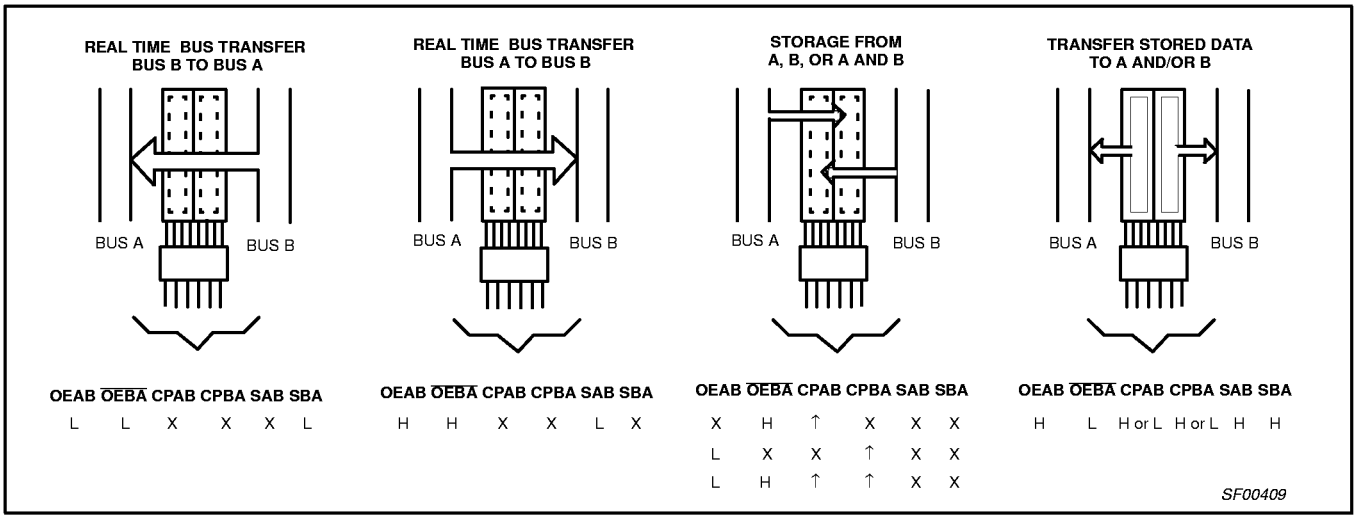


LOGIC DIAGRAM



The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74F651A and 74F652A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

BUS MANAGEMENT FUNCTIONS



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	74F651A	74F652A
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, hold B	Store A hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, store B	Hold A, store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{B}$ data to A bus	Stored B data to A bus

Notes to function table

1. H = High-voltage level
2. L = Low-voltage level
3. * = The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition of the clock.
4. ↑ = Low-to-high clock transition
5. X = Don't care

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		72	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current	Commercial range			48	mA
		Industrial range (74F652A only)			36	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range (74F652A only)	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA, SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA, SAB, SBA	V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH} + I_{IH}	Off-state output current, high-level voltage applied	A0–A7, B0–B7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied	A0–A7, B0–B7	V_{CC} = MAX, V_O = 0.5V					–70	µA
I_O	Output current[3]		V_{CC} = MAX, V_0 = 2.25V			–60		–160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				105	145	mA
		I_{CCL}	V_{CC} = MAX				115	165	mA
		I_{CCZ}	V_{CC} = MAX				115	160	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. I_O is tested under conditions that produce current approximately one half of the true short–circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS FOR 74F651A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	155	175		140		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	4.5 5.5	7.0 7.5	10.0 10.5	4.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Bn or An	Waveform 2, 3	2.5 4.0	4.5 6.5	7.5 9.0	2.0 4.0	8.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.0 5.0	7.0 7.0	10.0 10.0	3.5 4.5	12.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	3.0 3.5	5.0 6.0	8.0 8.5	2.5 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	1.5 2.5	4.0 6.0	7.0 8.5	1.0 2.0	7.5 9.0	ns

AC SETUP REQUIREMENTS FOR 74F651A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.5 3.5			4.5 4.0		ns

Note to AC setup requirements for 74F651A:

1. Setup time is to protect against surge current caused by enabling 16 outputs (48mA per output) simultaneously.

AC ELECTRICAL CHARACTERISTICS FOR 74F652A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	155	175		140		140		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.0	7.5 7.0	10.0 10.0	4.5 4.5	11.5 10.5	4.5 4.5	11.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Bn or An	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 8.5	3.5 2.5	10.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.5 4.0	7.0 8.0	10.0 10.0	4.0 4.0	11.0 11.5	4.0 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time[1] OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	3.0 3.5	5.0 6.0	8.0 8.5	2.5 3.0	8.5 9.0	2.5 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	1.5 2.5	4.0 6.0	7.0 8.5	1.0 2.0	7.5 9.0	1.0 2.0	7.5 9.0	ns

AC SETUP REQUIREMENTS FOR 74F652A

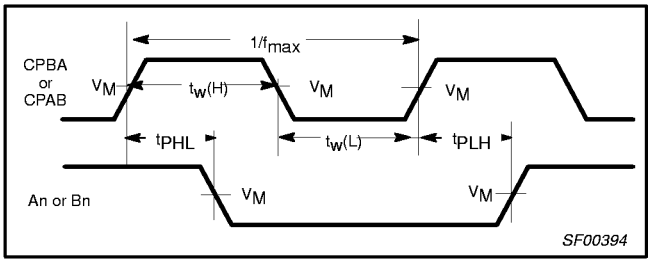
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		4.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.0 3.5			4.5 4.0		4.5 4.0		ns

Note to AC setup requirements for 74F652A

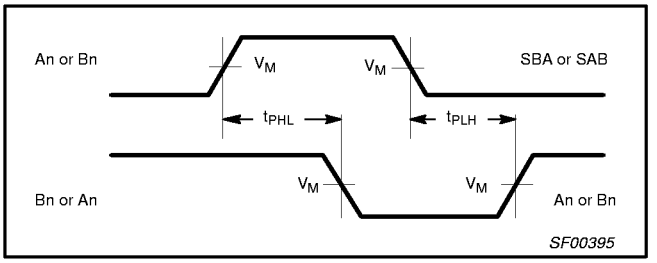
1. Setup time is to protect against surge current caused by enabling 16 outputs (48mA per output) simultaneously.

AC WAVEFORMS

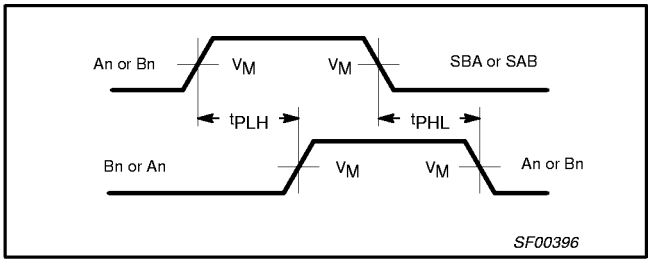
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



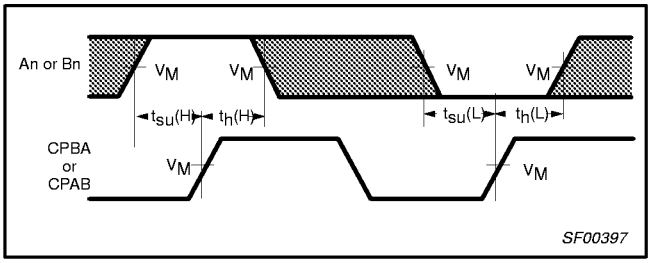
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



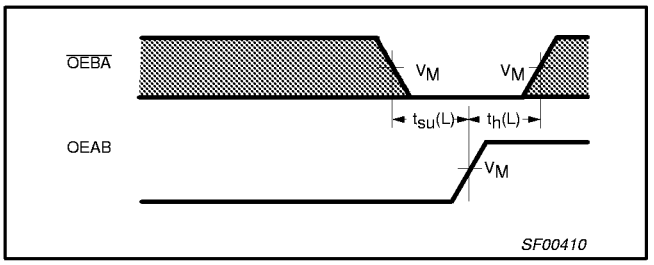
Waveform 2. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



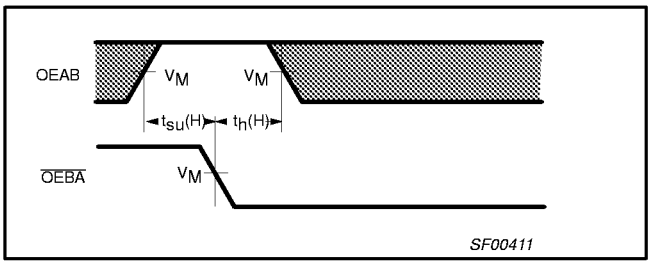
Waveform 3. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



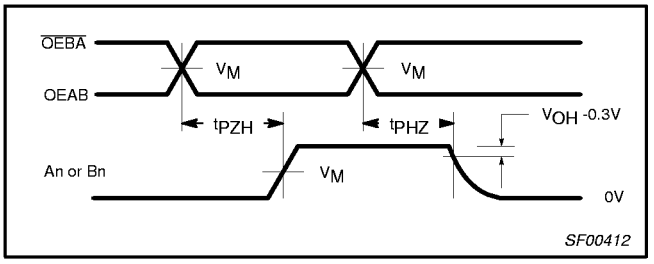
Waveform 4. Data setup time and hold times



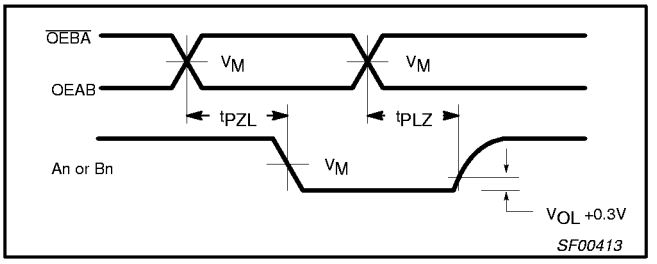
Waveform 5. $\overline{OEBA}$ to OEAB setup time and hold times



Waveform 6. OEAB to $\overline{OEBA}$ setup time and hold times

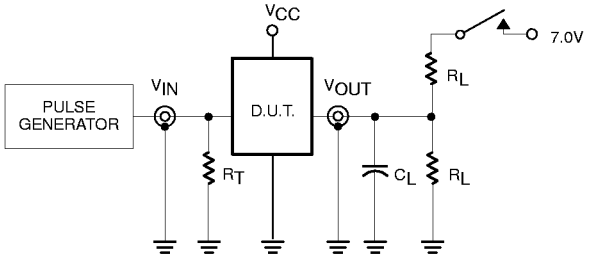


Waveform 7. 3-State output enable time to high level and output disable time from high level



Waveform 8. 3-State output enable time to low level and output disable time from low level

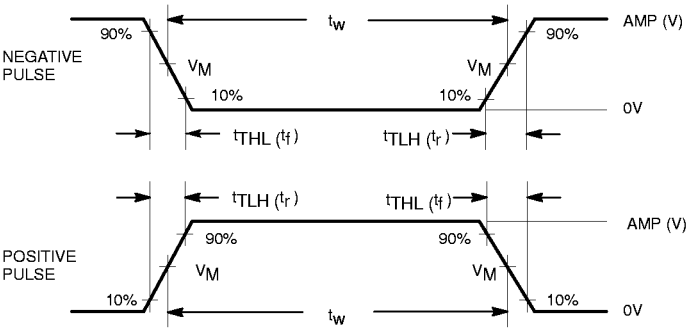
TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

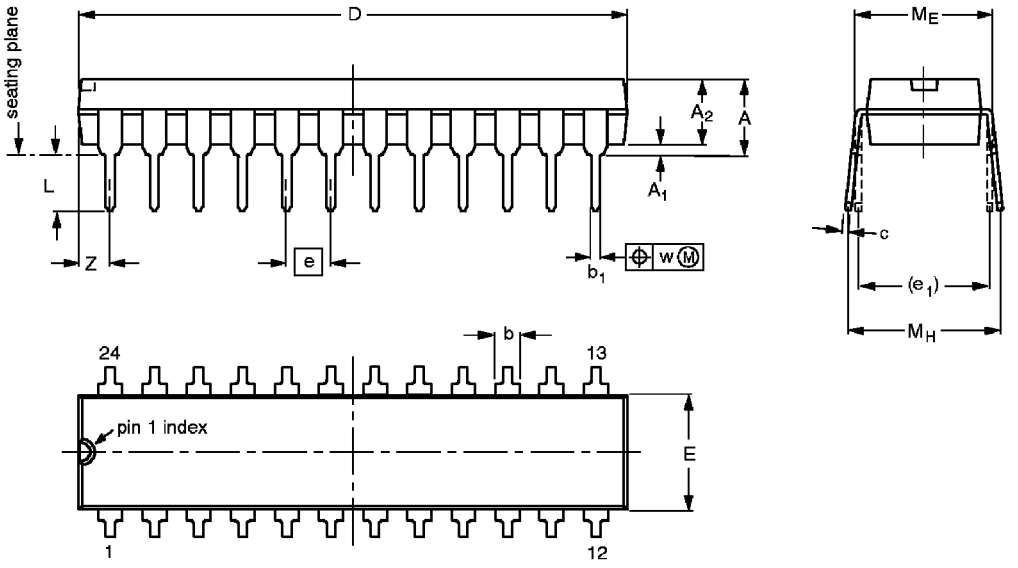
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

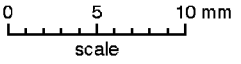
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

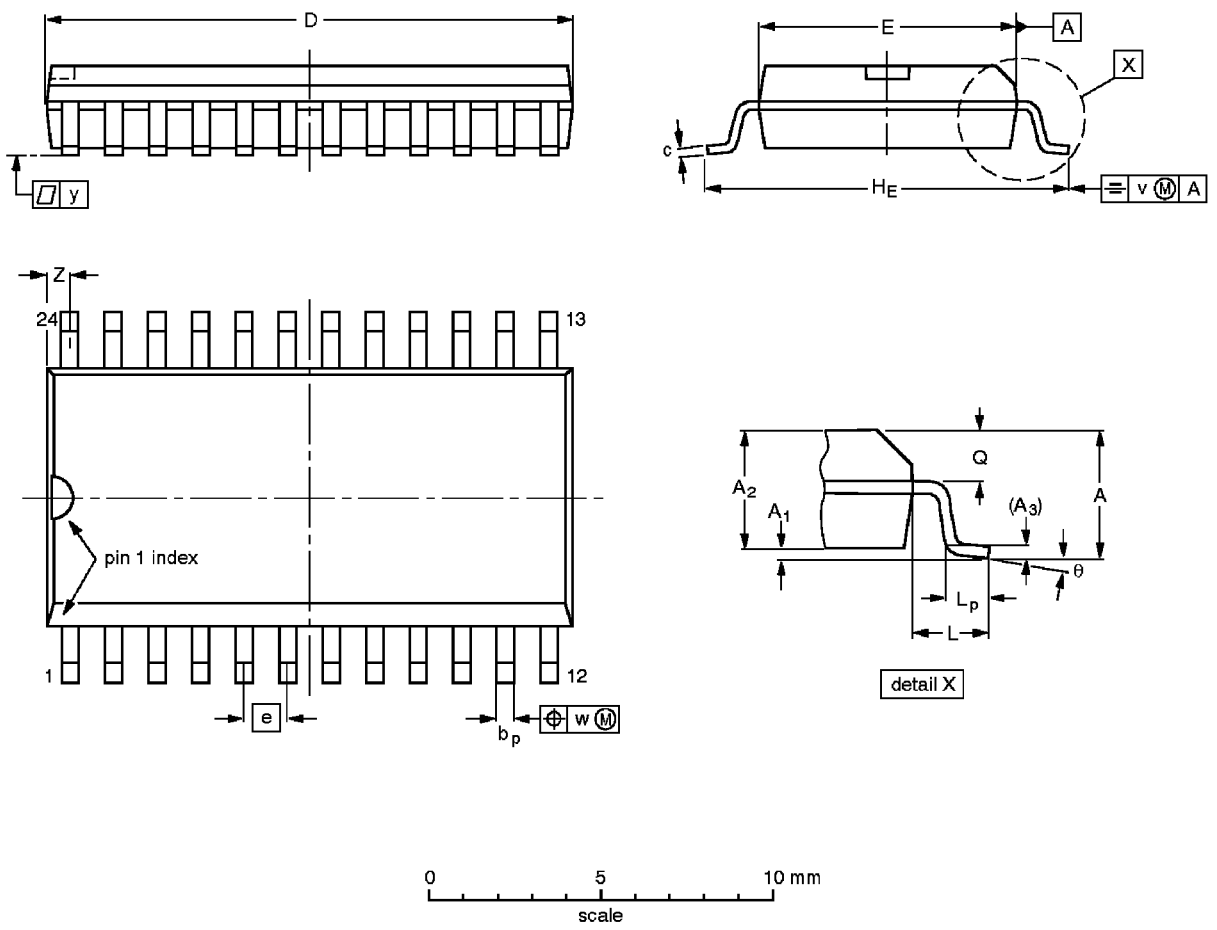
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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