SRAM

1 MEG x 1 SRAM

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-92316
- MIL-STD-883

FEATURES

- High speed: 15, 20, 25, 35 and 45ns
- Battery Backup: 2V data retention
- Low power standby
- High-performance, low-power, CMOS double-metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and output are TTL compatible

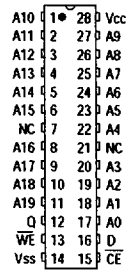
OPTIONS

	MARKING
• Timing	
15ns access (Contact factory)	-15
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
55ns access	-55*
70ns access	-70*
• Packages	
Ceramic DIP (400 mil)	C No. 109
Ceramic Flat Pack	F No. 303
Ceramic LCC	EC No. 207
Ceramic SOJ	DCJ No. 501
• 2V data retention, low power standby	L
• Radiation Tolerant(EPI)	E

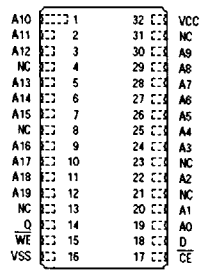
*Electrical characteristics identical to those provided for the 45ns access devices.

PIN ASSIGNMENT (Top View)

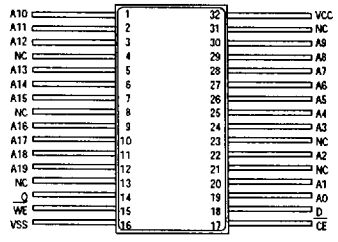
28-Pin DIP 400 MIL



32-Pin LCC 32-Pin SOJ



32-Pin Flat Pack



GENERAL DESCRIPTION

The Austin Semiconductor SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Austin Semiconductor SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

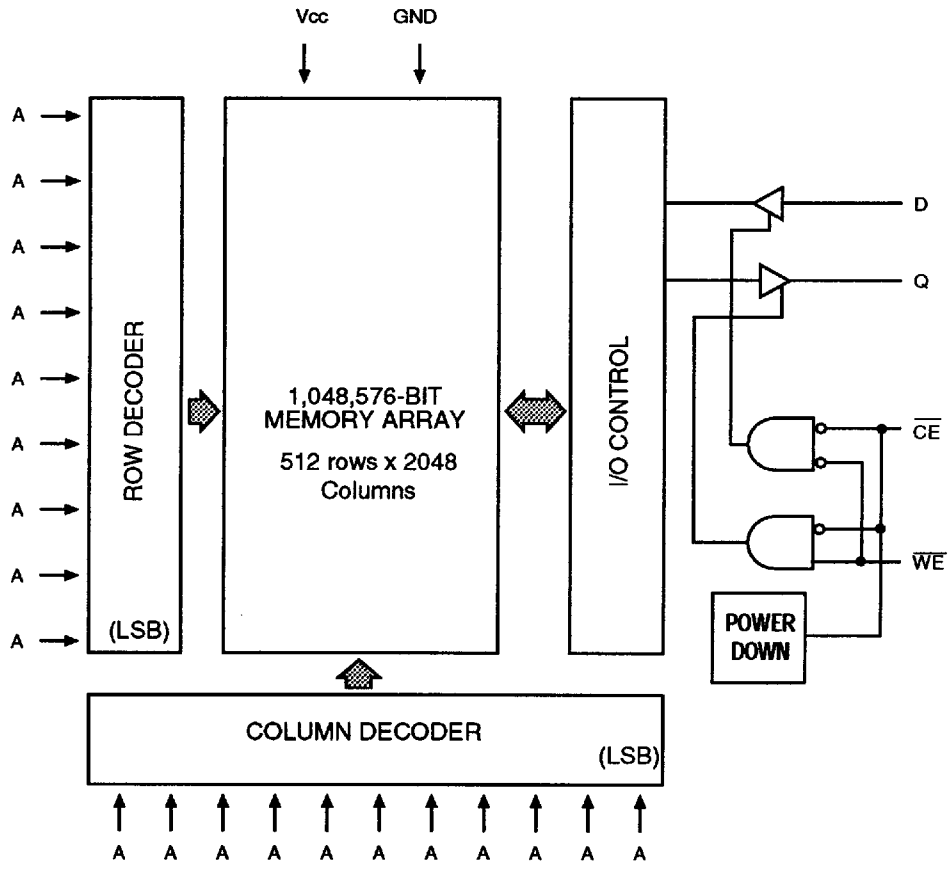
For flexibility in high-speed memory applications, Austin Semiconductor offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

The "L" version provides an approximate 50 percent reduction in CMOS standby current (I_{SBC2}) over the standard version.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Input Relative to Vss ..... -.5V to +7V
Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Voltage Applied to Q ..... -.5V to +6V
Storage Temperature ..... -65°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 20mA
Lead Temperature (soldering 10 seconds) ..... +260°C
Junction Temperature ..... +175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+0.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	$I_{OH} = -4.0mA$	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0mA$	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX -15	MAX -20	MAX -25	MAX -35	MAX -45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; Vcc = MAX f = MAX = 1/ ^tRC (MIN) Output Open	Icc	170	125	120	115	110	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; Vcc = MAX f = MAX = 1/ ^tRC (MIN) Output Open	I_{SBT1}	65	50	45	40	35	mA	
	$\overline{CE} \ge V_{IH}$, All Other Inputs $\le V_{IL}$ or $\ge V_{IH}$, Vcc = MAX f = 0 Hz	I_{SBT2}	25	25	25	25	25	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; Vcc = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0 Hz	I_{SBC2}	10	10	10	10	10	mA	
	"L" Version Only	I_{SBC2}	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A3-A5, A15-A17)	$T_A = 25°C$, f = 1MHz Vcc = 5V	C_I		10	pF	4
Output Capacitance (Q)		C_O		8	pF	4
Input Capacitance (All Other Inputs)		C_I		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5)(-55°C ≤ T_A ≤ +125°C; Vcc = 5V ± 10%)

DESCRIPTION		-15		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	15		20		25		35		45		ns	
Address access time	t_{AA}		15		20		25		35		45	ns	
Chip Enable access time	t_{ACE}		15		20		25		35		45	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		3		3		3		ns	4, 6, 7
Chip disable to output in High-Z	t_{HZCE}		6		8		10		15		15	ns	4, 6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		ns	4
Chip disable to power-down time	t_{PD}		15		20		25		35		45	ns	4
WRITE Cycle													
WRITE cycle time	t_{WC}	15		20		25		35		45		ns	
Chip Enable to end of write	t_{CW}	12		15		16		20		25		ns	
Address valid to end of write	t_{AW}	12		15		16		20		25		ns	
Address setup time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	1		1		1		1		1		ns	
WRITE pulse width	t_{WP}	12		15		16		20		25		ns	
Data setup time	t_{DS}	7		8		10		13		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	3		3		3		3		3		ns	7
Write Enable to output in High-Z	t_{HZWE}	0	7	0	9	0	10	0	13	0	13	ns	4, 6, 7

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AC TEST CONDITIONS

Input pulse levels	Vss to 3V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

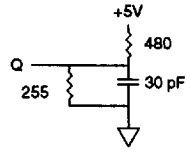


Fig. 1 OUTPUT LOAD EQUIVALENT

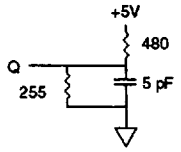


Fig. 2 OUTPUT LOAD EQUIVALENT

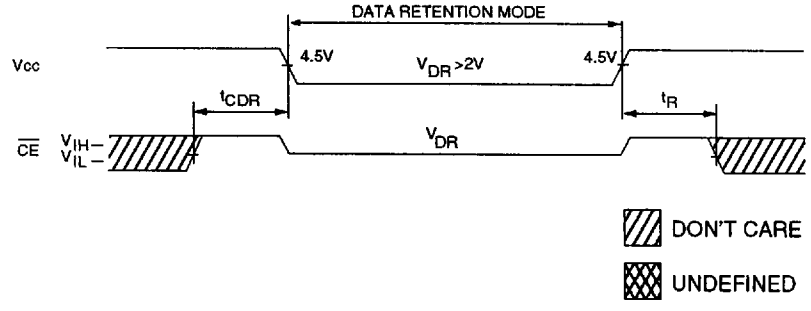
NOTES

1. All voltages referenced to Vss (GND).
2. -2V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the output unloaded, and $f = \frac{1}{{}^tRC\ (MIN)}$ Hz.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tLZCE$, ${}^tLZWE$, ${}^tHZCE$ and ${}^tHZWE$ are specified with CL = 5 pF as in Fig. 2. Transition is measured ±200mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable is held in its active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ${}^tRC$ = READ cycle time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE} \geq (Vcc - 0.2V)$ $V_{IN} \geq (Vcc - 0.2V)$ or $\leq 0.2V$	Vcc = 2V	I_{CCDR}			1.0	mA	
		Vcc = 3V				2.0	mA	
Chip Deselect to Data Retention Time			${}^tCDR$	0		—	ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

LOW Vcc DATA RETENTION WAVEFORM



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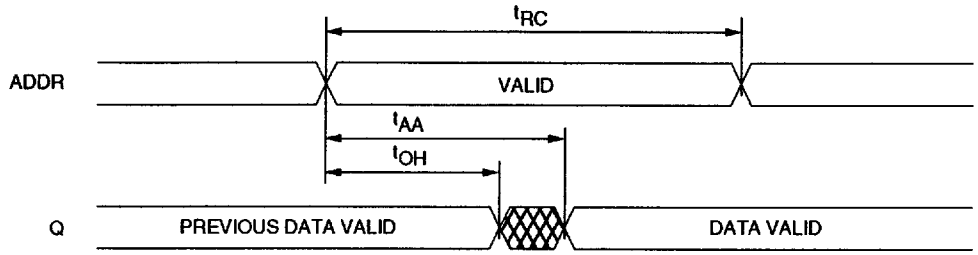
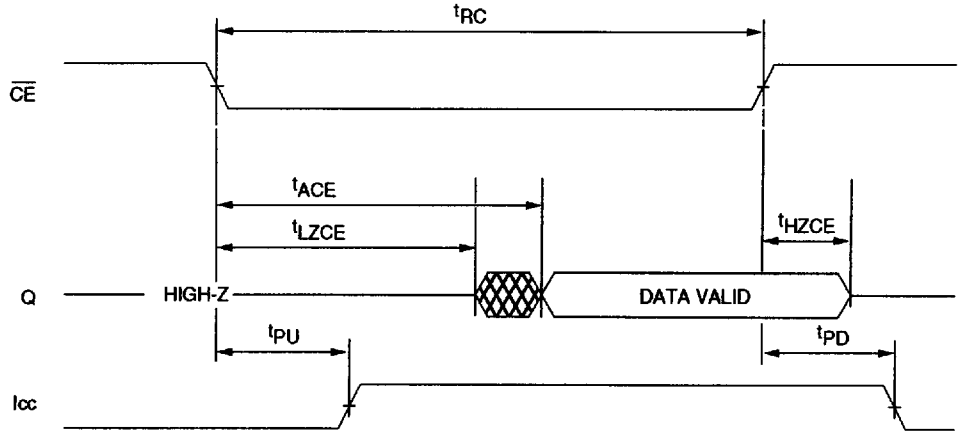
READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]

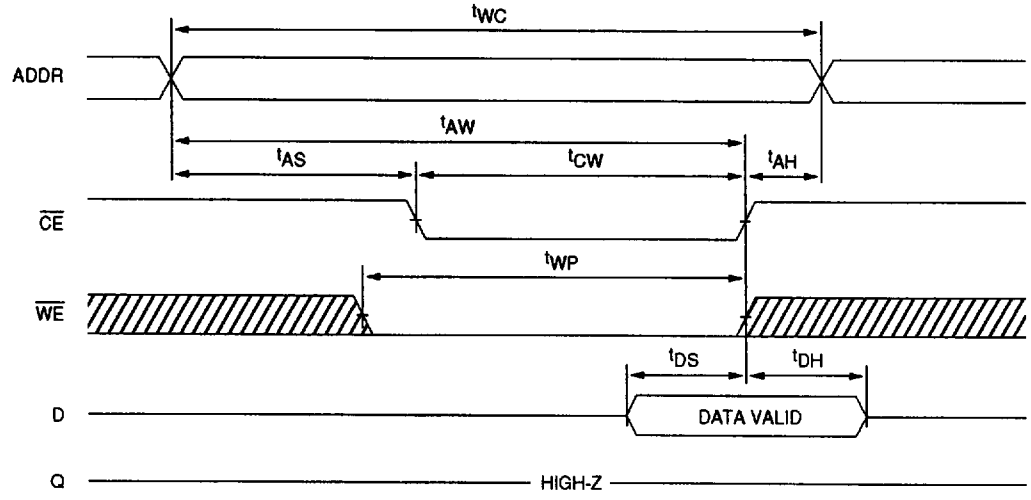


DON'T CARE

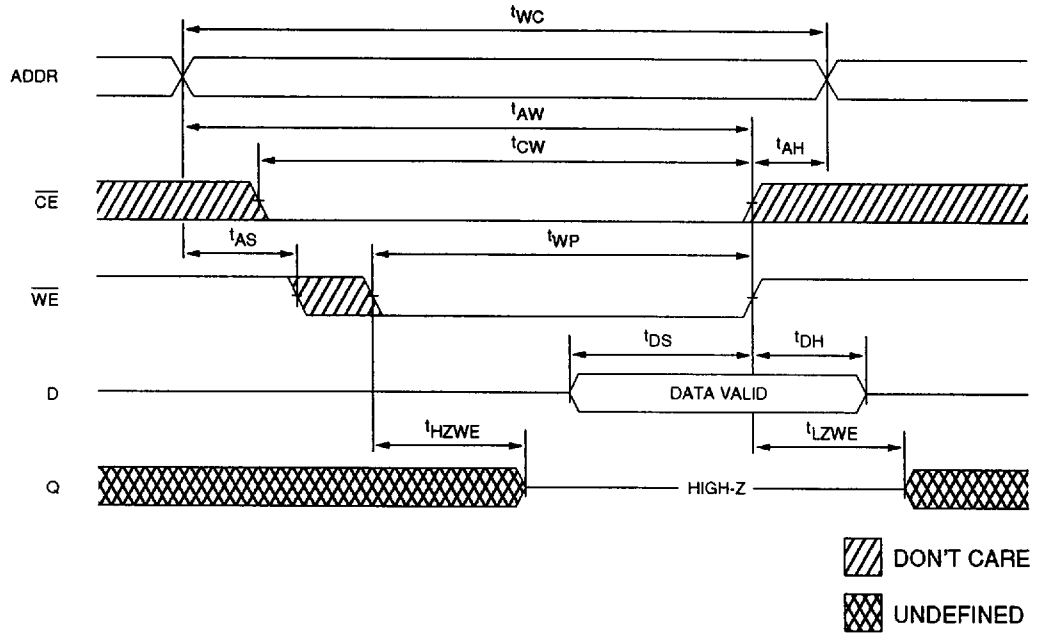
UNDEFINED

6

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



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ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.
** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.

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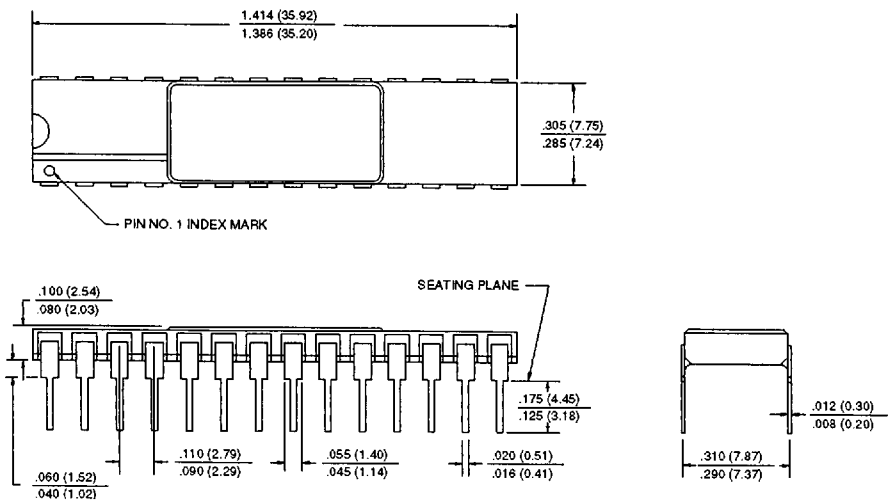
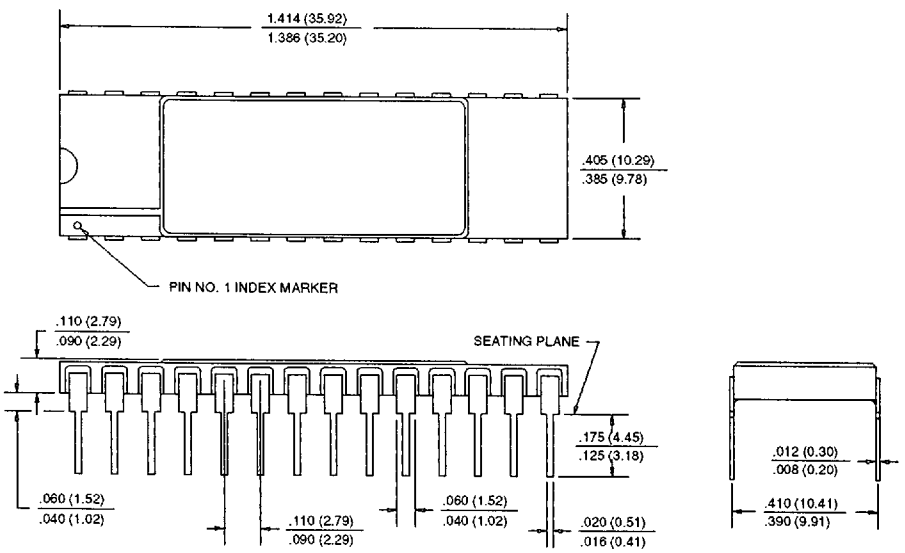
PACKAGE NO. 108
28 CDIP (300 mils) D-15

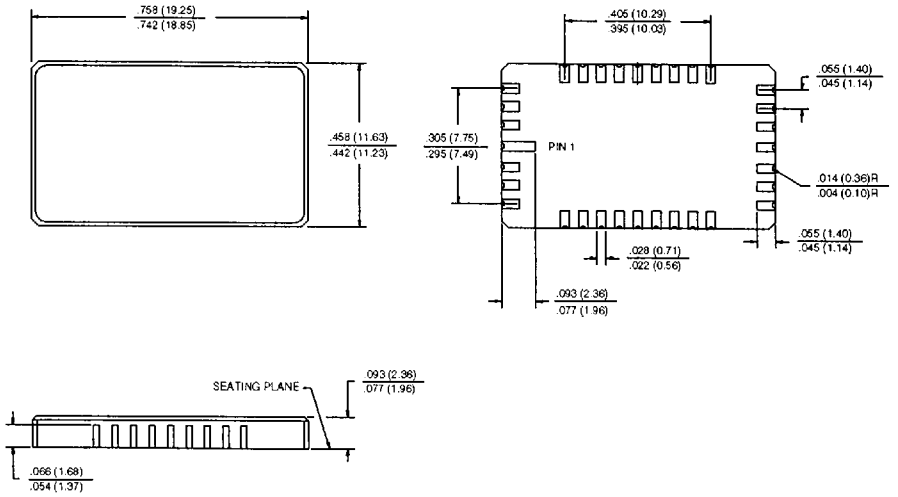


PACKAGE NO. 109
28 CDIP (400 mils)

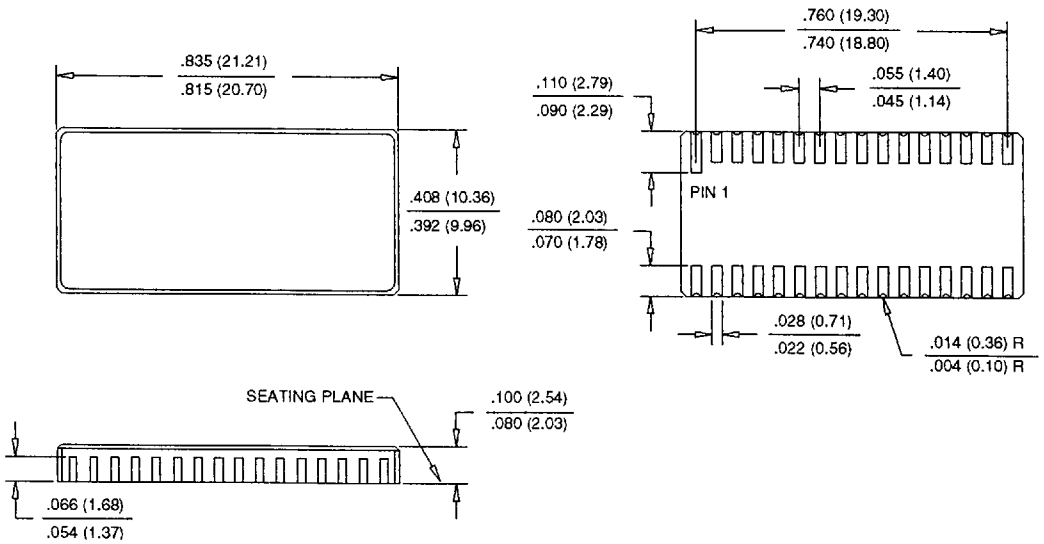


PKG-5

PACKAGE NO. 206
32 CLCC

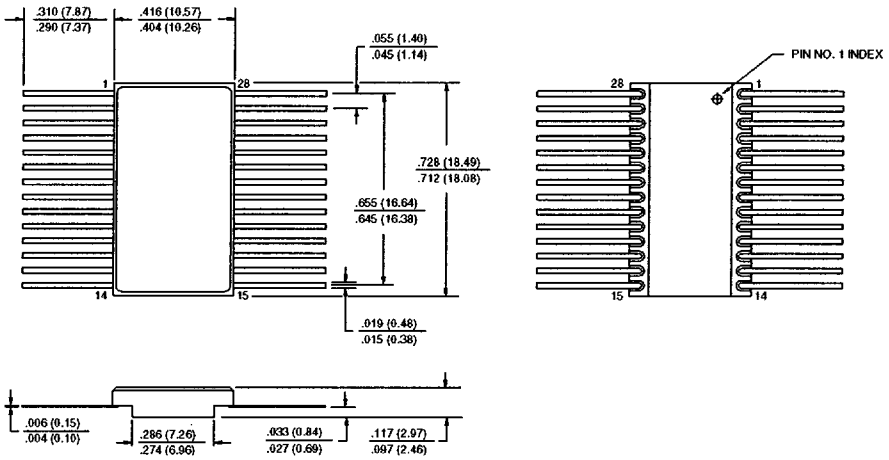


PACKAGE NO. 207
32 CLCC

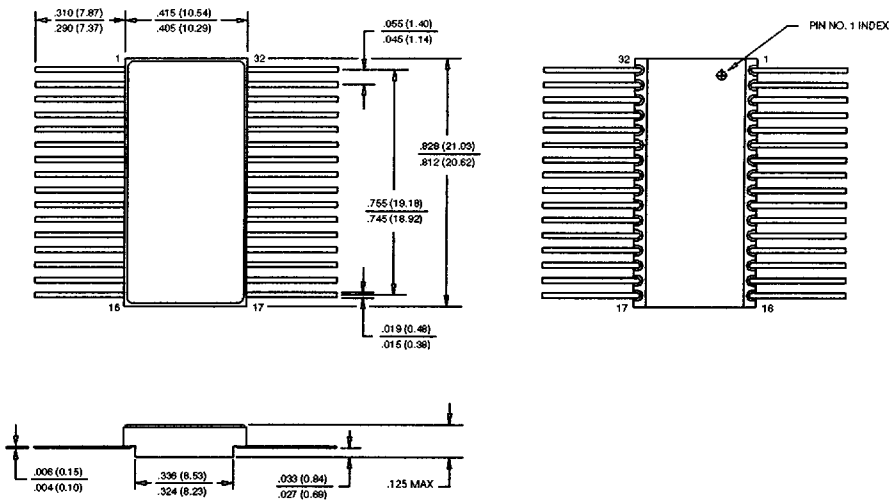


PKG-11

PACKAGE NO. 302
28 FP F-12

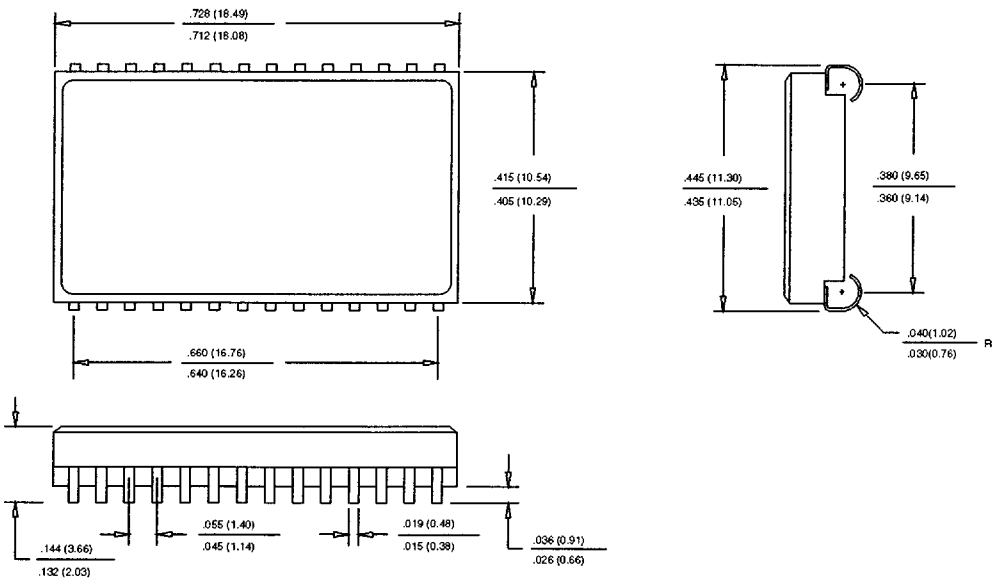


PACKAGE NO. 303
32 FP

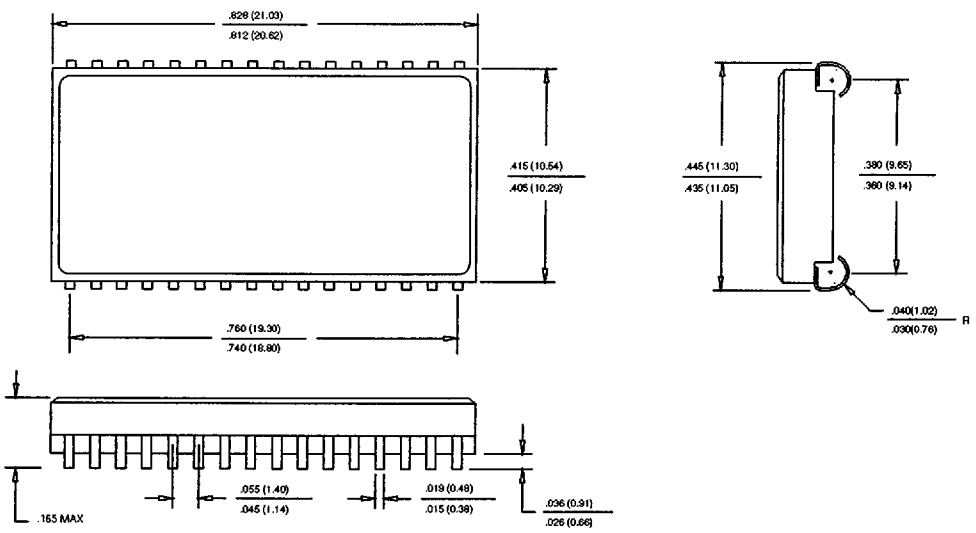


PKG-16

PACKAGE NO. 500
28 CSOJ



PACKAGE NO. 501
32 CSOJ



PKG-20