

# OKI Semiconductor

## MSC23S4641E-8BS16

4,194,304 Word x 64 Bit SYNCHRONOUS DYNAMIC RAM MODULE (2BANK):

### DESCRIPTION

The Oki MSC23S4641E-8BS16 is a fully decoded, 4,194,304 x 64bit synchronous dynamic random access memory composed of sixteen 16Mb DRAMs(2Mx8) in TSOP packages mounted with decoupling capacitors on a 168-pin glass epoxy Dual-in-Line Package supports any application where high density and large capacity of storage memory are required, like for example PCs or servers.

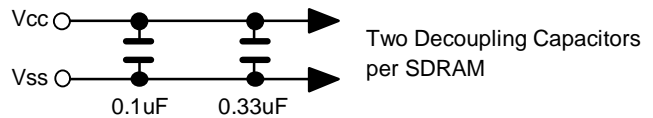
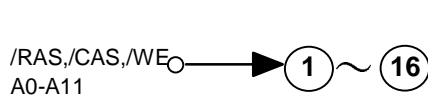
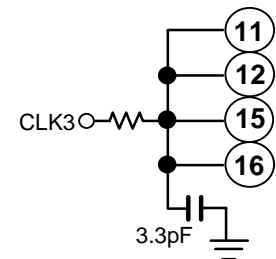
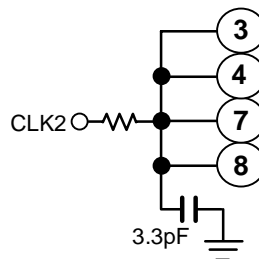
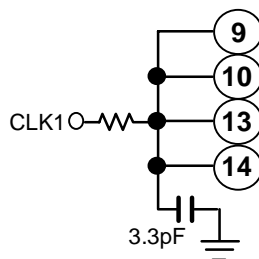
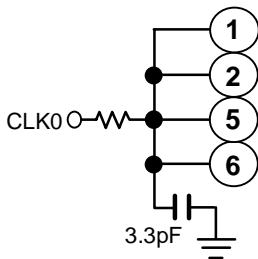
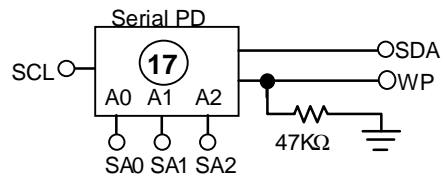
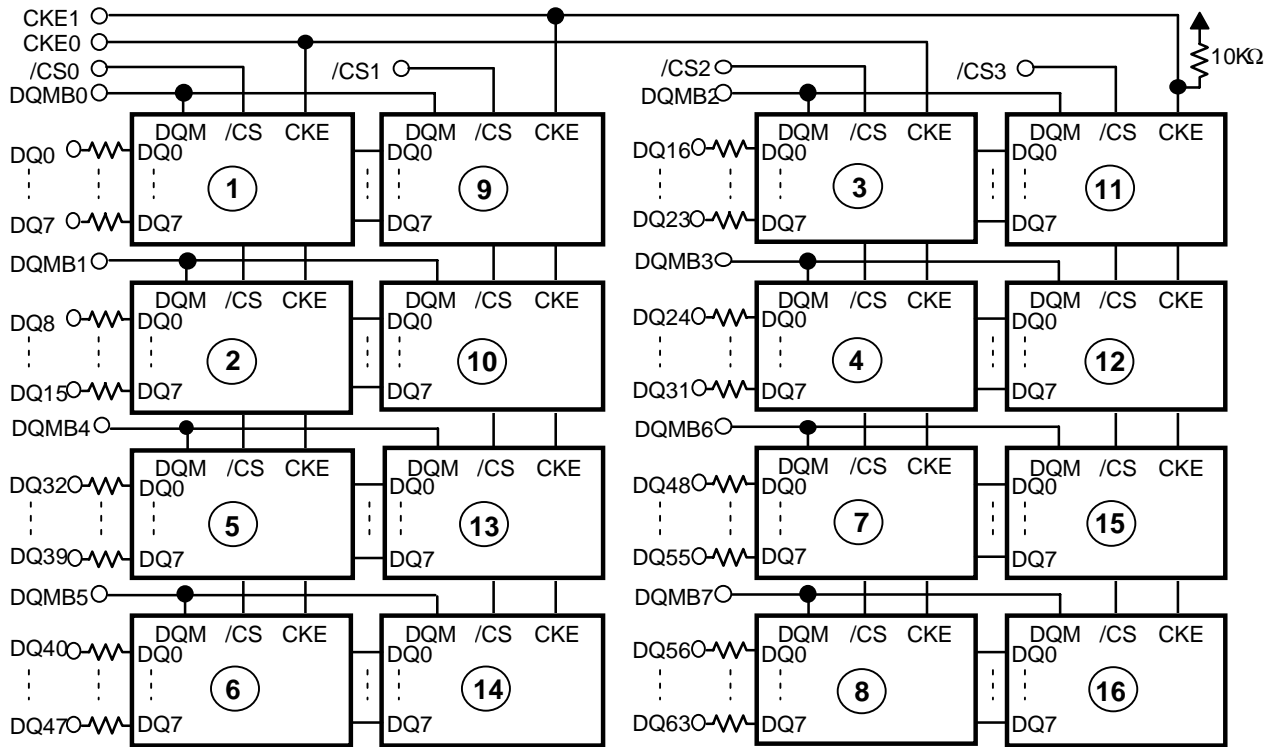
### FEATURES

- 4-Meg Word x 64-Bit (2Bank 8 Byte) organization
- 168-pin Dual Inline Memory Module
- All DQ Pins have 10 $\Omega$  Damping Resister
- Single 3.3V power supply,  $\pm$ 0.3V tolerance
- Input :LVTTL compatible
- Output :LVTTL compatible
- Refresh : 4,096 cycles/64 ms
- Programmable data transfer mode
  - CAS latency(2, 3)
  - Burst length(1,2,4,8,Full)
  - Data scramble(sequential,interleave)
- CBR auto-refresh, Self-refresh capability
- Serial Presence Detect (SPD) With EEPROM

### PRODUCT ORGANIZATION

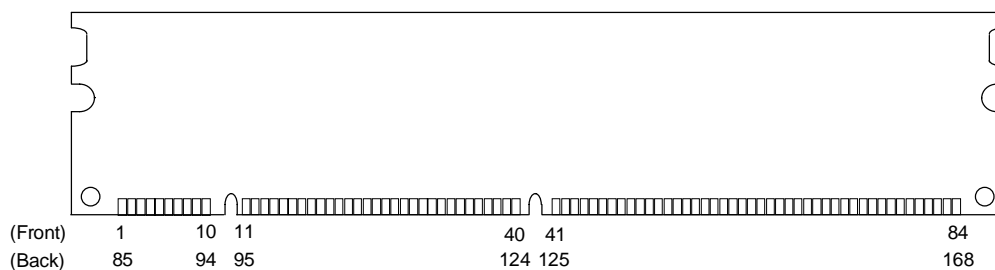
Product Name	Operation Frequency(Max.)	Access Time(Max.)	
		tAC2	tAC3
MSC23S4641E-8BS16	125MHz	10.0ns	6.0ns

# BLOCK DIAGRAM



Note. The Value of all resistors is 10Ω expect WP and CKE1

# MODULE OUTLINE



## PIN CONFIGURATION

Front side		Back side	
Pin No.	Pin name	Pin No.	Pin name
1	VSS	85	VSS
2	DQ0	86	DQ32
3	DQ1	87	DQ33
4	DQ2	88	DQ34
5	DQ3	89	DQ35
6	VCC	90	VCC
7	DQ4	91	DQ36
8	DQ5	92	DQ37
9	DQ6	93	DQ38
10	DQ7	94	DQ39
11	DQ8	95	DQ40
12	VSS	96	VSS
13	DQ9	97	DQ41
14	DQ10	98	DQ42
15	DQ11	99	DQ43
16	DQ12	100	DQ44
17	DQ13	101	DQ45
18	VCC	102	VCC
19	DQ14	103	DQ46
20	DQ15	104	DQ47
21	N.C	105	N.C
22	N.C	106	N.C
23	VSS	107	VSS
24	N.C	108	N.C
25	N.C	109	N.C
26	VCC	110	VCC
27	/WE	111	/CAS
28	DQMB0	112	DQMB4
29	DQMB1	113	DQMB5
30	/CS0	114	/CS1
31	N.C	115	/RAS
32	VSS	116	VSS
33	A0	117	A1
34	A2	118	A3
35	A4	119	A5
36	A6	120	A7
37	A8	121	A9
38	A10	122	A11(BA0)
39	N.C	123	N.C
40	VCC	124	VCC
41	VCC	125	CLK1
42	CLK0	126	N.C

Front side		Back side	
Pin No.	Pin name	Pin No.	Pin name
43	VSS	127	VSS
44	N.C	128	CKE0
45	/CS2	129	/CS3
46	DQMB2	130	DQMB6
47	DQMB3	131	DQMB7
48	N.C	132	N.C
49	VCC	133	VCC
50	N.C	134	N.C
51	N.C	135	N.C
52	N.C	136	N.C
53	N.C	137	N.C
54	VSS	138	VSS
55	DQ16	139	DQ48
56	DQ17	140	DQ49
57	DQ18	141	DQ50
58	DQ19	142	DQ51
59	VCC	143	VCC
60	DQ20	144	DQ52
61	N.C	145	N.C
62	N.C	146	N.C
63	CKE1	147	N.C
64	VSS	148	VSS
65	DQ21	149	DQ53
66	DQ22	150	DQ54
67	DQ23	151	DQ55
68	VSS	152	VSS
69	DQ24	153	DQ56
70	DQ25	154	DQ57
71	DQ26	155	DQ58
72	DQ27	156	DQ59
73	VCC	157	VCC
74	DQ28	158	DQ60
75	DQ29	159	DQ61
76	DQ30	160	DQ62
77	DQ31	161	DQ63
78	VSS	162	VSS
79	CLK2	163	CLK3
80	N.C	164	N.C
81	WP	165	SA0
82	SDA	166	SA1
83	SCL	167	SA2
84	VCC	168	VCC

Pin Name	Function	Pin Name	Function
VCC	Power Supply (3.3V)	/WE	Write Enable
VSS	Ground (0V)	DQMB#	Data Input/Output Mask
CLK#	System Clock	DQ#	Data Input/Output
/CS#	Chip Select	WP	Write Protect
CKE#	Clock Enable	SDA	Data I/O for SPD
A0-A10	Address	SCL	CLK input for SPD
A11	Bank Select Address	SA#	Socket Position Address for SPD
/RAS	Row Address Strobe	N.C	No Connection
/CAS	Column Address Strobe		

**SERIAL PRESENCE DETECT**

Byte No.	SPD Hex Value	Remark	Notes
0	80	Defines the number of bytes written into SPD memory	128 byte
1	08	Total number of bytes of SPD memory	256 byte
2	04	Fundamental memory type	SDRAM
3	0B	Number of rows	11 rows
4	09	Number of columns	9 columns
5	02	Number of module banks	2 bank
6	40	Data width of this assembly	64 bits
7	00	... Data width continuation	0
8	01	Voltage interface level	LVTTL
9	80	Cycle time (CL=3)	CL=3 tCC=8ns
10	60	Access time from CLK (CL=3)	CL=3 tAC3=6ns
11	00	DIMM configuration type	Non Parity
12	80	Refresh rate / type	Normal/ Self/
13	08	Primary SDRAM width	x8
14	00	Error checking SDRAM width	
15	01	Minimum CLK delay	tCCD: 1 CLK
16	8F	Burst lengths supported	1,2,4,8,F
17	02	Number of banks on each SDRAM	2 banks
18	06	/CAS latency	2,3
19	01	/CS latency	0
20	01	/WE latency	0
21	00	SDRAM module attributes	
22	06	SDRAM device attributes : General	
23	C0	Cycle time (CL=2)	CL=2 tCC2=12ns
24	A0	Access time from CLK (CL=2)	CL=2 tAC2=10ns
25	00	Cycle time (CL=1)	Not support
26	00	Access time from CLK (CL=1)	Not support
27	14	Minimum ROW pulse width	tRP=20ns
28	14	/RAS to /RAS bank delay	tRRD=20ns
29	14	/RAS to /CAS delay	tRCD=20ns
30	30	Minimum /RAS precharge time	tRAS=48ns
31	04	Density of each bank on module	16MB
32	20	Command and address signal input setup time	2ns
33	10	Command and address signal input hold time	1ns
34	20	Data signal input setup time	2ns
35	10	Data signal input hold time	1ns
36-61	00-00		R.F.U
62	12	SPD data revision code	1.2
63	2D	Checksum for byte 0-62	
64-71	41,45,20,20,20,20,20,20	Manufacturer's JEDEC ID code	
72	01/06	Manufacturing location	
73-90	43,32,33,53,34,36,34,31,45,2D,38,42,53,31,36,20,20,20	Manufacturer's part number	C23S4641E-8BS16
91,92	20,20	Revision code	
93-125	00-00	R.F.U	
126	64	Intel specification frequency	100MHz
127	F5	Intel specification /CAS latency	CLK0-3,CL=3
128-255	FF-FF	Unused storage locations	

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Voltage on any pin relative to Vss	$V_{IN}, V_{OUT}$	-0.5 to VCC+0.5	V
Vcc supply voltage	Vcc,VccQ	-0.5 to 4.6	V
Storage temperature	$T_{stg}$	- 55 to 125	°C
Power dissipation	$P_D^*$	16	W
Short circuit current	Ios	50	mA
Operating temperature	$T_{opr}$	0 to 70	°C

\*:  $T_a=25^{\circ}\text{C}$

### Recommended Operating Conditions

(Voltages referenced to Vss = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc,VccQ	3.0	3.3	3.6	V
Input high voltage	$V_{IH}$	2.0	-	VCC+0.3	V
Input low voltage	$V_{IL}$	-0.3	-	0.8	V

### Capacitance

(Vcc=3.3V ± 0.3V,  $T_a = 25^{\circ}\text{C}$  f=1MHz)

Parameter	Symbol	Max.	Unit
Input capacitance(A0-A11,/RAS, /CAS,/WE)	CIN1	98	pF
Input capacitance(/CS0,/CS1,/CS2,/CS3)	CIN2	34	pF
Input capacitance(DQMB0-DQMB7)	CIN3	22	pF
Input capacitance(CKE0,CKE1)	CIN4	58	pF
I/O capacitance(DQ0-DQ63)	CDQ	25	pF
Input capacitance(CLK0,CLK1,CLK2,CLK3)	CCLK	50	pF

## DC CHARACTERISTICS

(VCC = 3.3V ± 0.3V, Ta = 0 to 70°C)

Parameter	Symbol	Condition			Module Spec.		Unit	Note
		Bank	CKE	Others	Min	Max		
Input Leakage Current	I <sub>LI</sub>	-	-	-	-160	160	uA	
Output Leakage Current	I <sub>LO</sub>	-	-	-	-20	20	uA	
Output High Voltage	V <sub>OH</sub>	-	-	I <sub>OH</sub> = -2mA	2.4	-	V	
Output Low Voltage	V <sub>OL</sub>	-	-	I <sub>OL</sub> = 2mA	-	0.4	V	
Average Power Supply Current (Operating)	ICC1	One Bank Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> =min t <sub>RC</sub> =min No Burst	-	1000	mA	1,2
	ICC1D	Both Banks Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> =min t <sub>RC</sub> =min t <sub>RRD</sub> =min No Burst	-	1240	mA	1,2
Power Supply Current (Stand by)	ICC2	Both Banks Precharge	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> =min	-	640	mA	3
Average Power Supply Current (Clock Suspenson)	ICC3S	Both Banks Active	CKE ≤ V <sub>IL</sub>	t <sub>CC</sub> =min	-	344	mA	2
Average Power Supply Current (Active Stand by)	ICC3	One Banks Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> =min	-	680	mA	3
Power Supply Current (Burst)	ICC4	Both Banks Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> =min	-	1160	mA	1,2
Power Supply Current (Auto-Refresh)	ICC5	One Bank Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> =min t <sub>RC</sub> =min	-	960	mA	2
Average Power Supply Current (Self-Refresh)	ICC6	Both Banks Precharge	CKE ≤ V <sub>IL</sub>	t <sub>CC</sub> =min	-	32	mA	
Average Power Supply Current (Power down)	ICC7	Both Banks Precharge	CKE ≤ V <sub>IL</sub>	t <sub>CC</sub> =min	-	32	mA	

- NOTE: 1. Measured with the output open.  
 2. The address and data can be changed once or left unchanged during one cycle.  
 3. The address and data can be changed once or left unchanged during two cycles.

## MODE SET ADDRESS KEYS

/CAS Latency				Burst Type		Burst Length				
A6	A5	A4	CL	A3	BT	A2	A1	A0	BT=0	BT=1
0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	0	1	Reserved	1	Interleave	0	0	1	2	2
0	1	0	2			0	1	0	4	4
0	1	1	3			0	1	1	8	8
1	0	0	Reserved			1	0	0	Reserved	Reserved
1	0	1	Reserved			1	0	1	Reserved	Reserved
1	1	0	Reserved			1	1	0	Reserved	Reserved
1	1	1	Reserved			1	1	1	Full Page	Reserved

Note: A7,A8,A9, A10 and A11 should stay "L" during mode set cycle.

## POWER ON SEQUENCE

1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the VCC voltage has reached the specified level,pause for 200us or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply a CBR auto-refresh eight or more times.
5. Enter the mode register setting command.

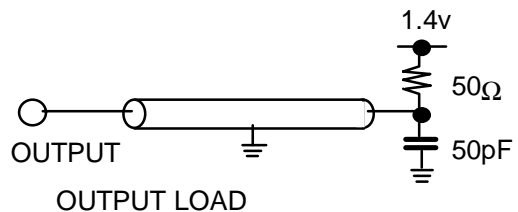
# AC CHARACTERISTIC

(VCC = 3.3 ± 0.3V, Ta = 0 ~70°C)

Parameter	Symbol	Module Spec.		Unit	Note	
		Min.	Max.			
Clock Cycle Time	CL=3	tCC	8	-	ns	
	CL=2		12	-	ns	
Access Time from Clock	CL=3	tAC	-	6	ns	3,4
	CL=2		-	10	ns	3,4
Clock "H" Pulse Time		tCH	3	-	ns	
Clock "L" Pulse Time		tCL	3	-	ns	
Input Setup Time(CLK,ADD,DIN)		tSI	2	-	ns	
Input Hold Time(CLK,ADD,DIN)		tHI	1	-	ns	
Output Low Impedance Time from Clock		tOLZ	3	-	ns	
Output High Impedance Time from Clock		tOHZ	-	9	ns	
Output Hold from Clock		tOH	3	-	ns	
/RAS Cycle Time		tRC	70	-	ns	
/RAS Precharge Time		tRP	20	-	ns	
/RAS Active Time		tRAS	48	100,000	ns	
/RAS to /CAS Delay Time		tRCD	20	-	ns	
Write Recovery Time		tWR	8	-	ns	
Write Command Input Time from Output		tOWD	20	-	ns	
/RAS to /RAS Bank Active Delay Time		tRRD	20	-	ns	
Refresh Time		tREF	-	64	ms	
Power-down Exit Set-up Time		tPDE	10	-	ns	
Input Level Transition Time		tT	-	3	ns	
/CAS to /CAS Delay Time (Min)		ICCD	1		Cycle	
Clock Disable Time from CKE		ICKE	1		Cycle	
Data Output High Impedance Time from DQM		IDOZ	2		Cycle	
Data Input Mask Time from DQMB		IDOD	0		Cycle	
Data Input Time from Write Command		IDWD	0		Cycle	
Data Output High Impedance Time		IROH	CL		Cycle	
Active Command Input Time from MODE		IMRD	3		Cycle	

**NOTES:**

- 1) AC measurements assume that tT=1ns.
- 2) The reference level for timing of input signals is 1.4V.
- 3) This parameter is measured with a load circuit equivalent to 1 TTL load and 50pF (R Load is 50ohm).
- 4) An access time is measured at 1.4V.
- 5) If tT is longer than 1ns, the reference level for timing of input signals are VIH and VIL.





**FUNCTION TRUTH TABLE (Table1)(1/2)**

Current State	/CS	/RAS	/CAS	/WE	BA	ADDR	Action
Idle	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	Row Active
	L	L	H	L	BA	A10	NOP <sup>4</sup>
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh <sup>5</sup>
	L	L	L	L	L	OP Code	Mode Register write
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BA	CA,A10	Read
	L	H	L	L	BA	CA,A10	Write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP(Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP(Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Reserved
	L	H	L	H	BA	CA,A10	Term Burst,start new Burst Read
	L	H	L	L	BA	CA,A10	Term Burst,start new Burst Write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	Term Burst,execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP(Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP(Continue Row Active after Burst ends)
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BA	CA,A10	Term Burst,start new Burst Read
	L	H	L	L	BA	CA,A10	Term Burst,start new Burst Write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	Term Burst,execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP(Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP(Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BA	CA,A10	ILLEGAL <sup>2</sup>
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA,A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	X	NOP(Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP(Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BA	CA,A10	ILLEGAL <sup>2</sup>
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA,A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL

**FUNCTION TRUTH TABLE (Table1)(2/2)**

Current State	/CS	/RAS	/CAS	/WE	BA	ADDR	Action
Precharge	H	X	X	X	X	X	NOP → Idle after tRP
	L	H	H	H	X	X	NOP → Idle after tRP
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	NOP <sup>4</sup>
	L	L	L	X	X	X	ILLEGAL
Write Recovery	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Row Active	H	X	X	X	X	X	NOP Row Active after tRCD
	L	H	H	H	X	X	NOP Row Active after tRCD
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Refresh	H	X	X	X	X	X	NOP → Idle after tRC
	L	H	H	X	X	X	NOP → Idle after tRC
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Resister Access	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

**ABBREVIATIONS**

RA=Row Address  
CA=Column Address

BA=Bank Address  
AP=Auto Precharge

NOP=No Operation command

**Notes:**

- All inputs will be enabled when CKE is set high for at least 1 cycle prior to the inputs.
- Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
- Satisfy the timing of tCCD and tWR to prevent bus contention.
- NOP to bank precharging or in idle state. Precharges activated bank by BA or A10.
- Illegal if any bank is not idle.

**FUNCTION TRUTH TABLE (CKE) (Table2)**

Current State(n)	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	Action
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh → ABI
	L	H	L	H	H	H	X	Exit Self Refresh → ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Self Refresh)
Power Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down → ABI
	L	H	L	H	H	H	X	Exit Power Down → ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	X	ILLEGAL <sup>6</sup>
	L	L	X	X	X	X	X	NOP(Continue power down mode)
All Banks idle <sup>6</sup> (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	L	L	L	L	L	L	X	ILLEGAL
Any State Other than Listed Above	L	L	X	X	X	X	X	NOP
	H	H	X	X	X	X	X	Refer to Operations in Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

Notes:

6. Power-down and self refresh can be entered only when all the banks are in an idle state.