HYUNDAI SEMICONDUCTOR

HY61C16

2048×8-Bit CMOS Static RAM

FEBRUARY 1986

DESCRIPTION

The HY61C16 is a high speed, low power, 2048-word by 8-bit static CMOS RAM fabricated using high-performance CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields access times of 45 ns maximum.

When the chip select is brought high, the device assumes a standby mode in which the device power dissipation is reduced to 0.5 μW (typically). The HY61C16L has a data retention mode that guarantees data will remain valid at a minimum power supply voltage of 2.0 volts.

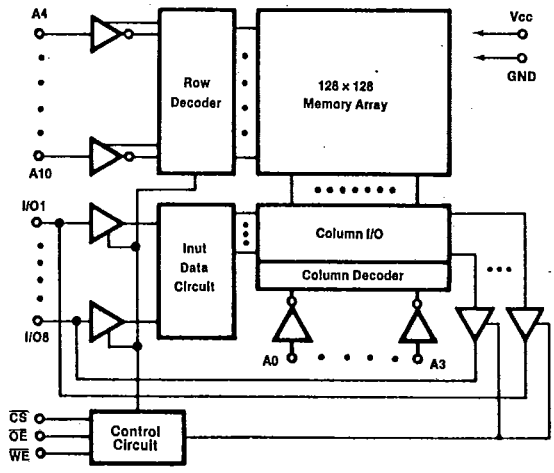
Using CMOS technology, supply voltages from 2.0 to 5.5 volts have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY61C16 family.

FEATURES

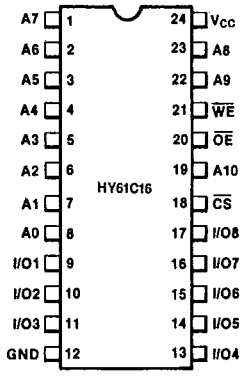
- ▲ **High Speed**
  - — **Maximum access time of 45/55/70 ns**
  - — **Equal access and cycle times**
- ▲ **Low Power**
  - — **200 mW typical operating**
  - — **0.5μW typical standby**
  - — **0.1μW typical data retention**
- ▲ **Battery Backup**
  - — **2 volt data retention (HY61C16-L)**
- ▲ **Six transistor CMOS Memory Cell**
- ▲ **CMOS process virtually eliminates alpha particle induced soft errors without die coating**
- ▲ **Fully Static Operation**
  - — **No clock or refresh required**
- ▲ **Pin Compatible with Standard 16K Static RAMS and EPROMS in 600 mil DIP**
- ▲ **For extended temperature ranges, variations in access times, packages, power consumption, and screening, call HYUNDAI.**

Part Number	Access Time (ns, max)	POWER SUPPLY CURRENT Active (mA, max)	Standby (μA, max)	Data Retention (μA, max)
HY61C16-45	45	100	100	N/A
HY61C16-55	55	80	100	N/A
HY61C16-70	70	70	100	N/A
HY61C16L-45	45	90	2	2
HY61C16L-55	55	70	2	2
HY61C16L-70	70	60	2	2

BLOCK DIAGRAM



PIN CONNECTIONS



(TOP VIEW)

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{TERM}	Voltage on any Pin with Respect to GND	−0.5* to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−10 to +85	°C
T_{STG}	Storage Temperature	−55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

*−3.5V for 20ns pulse.

RECOMMENDED OPERATING CONDITIONS

T_A=0 to 70°C

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC}	V
V_{IL}	Input Low Voltage	−0.5*	—	+0.8	V
C_L	Output Load	—	—	30	pF

* −3.5V for 20ns pulse.

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

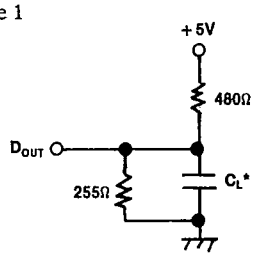
AC TEST CONDITIONS

T_A=0 to 70°C

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
	(See Figure 1)

OUTPUT LOAD

Figure 1



*Including scope and the jig

C_L=30 pF standard output
C_L=5 pF for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW}

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

CAPACITANCE[1]

T_A=25°C, f=1.0MHz

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

1. This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5V ± 10%, T_A = 0 to 70°C

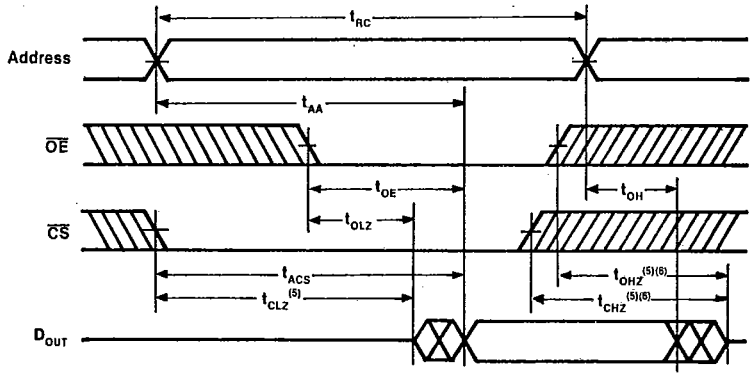
READ CYCLE

SYMBOL	PARAMETER	HY61C16-45		HY61C16-55		HY61C16-70		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	70	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	20	—	25	—	50	ns
t_{OLZ}	Output Enable to Output in Low Z	0	—	5	—	5	—	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	20	0	25	0	35	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	25	—	35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns

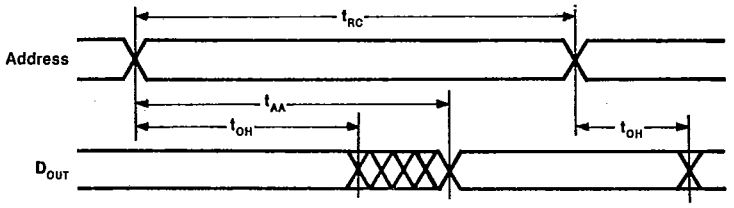
NOTES:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and load capacitance, as in Output Load.

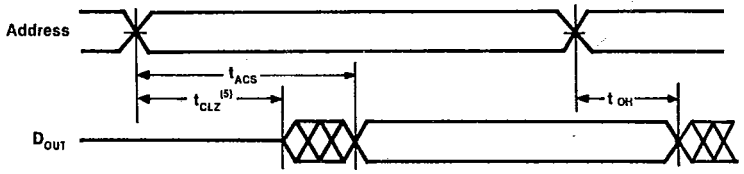
TIMING WAVEFORMS OF READ CYCLE 1[1]



READ CYCLE 2[1,2,4]



READ CYCLE 3[1,3,4]



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. t_{OHZ} and t_{CHZ} are tested with C_L = 5 pF.

AC ELECTRICAL CHARACTERISTICS (1)

V_{CC}=5V±10%, T_A=0 to 70°C

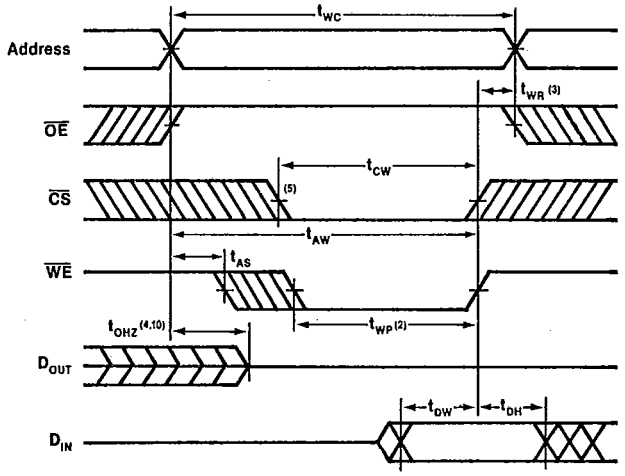
WRITE CYCLE

SYMBOL	PARAMETER	HY61C16-45		HY61C16-55		HY61C16-70		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{CW}	Chip Selection to End of Write	40	—	50	—	65	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	65	—	ns
t_{AS}	Address Set-up Time	0	—	10	—	15	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	5	—	5	—	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	25	—	35	ns
t_{WHZ}	Write to Output in High Z	0	20	0	25	0	40	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	30	—	ns
t_{DH}	Data Hold from Write Time	0	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	ns

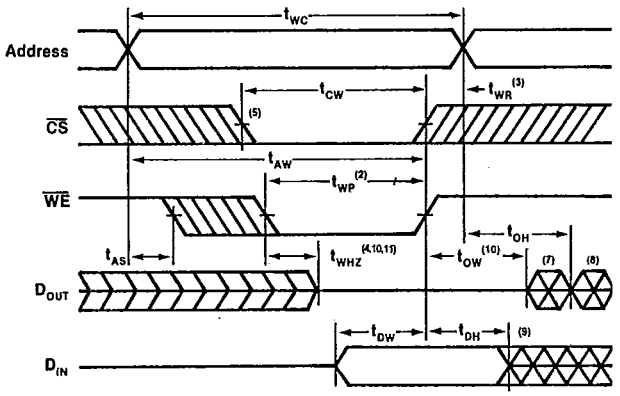
NOTES:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in Output Load.

TIMING WAVEFORMS OF WRITE CYCLE 1(1)



WRITE CYCLE 2(1,6)



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
11. t_{WHZ} is tested with C_L=5pF.

HY61C16 DC ELECTRICAL CHARACTERISTICS

V_{CC}=5V±10% T_A=0 to 70°C

SYMBOL	PARAMETER	TEST CONDITIONS		HY61C16 Min.	HY61C16 Typ.[1]	HY61C16 Max.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC}=5.5V, V_{IN}=GND to V_{CC}		—	—	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$= V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=GND to V_{CC}		—	—	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA Duty Cycle=100%	HY61C16-45	—	60	100	mA
			HY61C16-55	—	45	80	mA
			HY61C16-70	—	40	70	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$=V_{IH}		—	2	5	mA
I_{SB1}		$\overline{CS}$≥V_{CC}-0.2V, V_{IN}=0 to V_{CC}		—	4	100	μA
V_{OL}	Output Low Voltage	I_{OL}=8mA		—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−4.0mA		2.4	—	—	V

HY61C16L DC ELECTRICAL CHARACTERISTICS

V_{CC}=5V ± 10%, T_A=0 to 70°C

SYMBOL	PARAMETER	TEST CONDITIONS		HY61C16L Min.	HY61C16L Typ.[1]	HY61C16L Max.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC}=5.5V, V_{IN}=GND to V_{CC}		—	—	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=GND to V_{CC}		—	—	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA Duty Cycle=100%	HY61C16L-45	—	50	90	mA
			HY61C16L-55	—	40	70	mA
			HY61C16L-70	—	35	60	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$=V_{IH}		—	2	5	mA
I_{SB1}		$\overline{CS}$≥V_{CC}-0.2V, V_{IN}=0 to V_{CC}		—	0.1	2	μA
V_{OL}	Output Low Voltage	I_{OL}=8mA		—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−4.0mA		2.4	—	—	V

NOTES:

1. V_{CC}=5V, T_A=25°C

LOW V_{CC} DATA RETENTION CHARACTERISTICS [1]

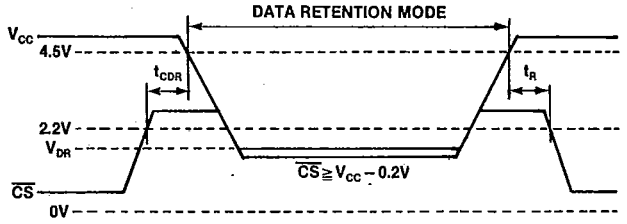
T_A=0°C to 70°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		Min.	Typ.	Max.		
Data Retention Supply Voltage	V_{CCDR}	2.0	—	5.5	V	V_{IN}=0 to V_{CC}, $\overline{CS}\geq V_{CC}-0.2V$
Data Retention Supply Current	I_{CCDR}	—	0.05	2.0	μA	V_{CC}=2.0V, V_{IN}=0 to V_{CC}, $\overline{CS}\geq V_{CC}-0.2V$
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	t_{RC}[2]	—	—	ns	

Notes:

1. For HY61C16L-45/55/70
2. t_{RC}=Read Cycle Time

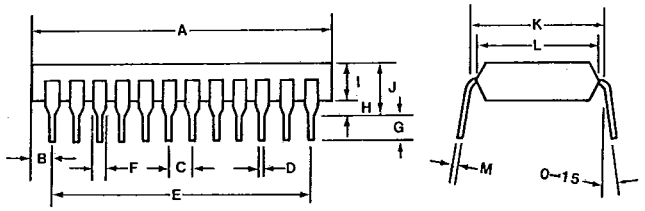
LOW V_{CC} DATA RETENTION WAVEFORM



PACKAGE OUTLINE

24 PIN PLASTIC

ITEM	MILLIMETERS	INCHES
A	31.75	1.250
B	1.905	0.075
C	2.54	0.100
D	0.457	0.018
E	27.94	1.100
F	1.524	0.060
G	3.302	0.130
H	0.508	0.020
I	3.81	0.150
J	4.318	0.170
K	15.24	0.600
L	13.716	0.540
M	0.254	0.010



ORDERING INFORMATION

HY61C16X-XX

L=Low Power
=Standard

45=45ns
55=55ns
70=70ns

HYUNDAI SEMICONDUCTOR

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