HOLTEK

283-599

HT6116-70
2K × 8 Bit SRAM

Features

- Single 5V power supply
- Low standby and operating power
  - Standby: 5μW (Typ.)
  - Operating: 400mW (Typ.)
- 70ns (Max.) high speed access time
- Neither external clock nor refreshing required
- Power down by pin $\overline{CS}$
- TTL compatible interface levels
- Pin compatible with standard 2K×8 bits of EPROM/MASK ROM
- Three-state output pins
- Memory expansion by pin $\overline{OE}$

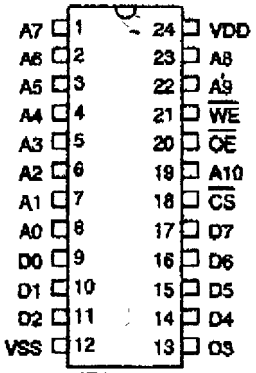
Applications

- Small-capacity memory units

General Description

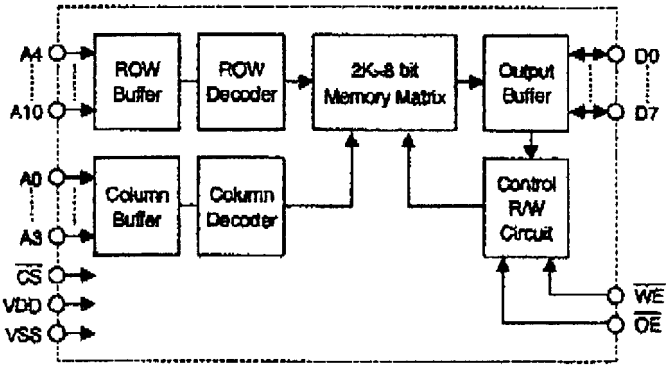
The HT6116-70 is a 16384-bit static random access memory. It is organized with 2048 words of 8 bits in length, and operates with a single 5V power supply. The IC is built with a high performance CMOS 0.8μm process in order to obtain a low standby current and high reliability. The IC contains six-transistor full CMOS memory cells and TTL compatible inputs and outputs, which are easily interface with common system bus structures. The Data bus of the HT6116-70 is designed as a three-state type The IC is in the standby mode if the $\overline{CS}$ pin is set to "high". The chip is packaged as a standard 24-pin DIP/SDIP/ SOP.

Pin Assignment



HT6116-70
– 24 DIP/SDIP/SOP

Block Diagram



Pin Description

Pin No.	Pin Name	I/O	Description
8~1, 23, 22, 19	A0~A7 A8, A9, A10	I	Address inputs
9~11 13~17	D0~D2 D3~D7	I/O	Data inputs and outputs
12	VSS	I	Negative power supply, usually connected to the ground
18	$\overline{CS}$	I	Chip select signal pin When this signal is high, the chip is in the standby mode. The chip is in the active mode, if $\overline{CS}$ is low.
20	$\overline{OE}$	I	Output enable signal pin
21	$\overline{WE}$	I	Write enable signal pin
24	VDD	I	Positive power supply

Absolute Maximum Rating

Supply Voltage ..... −0.3V to 5.5V
Input Voltage ..... V_{SS}−0.3V to V_{DD}+0.3V
Storage Temperature ..... −50°C to 125°C
Operating Temperature ..... −20°C to 70°C

D.C. Characteristics

(Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	4.5	5.0	5.5	V
I_{LI}	Input Leakage Current	5V	V_{IN}=0 to V_{DD}	—	0.1	10	μA
I_{LO}	Output Leakage Current	5V	V_O=0 to V_{DD}	—	0.1	10	μA
I_{DD}	Operating Current	5V	V_{IH}=2.2V, V_{IL}=0.8V In write mode, t_{WC}=1μs.	—	45	90	mA
		5V	V_{IH}=2.2V, V_{IL}=0.8V In read mode, t_{RC}=1μs.	—	80	90	mA
I_{STB}	Standby Current	5V	V_{IH}=2.2V, V_{IL}=0.8V (TTL Input)	—	0.8	1.5	mA
		5V	V_{IH}=4.8V, V_{IL}=0.2V (CMOS Input)	—	0.1	3	μA
V_{IH}	Input Voltage	5V	—	2.2	2	5.3	V
V_{IL}		5V		−0.3	0.2	0.8	V
I_{OH}	Output Source Current	5V	V_{OH}=4.5V	−1.2	−6.2	—	mA
I_{OL}	Output Sink Current	5V	V_{OL}=0.5V	4.8	14.5	—	mA

AC Test Condition and Load

Item	Condition
Input pulse high level	V_{IH}=3V
Input pulse low level	V_{IL}=0V
Input and output reference level	1.5V
Output load	See Figure 1

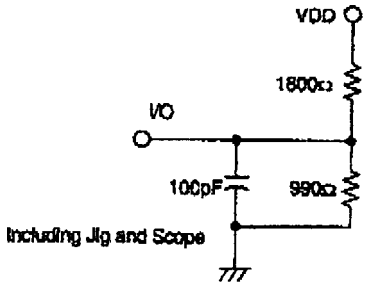


Figure1 Loading Diagram

AC Electrical Characteristics

Read cycle

(V_{DD}=5V±10%, GND=0V, Ta=0° to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	70	36	—	ns
t_{AA}	Address Access Time	—	35	70	ns
t_{ACS}	Chip Select Access Time	—	35	70	ns
t_{OE}	Output Enable to Output Valid	—	12	40	ns
t_{OH}	Output Hold from Address Change	10	12	—	ns
t_{CLZ}	Chip Enable to Output in Low-Z	10	—	—	ns
t_{OLZ}	Output Enable to Output in Low-Z	10	—	—	ns
t_{OHZ}	Output Disable to Output in High-Z	0	—	30	ns
t_{CHZ}	Chip Disable to Output in High-Z	0	—	30	ns

Write cycle (V_{DD}=5V±10%, GND=0V, Ta=0° to 70°C))

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WC}	Write Cycle Time	70	36	—	ns
t_{DW}	Data Set up Time	20	18	—	ns
t_{DH}	Data Hold Time from Write Time	5	0	—	ns
t_{AW}	Address Valid to End of Write	50	15	—	ns
t_{AS}	Address Setup Time	20	14		ns
t_{WP}	Write Pulse Width	25	0	—	ns
t_{WR}	Write Recovery Time	5	—	—	ns
t_{CW}	Chip Selection to End of Write	35	—	—	ns
t_{OW}	Output Active from End of Write	5	—	—	ns
t_{OHZ}	Output Disable to Output in High-Z	0	—	40	ns
t_{WHZ}	Write to Output in High-Z	0	—	50	ns

Function Description

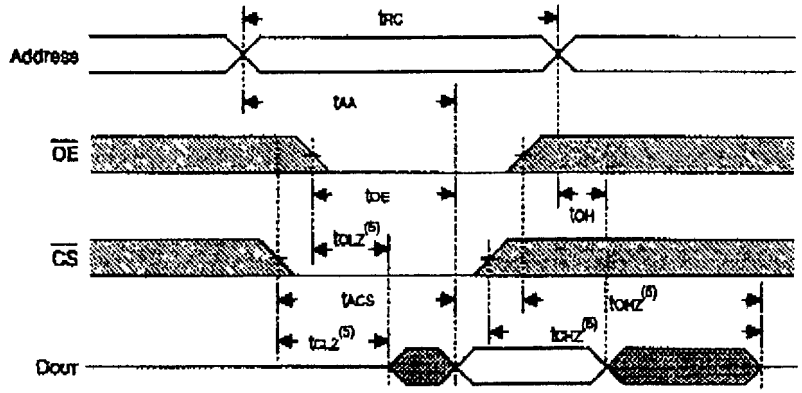
The HT6116-70 is a 2K×8 bit SRAM. When the $\overline{CS}$ pin of the chip is set to "low", data can be written in or read from eight data pins; otherwise, the chip is in the standby mode. During a write cycle, the data pins are defined as the input state by setting the $\overline{WE}$ pin to low. Data should be ready before the rising edge of the $\overline{WE}$ pin according to the timing of the writing cycle. While in the read cycle, the $\overline{WE}$ pin is set to high and the $\overline{OE}$ pin is set to low to define the data pins as the output state. All data pins are defined as a three-state type, controlled by the $\overline{OE}$ pin. In both cycles (namely, write and read cycles), the locations are defined by the address pins A0~A10. The following table illustrates the relations of $\overline{WE}$, $\overline{OE}$, $\overline{CS}$ and their corresponding mode.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	D0~D7
H	X	X	Stand-by	High-Z
L	L	H	Read	Dout
L	H	H	—	High-Z
L	X	L	Write	Din

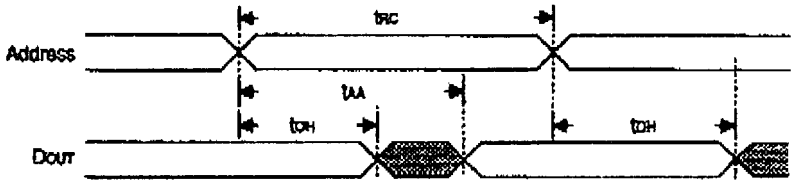
where. X stands for "don't care".
H stands for high level
L stands for low level.

Timing Diagrams

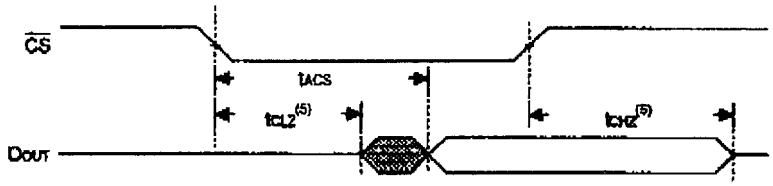
Read cycle (1)



Read cycle (1, 2, 4)



Read cycle (1, 3, 4)



Notes: (1) $\overline{WE}$ is high during the Read cycle

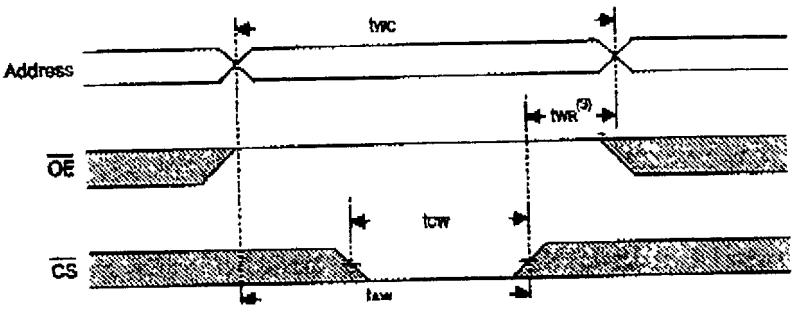
(2) Device is continuously enabled, $\overline{CS}$=V_{IL}

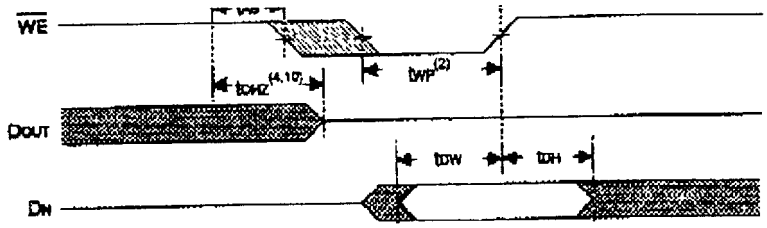
(3) Address is valid prior to or coincident with the $\overline{CS}$ transition low.

(4) $\overline{OE}$=V_{IL}

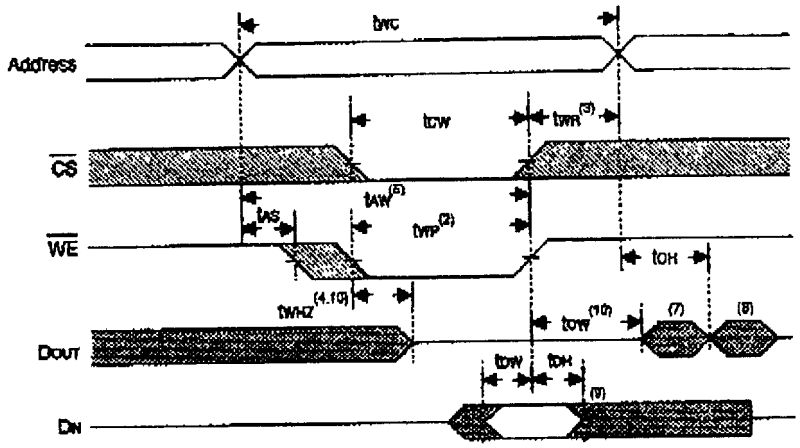
(5) Transition is measured±500mV from the steady state.

Write cycle 1 [1]





Write cycle 2 (1, 6)



Notes:
(1) $\overline{WE}$ must be high during all address transitions.
(2) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
(4) During this period, I/O pins are in the output state, so the input signals of the opposite phase to the outputs must not be applied.