HI-REL DATA SHEET

HM 65756

32 k x 8
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME : 25*/35/45/55 ns**
- **LOW POWER CONSUMPTION**
  ACTIVE : 825 mW
  STANDBY : 190 mW
- **WIDE TEMPERATURE RANGE : - 55 TO + 125°C**
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **OUTPUT ENABLE**
- **SINGLE 5 VOLT SUPPLY**

* Preliminary

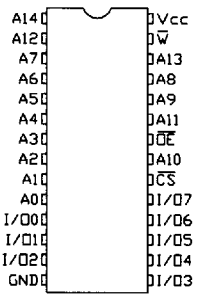
DESCRIPTION

The HM 65756 is a high speed CMOS static RAM organized as 32,768 x 8 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 25 ns are available.
The HM 65756 features fully static operation requiring no external clocks or timing strobes.The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.
Easy memory expansion is provided by an active low chip select ($\overline{CS}$) an active low output enable ($\overline{OE}$), and three state drivers.
All inputs and outputs of the HM 65756 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65756 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

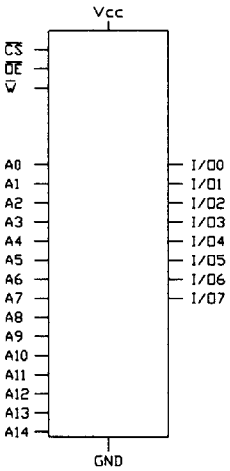
PACKAGES

Ceramic 300 and 600 mils, 28 pins, DIL. LCC 32 pins, LCC 28 pins

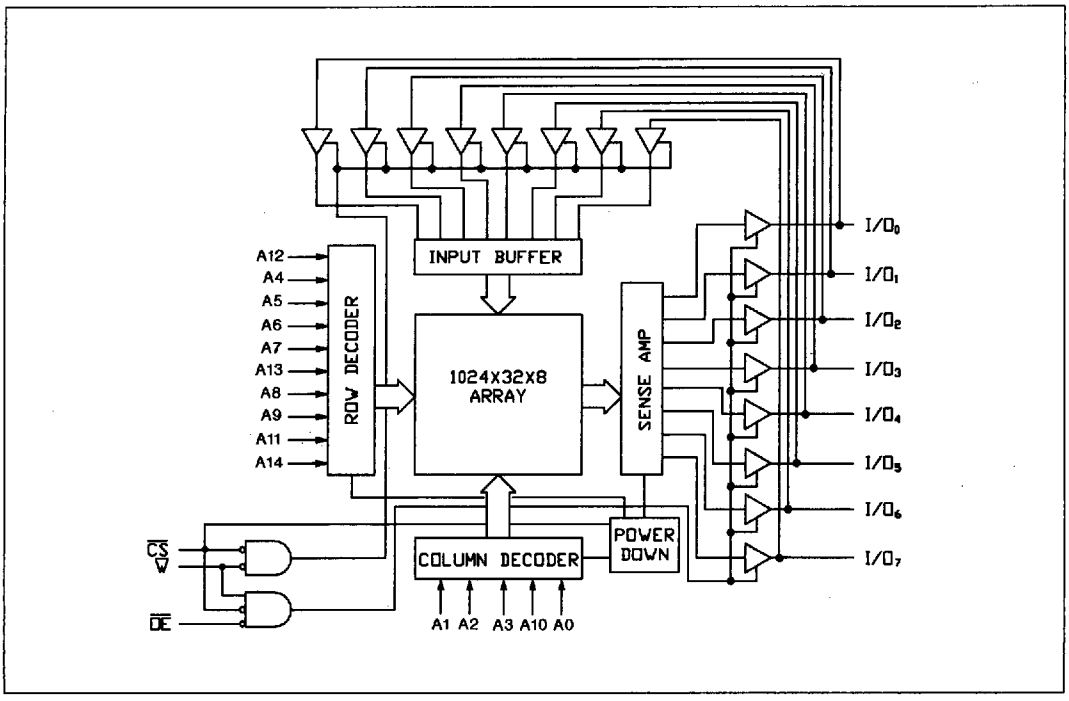
Pinout DIL 28 pins



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A14 : Address inputs	$\overline{CS}$: Chip-Select
I/00-I/07 : Inputs/Outputs	$\overline{OE}$: Output enable
VCC : Power	$\overline{W}$: Write Enable
GND : Ground	

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	I/O 's	MODE
H	X	X	Z	Stand-by
L	L	H	Output	Read
L	X	L	Input	Write
L	H	H	Z	Output disable

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V
DC input voltage : - 3.0 V to 7.0 V
DC output voltage in high Z state : - 0.5 V to + 7.0 V
Storage temperature : - 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2000 V
(MIL STD 883C method 3015)

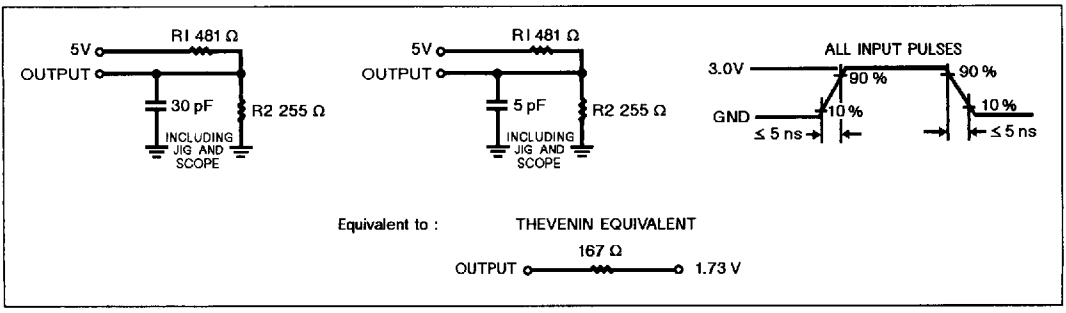
OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	5 V ± 10 %	- 55°C to + 125°C
Industrial	5 V ± 10 %	- 40°C to + 85°C

ELECTRICAL CHARACTERISTICS
DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65756 H	65756 K	65756 M	65756 N	Unit	Value	Note 6
ICCSB (1)	Standby supply current	20	20	20	20	mA	Max	M
ICCSB (1a)	Standby supply current	35	35	35	35	mA	Max	M
ICCOP (2)	Operating supply current	180	160	160	160	mA	Max	M
II X (3)	Input leakage current	± 10	± 10	± 10	± 10	µA	Max	M
IOZ (3)	Output leakage current	± 10	± 10	± 10	± 10	µA	Max	M
VIL (4)	Input low voltage	0.8	0.8	0.8	0.8	V	Max	T
VIH (4)	Input high voltage	2.2	2.2	2.2	2.2	V	Min	T
VOL (5)	Output low voltage	0.4	0.4	0.4	0.4	V	Max	M
VOH (5)	Output high voltage	2.4	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	5	5	5	5	pF	Max	G
C OUT	Output capacitance	7	7	7	7	pF	Max	G

Notes : 1. $\overline{CS}$ > = Vcc - 0.3V , VIN > Vcc - 0.3V or < = 0.3V
1a. $\overline{CS}$ = VIH
2. Vcc max, Output current = 0 mA, Minimum cycle
3. Vcc max, Vin = Gnd to Vcc
4. VIL min = - 3.0V, VIH max = Vcc
5. Vcc Min, IOL = 8 mA, IOH = - 4 mA
6. Including open/short test or inputs clamp voltage.
G - Guaranted - Not tested : Parameter measured at design validation and at any design change.
M - Measured : Parameter measured and data-log capability.
T - Tested : Parameter verification during testing.

AC TEST LOADS WAVEFORMS



AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)

Conditions :

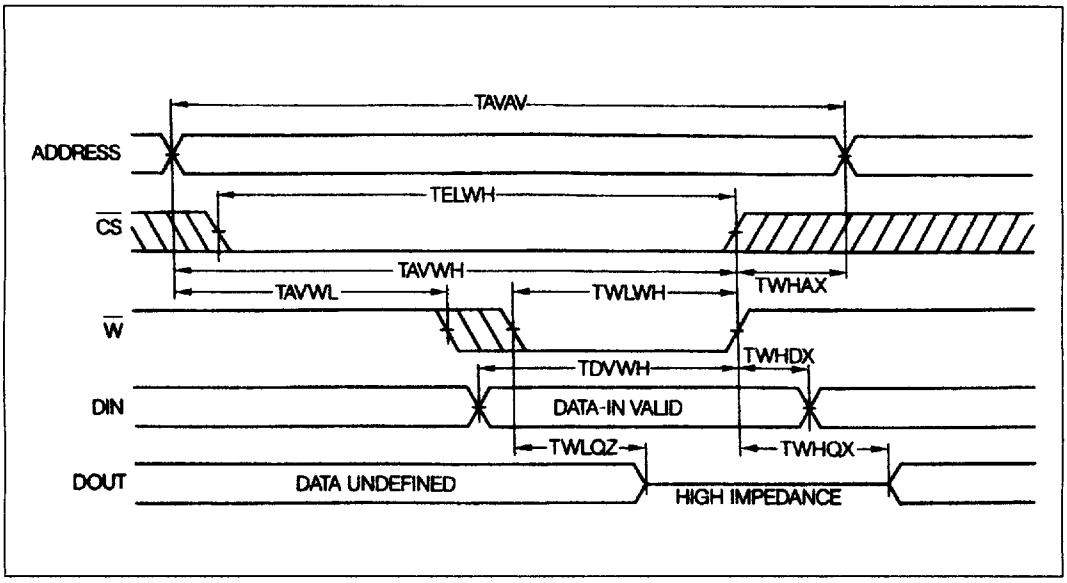
VCC	5V ± 10 %
Input pulse levels	Gnd to 3.0V
Input rise	5 ns
Input timing reference levels	1.5V
Output loading IOL / IOH	+ 30 pF
Operating temperature	- 55°C to + 125°C

WRITE CYCLE :

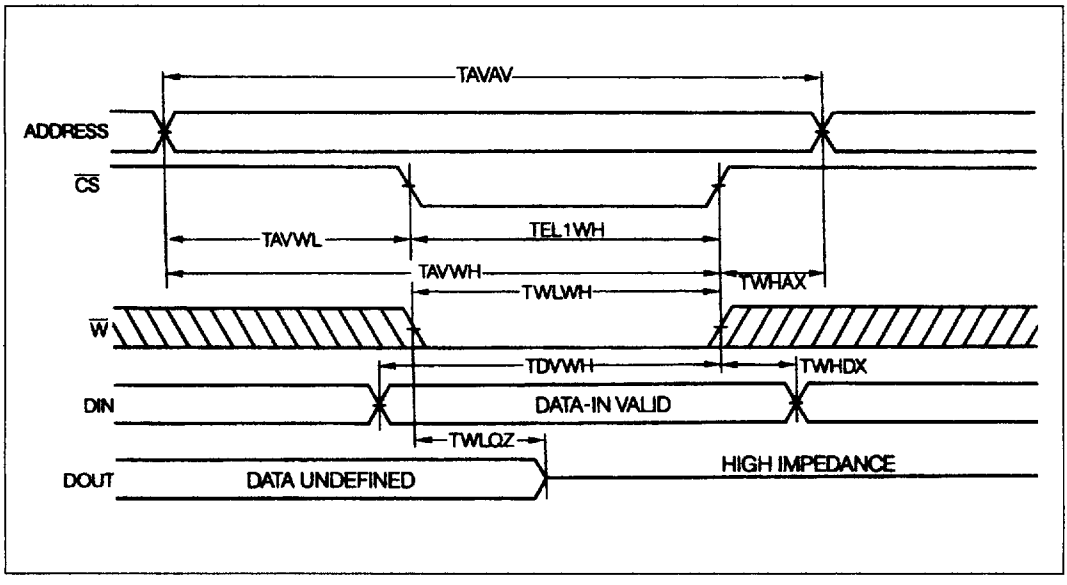
SYMBOL	PARAMETER (8)	65756 H	65756 K	65756 M	65756 N	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	40	50	ns	min
TDVWH	Data set-up time	15	17	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	40	50	ns	min
TWLQZ (7)	Write low to high Z	13	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	40	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (7)	Write high to low Z	3	3	3	3	ns	min

Notes : 7. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. All parameters tested only.
All parameters are screened during full speed functional test.
For subgroups 7 and 8 (functional test).
Tested at 1 MHz with VIL = 0V and VIH = 3V.
HM 65756 is verified with differents patterns unit for basic function, latch-up, maximum rating, data-retention.

WRITE CYCLE 1 : $\overline{W}$ CONTROLLED (note 9)



WRITE CYCLE 2 : $\overline{CS}$ CONTROLLED (note 9)



Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

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READ CYCLE :

SYMBOL	PARAMETER (8)	65756 H	65756 K	65756 M	65756 N	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	13	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	15	20	20	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	13	15	20	25	ns	min

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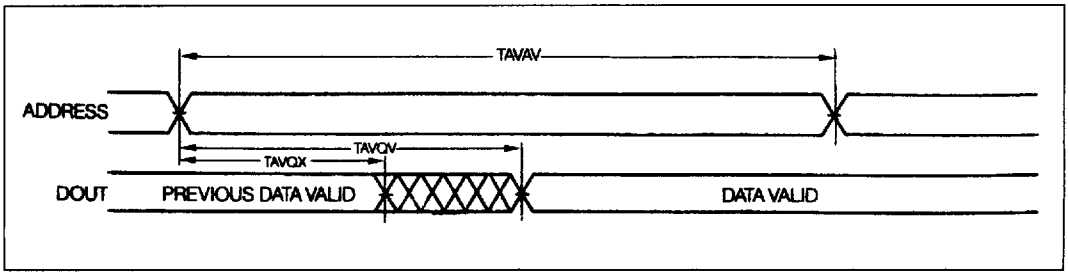
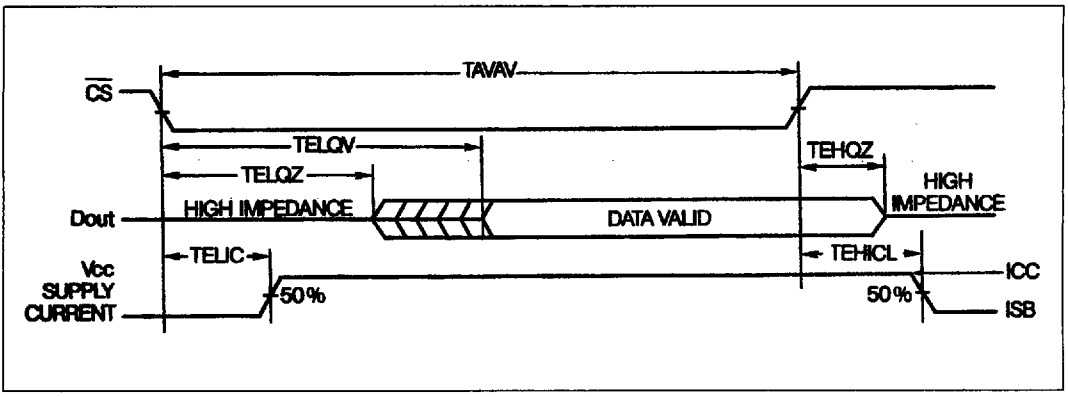
READ CYCLE 1 : (note 10, 11)

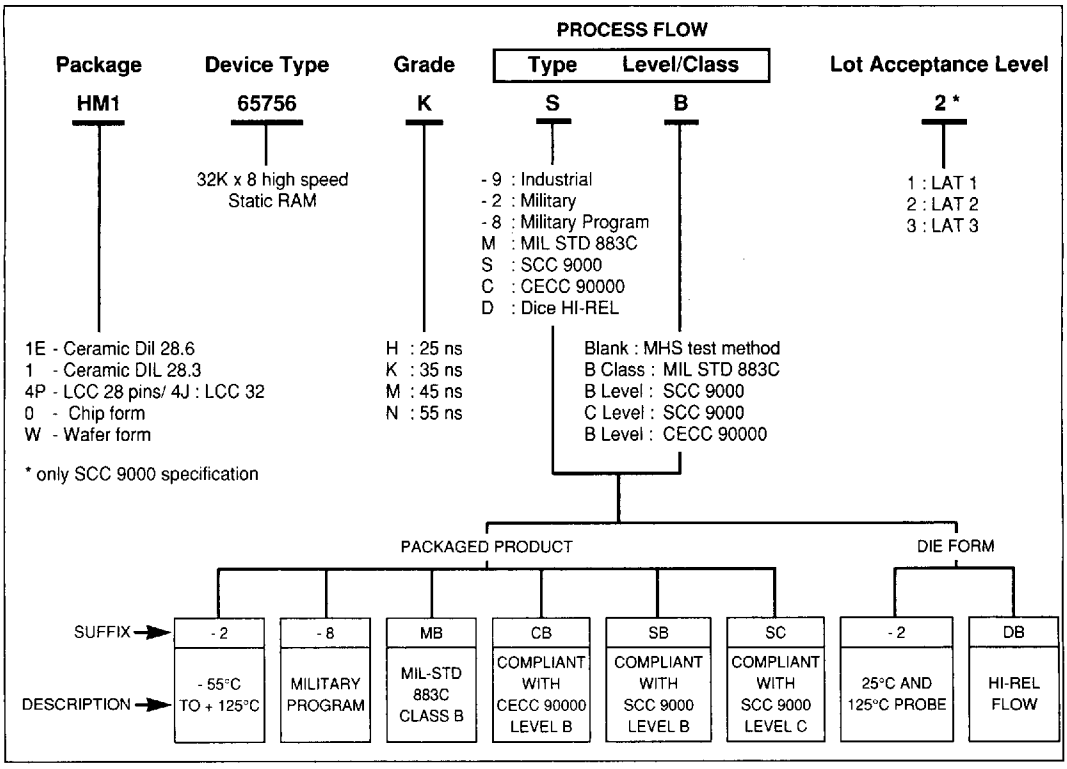


READ CYCLE 2 : (note 10, 12)



Notes : 10. $\overline{W}$ is high for read cycle.
11. $\overline{CS}$ and OE = VIL.
12. Address valid prior or coincident with $\overline{CS}$ low.

ORDERING INFORMATION



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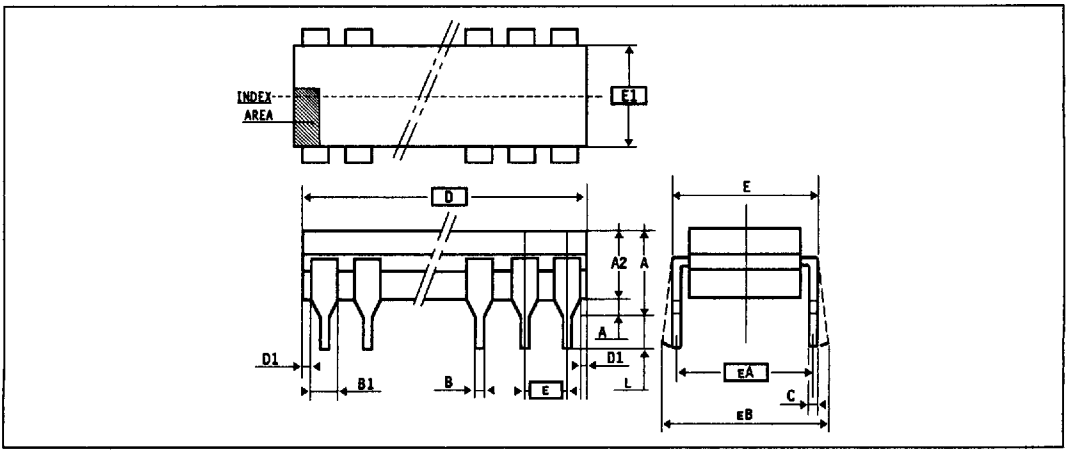
PACKAGE OUTLINES



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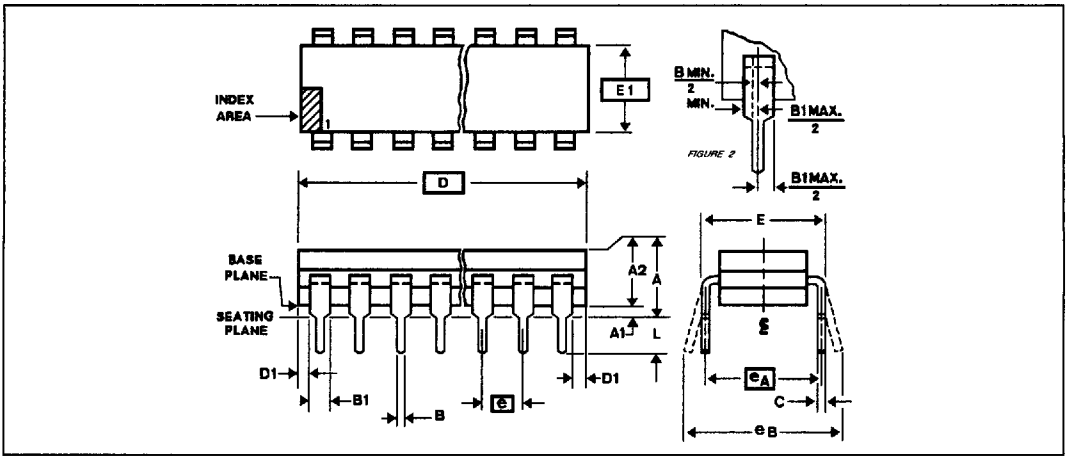
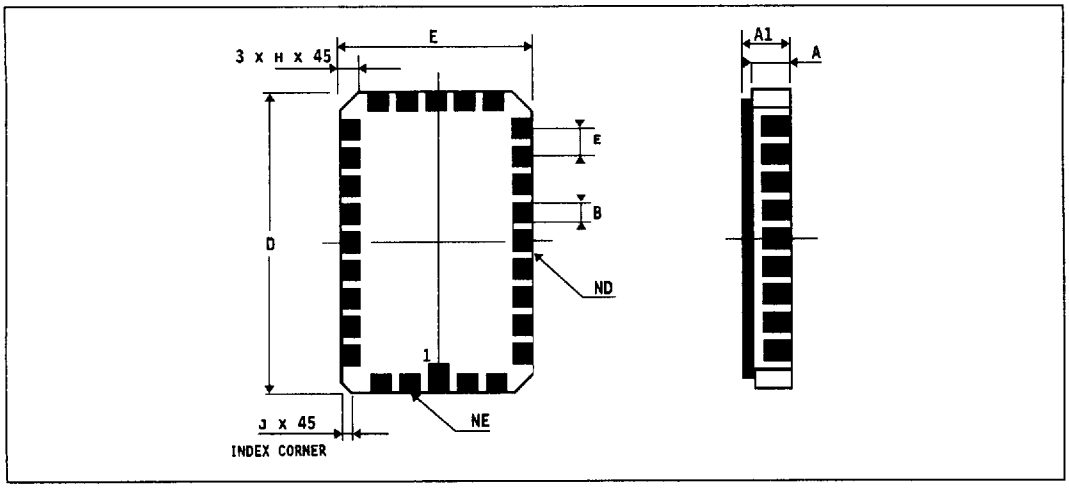
28 LEADS CERDIP .600

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	4.31	0.51	—	0.38	1.27	0.20	36.90	0.25	15.24	13.05	2.54	15.54	—	3.17
	MAX	5.71	1.52	4.57	0.51	1.78	0.38	38.90	—	15.75	13.66	BSC	BSC	17.78	5.08
INCHES	MIN	.170	.020	—	.014	.050	.008	1.452	.010	.600	.514	.100	.600	—	.125
	MAX	.225	.060	.180	.020	.070	.015	1.531	—	.620	.538	BSC	BSC	.700	.200



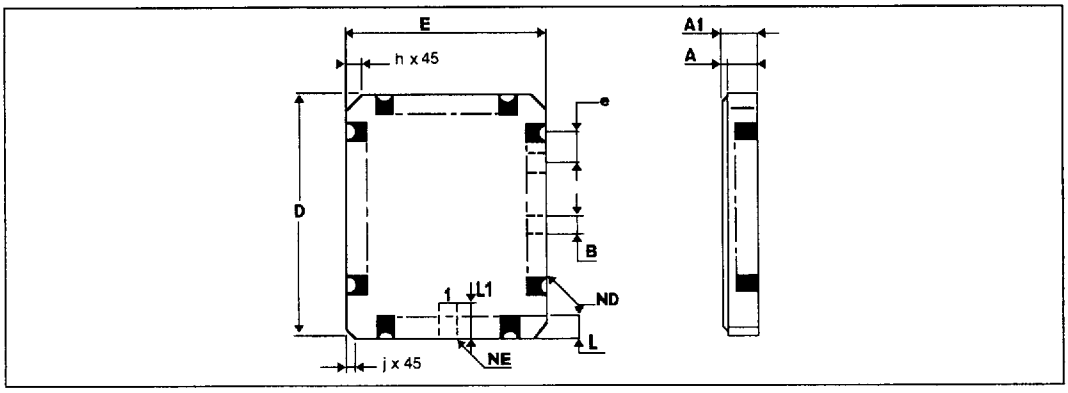
28 PINS CERDIP .300

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	—	0.38	2.92	0.36	1.14	0.20	36.58	0.13	7.62	6.10	2.54	7.62	—	3.05
	MAX	5.84	—	4.95	0.58	1.78	0.38	37.50	—	8.25	7.87	BSC	BSC	11.43	5.08
INCHES	MIN	—	.015	.115	.014	.045	.008	1.440	.005	.300	.240	.100	.300	—	.125
	MAX	.230	—	.195	.023	.070	.015	1.476	—	.325	.310	BSC	BSC	.450	.200



28 LDS .050 CENTER LEADLESS RECTANGULAR CHIP CARRIER

		A	A1	B	D	E	e	h	j	ND	NE
MM	MIN	1.37	1.62	0.56	13.81	8.74	1.27	0.64	0.38	9	5
	MAX	1.65	2.00	0.71	14.22	9.14	BSC	Ref	Ref		
INCHES	MIN	.054	.064	.022	.544	.344	.050	0.25	.015	9	5
	MAX	.065	.079	.028	.560	.360	BSC	Ref	Ref		



32 LDS .050 CENTER LEADLESS RECTANGULAR CHIP CARRIER.

		A	A1	B	D	E	e	h	j	L	L1	ND	NE
MM	MIN	1.37	1.62	0.635	13.81	11.30	1.27	1.016	0.51	1.14	1.8	9	7
	MAX	1.93	2.23	TYP	14.22	11.63	BSC			1.4	2.11		
INCHES	MIN	.054	.064	.025	.544	.445	.050	0.40	.020	.045	.077	9	7
	MAX	.076	.088	TYP	.560	.458	BSC			.055	.083		