HARRIS

HM-6551

256 x 4 CMOS RAM

Features

- Low Standby Power ..... 50μW Max.
- Low Operating Power ..... 20mW/MHz Max.
- Fast Access Time ..... 220ns Max.
- Data Retention Voltage ..... 2.0V Min.
- TTL Compatible In/Out
- High Output Drive - 1 TTL Load
- Internal Latched Chip Select
- High Noise Immunity
- On Chip Address Registers
- Latched Outputs
- Three-State Outputs
- Wide Operating Temperature Ranges:
  - ▸ HM-6551-5 ..... 0°C to +70°C
  - ▸ HM-6551-9 ..... -40°C to +85°C
  - ▸ HM-6551-8 ..... -55°C to +125°C

Description

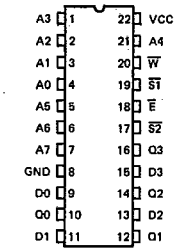
The HM-6551 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for addresses and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

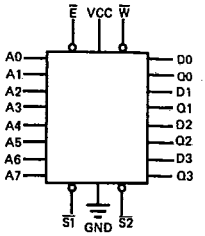
Pinout

TOP VIEW

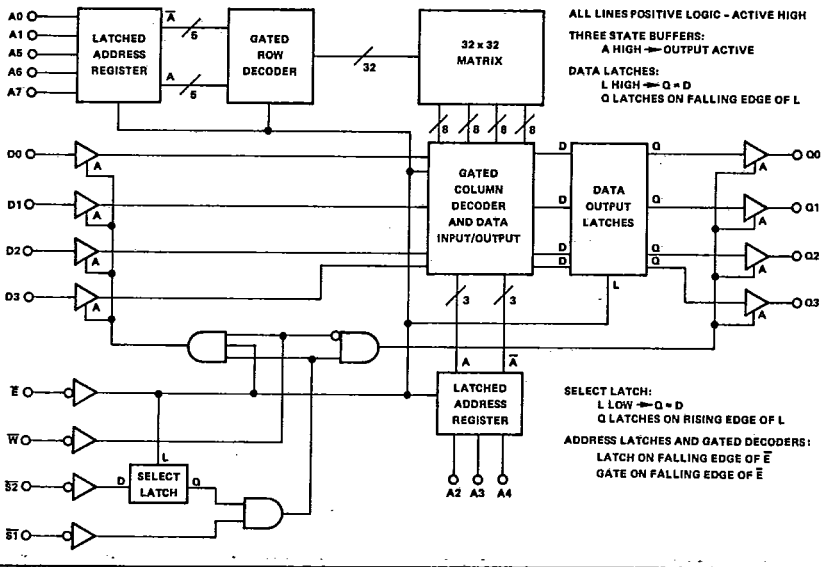


A-Address Input — W-Write Enable
E-Chip Enable — D-Data Input
S-Chip Select — Q-Data Output

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Specifications HM-6551B-8/HM-6551B-9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 15°C/W (CERDIP Package)
θ_{ja} ..... 60°C/W (CERDIP Package)
Gate Count ..... 1930 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6551B-9 ..... -40°C to +85°C
HM-6551B-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-6551B-9 -40°C to +85°C
T_A = HM-6551B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	10	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	10	µA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Specifications HM-6551B-8/HM-6551B-9

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6551B-9 -40°C to +85°C
T_A = HM-6551B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	220	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	220	ns	(Notes 1, 4)
(3) TS1LQX	Chip Select 1 Output Enable Time	5	130	ns	(Notes 2, 4)
(4) TWLQZ	Write Enable Output Disable Time	-	130	ns	(Notes 2, 4)
(5) TS1HQZ	Chip Select 1 Output Disable Time	-	130	ns	(Notes 2, 4)
(6) TELEH	Chip Enable Pulse Negative Width	220	-	ns	(Notes 1, 4)
(7) TEHEL	Chip Enable Pulse Positive Width	100	-	ns	(Notes 1, 4)
(8) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(9) TS2LEL	Chip Select 2 Setup Time	0	-	ns	(Notes 1, 4)
(10) TELAX	Address Hold Time	40	-	ns	(Notes 1, 4)
(11) TELS2X	Chip Select 2 Hold Time	40	-	ns	(Notes 1, 4)
(12) TDVWH	Data Setup Time	100	-	ns	(Notes 1, 4)
(13) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(14) TWLS1H	Chip Select 1 Write Pulse Setup Time	120	-	ns	(Notes 1, 4)
(15) TWLEH	Chip Enable Write Pulse Setup Time	120	-	ns	(Notes 1, 4)
(16) TS1LWH	Chip Select 1 Write Pulse Hold Time	120	-	ns	(Notes 1, 4)
(17) TELWH	Chip Enable Write Pulse Hold Time	120	-	ns	(Notes 1, 4)
(18) TWLWH	Write Enable Pulse Width	120	-	ns	(Notes 1, 4)
(19) TELEL	Read or Write Cycle Time	320	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 15°C/W (CERDIP Package)
θ_{ja} ..... 60°C/W (CERDIP Package)
Gate Count ..... 1930 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6551-9 ..... -40°C to +85°C
HM-6551-8 ..... -55°C to +125°C

D.C. Electrical Specifications

V_{CC} = 5V ± 10%; T_A = HM-6551-9 -40°C to +85°C
T_A = HM-6551-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	10	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	10	µA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6551-9 -40°C to +85°C
T_A = HM-6551-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	300	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	300	ns	(Notes 1, 4)
(3) TS1LQX	Chip Select 1 Output Enable Time	5	150	ns	(Notes 2, 4)
(4) TWLQZ	Write Enable Output Disable Time	-	150	ns	(Notes 2, 4)
(5) TS1HQZ	Chip Select 1 Output Disable Time	-	150	ns	(Notes 2, 4)
(6) TELEH	Chip Enable Pulse Negative Width	300	-	ns	(Notes 1, 4)
(7) TEHEL	Chip Enable Pulse Positive Width	100	-	ns	(Notes 1, 4)
(8) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(9) TS2LEL	Chip Select 2 Setup Time	0	-	ns	(Notes 1, 4)
(10) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(11) TELS2X	Chip Select 2 Hold Time	50	-	ns	(Notes 1, 4)
(12) TDVWH	Data Setup Time	150	-	ns	(Notes 1, 4)
(13) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(14) TWLS1H	Chip Select 1 Write Pulse Setup Time	180	-	ns	(Notes 1, 4)
(15) TWLEH	Chip Enable Write Pulse Setup Time	180	-	ns	(Notes 1, 4)
(16) TS1LWH	Chip Select 1 Write Pulse Hold Time	180	-	ns	(Notes 1, 4)
(17) TELWH	Chip Enable Write Pulse Hold Time	180	-	ns	(Notes 1, 4)
(18) TWLWH	Write Enable Pulse Width	180	-	ns	(Notes 1, 4)
(19) TELEL	Read or Write Cycle Time	400	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Specifications HM-6551-5

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 15°C/W (CERDIP Package)
θ_{ja} ..... 60°C/W (CERDIP Package)
Gate Count ..... 1930 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6551-5 ..... 0°C to +70°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6551-5 0°C to +70°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	100	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	100	µA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA
VOH	Output High Voltage	2.4	-	V	IO = -0.2mA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

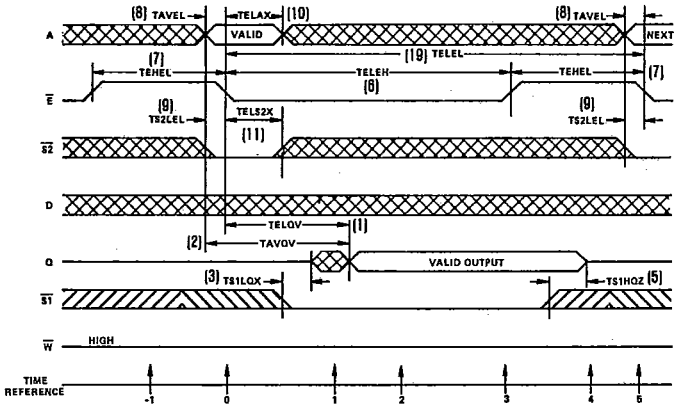
Specifications HM-6551-5

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6551-5 0°C to +70°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	350	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	360	ns	(Notes 1, 4)
(3) TS1LQX	Chip Select 1 Output Enable Time	5	180	ns	(Notes 2, 4)
(4) TWLQZ	Write Enable Output Disable Time	-	180	ns	(Notes 2, 4)
(5) TS1HQZ	Chip Select 1 Output Disable Time	-	180	ns	(Notes 2, 4)
(6) TELEH	Chip Enable Pulse Negative Width	350	-	ns	(Notes 1, 4)
(7) TEHEL	Chip Enable Pulse Positive Width	150	-	ns	(Notes 1, 4)
(8) TAVEL	Address Setup Time	10	-	ns	(Notes 1, 4)
(9) TS2LEL	Chip Select 2 Setup Time	10	-	ns	(Notes 1, 4)
(10) TELAX	Address Hold Time	70	-	ns	(Notes 1, 4)
(11) TELS2X	Chip Select 2 Hold Time	70	-	ns	(Notes 1, 4)
(12) TDVWH	Data Setup Time	170	-	ns	(Notes 1, 4)
(13) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(14) TWLS1H	Chip Select 1 Write Pulse Setup Time	210	-	ns	(Notes 1, 4)
(15) TWLEH	Chip Enable Write Pulse Setup Time	210	-	ns	(Notes 1, 4)
(16) TS1LWH	Chip Select 1 Write Pulse Hold Time	210	-	ns	(Notes 1, 4)
(17) TELWH	Chip Enable Write Pulse Hold Time	210	-	ns	(Notes 1, 4)
(18) TWLWH	Write Enable Pulse Width	210	-	ns	(Notes 1, 4)
(19) TELEL	Read or Write Cycle Time	500	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Read Cycle



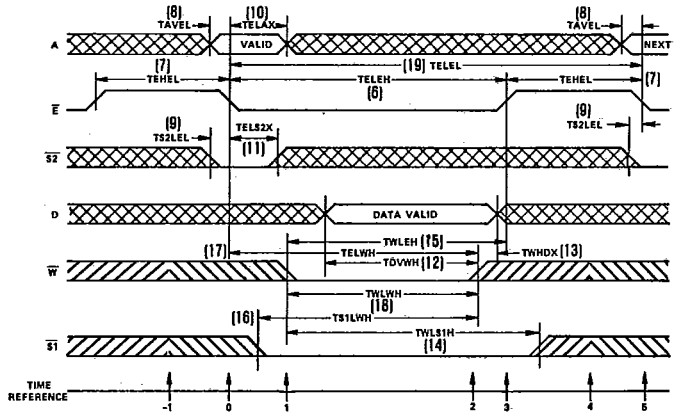
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↓	X	L	H	V	X	Z	Addresses and $\overline{S2}$ are Latched, Cycle Begins
1	L	L	X	H	X	X	X	Output Enabled But Undefined
2	L	L	X	H	X	X	V	Data Output Valid
3	↑	L	X	H	X	X	V	Outputs Latched, Valid Data, $\overline{S2}$ Unlatches
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	L	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The HM-6551 Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on chip registers providing the minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HM-6551 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Also on the rising edge of $\overline{E}$, $\overline{S2}$ unlatches and controls the outputs along with $\overline{S1}$. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↓	X	L	X	V	X	Z	Cycle Begins, Addresses and $\overline{S2}$ are Latched
1	L	L	X	↓	X	X	Z	Write Period Begins
2	L	L	X	↑	X	V	Z	Data In is Written
3	↑	X	X	H	X	X	Z	Write is Completed
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	L	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$.

By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HM-6551 may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.