

Description

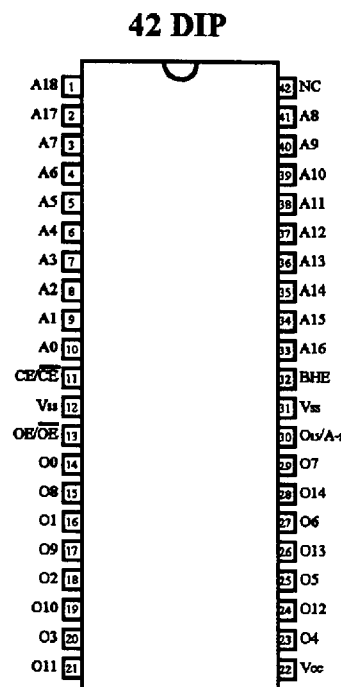
The GM23C8100A high performance read only memory is organized as 1,048,576 x 8 bit (Byte Mode) or as 524,288 x 16 bit (Word Mode) followed by BHE mode select. The GM23C8100A offers automatic power down controlled by the mask programmed CE or $\overline{CE}$ input. The low power feature allows the battery operation. The large size of 8M bit memory density is ideal for character generator, data or program memory in microprocessor application. This ROM is packaged in 42 pin DIP.

Features

- Switchable Organization
Byte Mode : 1,048,576 x 8 bit
Word Mode : 524,288 x 16 bit
- Single + 5V Supply
- Access Time : 120/150ns (Max)
- Operating current : 50mA (Max)
- Standby current : 50 μ A (Max)
- TTL-compatible inputs and outputs
- Polarity programmable chip enable and out enable pin
- Byte or Word switchable by BHE pin
(BHE can be switched on the fly or a DC signal)
- 3-State outputs for wired-OR expansion
- Fully static operation
- Package :

GM23C8100A : 42 Pin Plastic DIP (600 mil)

Pin Configuration



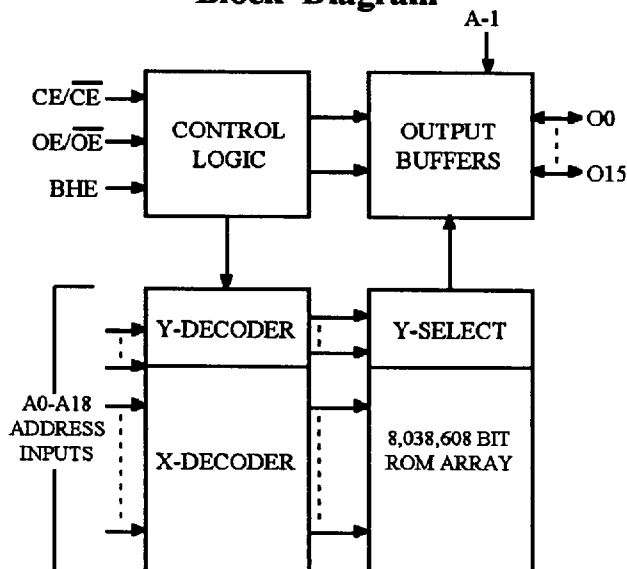
(Top View)

Pin Description

Pin	Function
A0-A18	Address Inputs
O0-O14	Data Outputs
O15/A-1	Output O15 (Word Mode)/ LSB Address (Byte Mode)
BHE	Word/Byte Selection
CE/ $\overline{CE}$ *	Chip Enable Input
OE/ $\overline{OE}$ *	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground
NC	No Connection

*User Selectable Polarity.

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Operating Temperature	-10 ~ 80	°C
T _{STG}	Storage Temperature	-65 ~ 150	°C
V _{CC}	Supply Voltage to Ground Potential	-0.5 ~ V _{CC} + 0.5	V
V _{OUT}	Output Voltage	-0.5 ~ V _{CC} + 0.5	V
V _{IN}	Input Voltage	-0.5 ~ 7.0	V

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (V_{CC} = 5.0V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	V

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	I _{OH} = -1mA	2.4			V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA			0.4	V
I _{IL}	Input Leakage Current	V _{IN} = 0V to V _{CC}			± 10	μA
I _{OL}	Output Leakage Current	V _{OUT} = 0V to V _{CC}			± 10	μA
I _{CC}	Operating Supply Current (f = 6.7 MHz)	$\overline{CE} = V_{IL}$, CE = V _{IH}			50	mA
I _{SB1}	Standby Current (TTL)	$\overline{CE} = V_{IH}$, all Output Open			1	mA
I _{SB2}	Standby Current (CMOS)	$\overline{CE} = V_{CC}$, all Output Open			50	μA

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Min	Max	Unit
C _I	Input Capacitance	V _{IN} = 0V		10	pF
C _O	Output Capacitance	V _{OUT} = 0V		10	pF

Note : Capacitance is periodically sampled and not 100% tested.

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Mode Selection

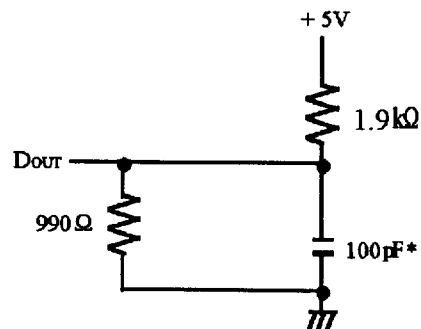
Mode	CE/ $\overline{\text{CE}}$	OE/ $\overline{\text{OE}}$	BHE	O0~07	O8~014	O15/A-1	Power
Standby	L/H	X	X	High-Z			Standby
16 Bit Operating	H/L	H/L	H	Data Out			Active
8 Bit Operating			L	Data Out (Lower 8 Bit)	High-Z	L	
				Data Out (Upper 8 Bit)		H	
Output Disable		L/H	X	High-Z			

AC Operating Characteristics ($V_{CC} = 5.0V \pm 10\%$, $T_A = 0 \sim 70^\circ\text{C}$)

Symbol	Parameter	GM23C8100A-12		GM23C8100A-15		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	120		150		ns
t_{ACE}	Chip Enable Access Time		120		150	ns
t_{AA}	Address Access Time		120		150	ns
t_{AOE}	Output Enable Access Time		60		70	ns
t_{OH}	Output Hold From Address Change	10		10		ns
t_{OHZ} t_{CHZ}	Output or Chip Disable to Output High-Z		50		60	ns
t_{OLZ} t_{CLZ}	Output or Chip Enable to Output Low-Z	10		10		ns

AC Test Condition

Input Pulse Level	0.4V to 2.4V
Input Rise and Fall Time	10ns
Input and Output Timing Level	0.8V to 2.0V
Output Load	See Fig. 1



*Including scope and jig.

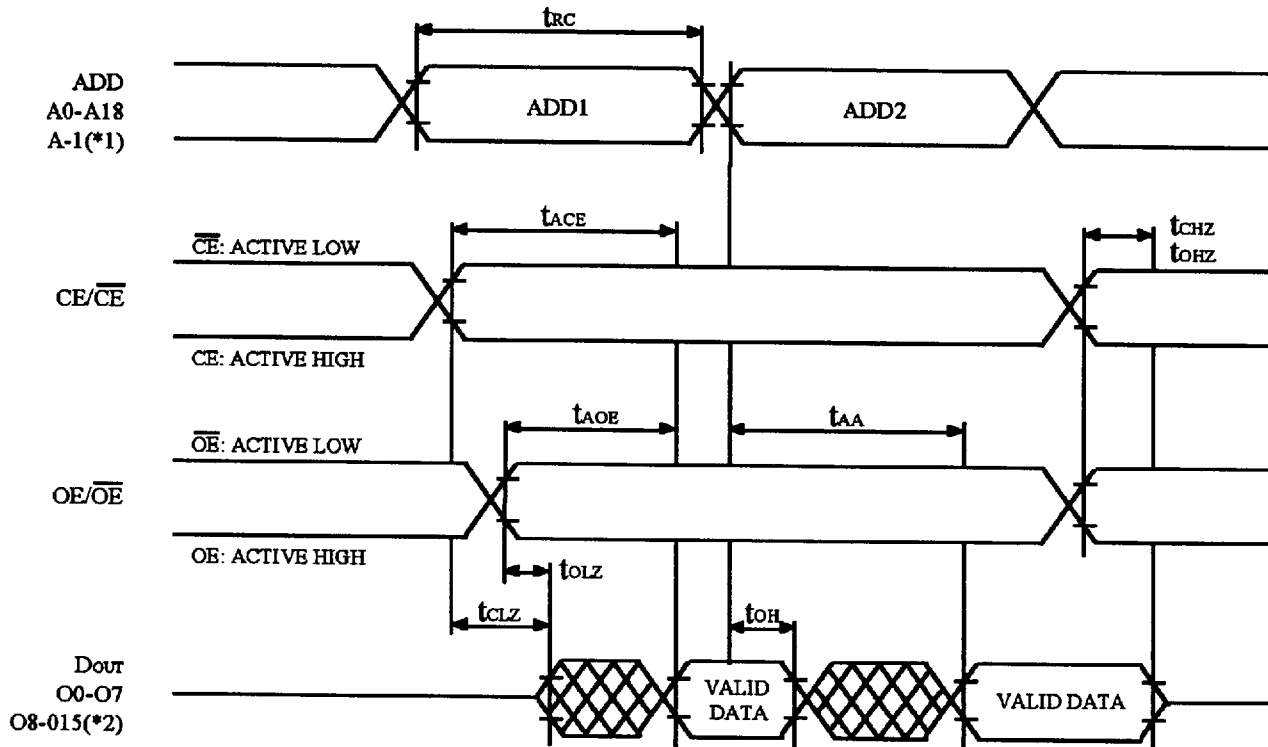
Fig. 1 Output Load Circuit



Timing Waveforms

Read

Word Mode (BHE= V_{IH}) / Byte Mode (BHE= V_{IL})



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})

(*2) Word Mode only. (BHE = V_{IH})

42 DIP

