National Semiconductor Corporation

PRELIMINARY

DM54ALS192/DM74ALS192/DM54ALS193/DM74ALS193 Synchronous Four-Bit Up/Down Counters (Dual Clock with Clear)

General Description

The 'ALS192 and 'ALS193 are synchronous, reversible up/down counters. The 'ALS192 is a 4-bit decade counter and the 'ALS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high level transition of either count (clock) input (up or down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

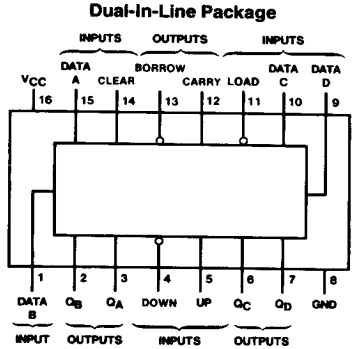
These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterparts
- Improved AC performance over Schottky and low power Schottky counterparts
- Look ahead circuitry enhances cascaded counters
- Fully synchronous in count mode
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear

Connection Diagram

Dual-In-Line Package



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Order Number DM54ALS192J, 193J, DM74ALS192M, 193M or DM74ALS192N, 193N
See NS Package Number J16A, M16A or N16A

This document contains information on a device under development. National Semiconductor Corporation reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0 to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS192, 193			DM74ALS192, 193			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency	'ALS192	0		20	0		25	MHz
		'ALS193	0		25	0		30	MHz
t_W	Pulse Duration	CLR High	10			10			ns
		$\overline{LOAD}$ Low	25			20			ns
		UP or DOWN High or Low 'ALS192	25			20			ns
		UP or DOWN High or Low 'ALS193	30			16.5			ns
t_{SU}	Setup Time	Data before $\overline{LOAD}$ ↑	25			20			ns
		CLR Inactive before UP ↑ or DOWN ↑	20			20			ns
		$\overline{LOAD}$ Inactive before UP ↑ or DOWN ↑	20			20			ns
		UP High before DOWN ↑	17			17			ns
		DOWN High before UP ↑	15			15			ns
t_H	Hold Time	Data after $\overline{LOAD}$ ↑	5			5			ns
		UP High after DOWN ↑	0			0			ns
		DOWN High after UP ↑	0			0			ns
T_A	Operating Free Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions		DM74ALS192, 193			Units
				Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5V	74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	UP, DOWN			−0.2	mA
			All Others			−0.1	mA

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Electrical Characteristics over recommended operating free air temperature range (Continued)

Symbol	Parameter	Conditions	DM74ALS192, 193			Units
			Min	Typ (Note 1)	Max	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V (Note 2)	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 3)		12	22	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Note 3: I_{CC} is measured with the clear and load inputs grounded, and all other inputs at 4.5V.

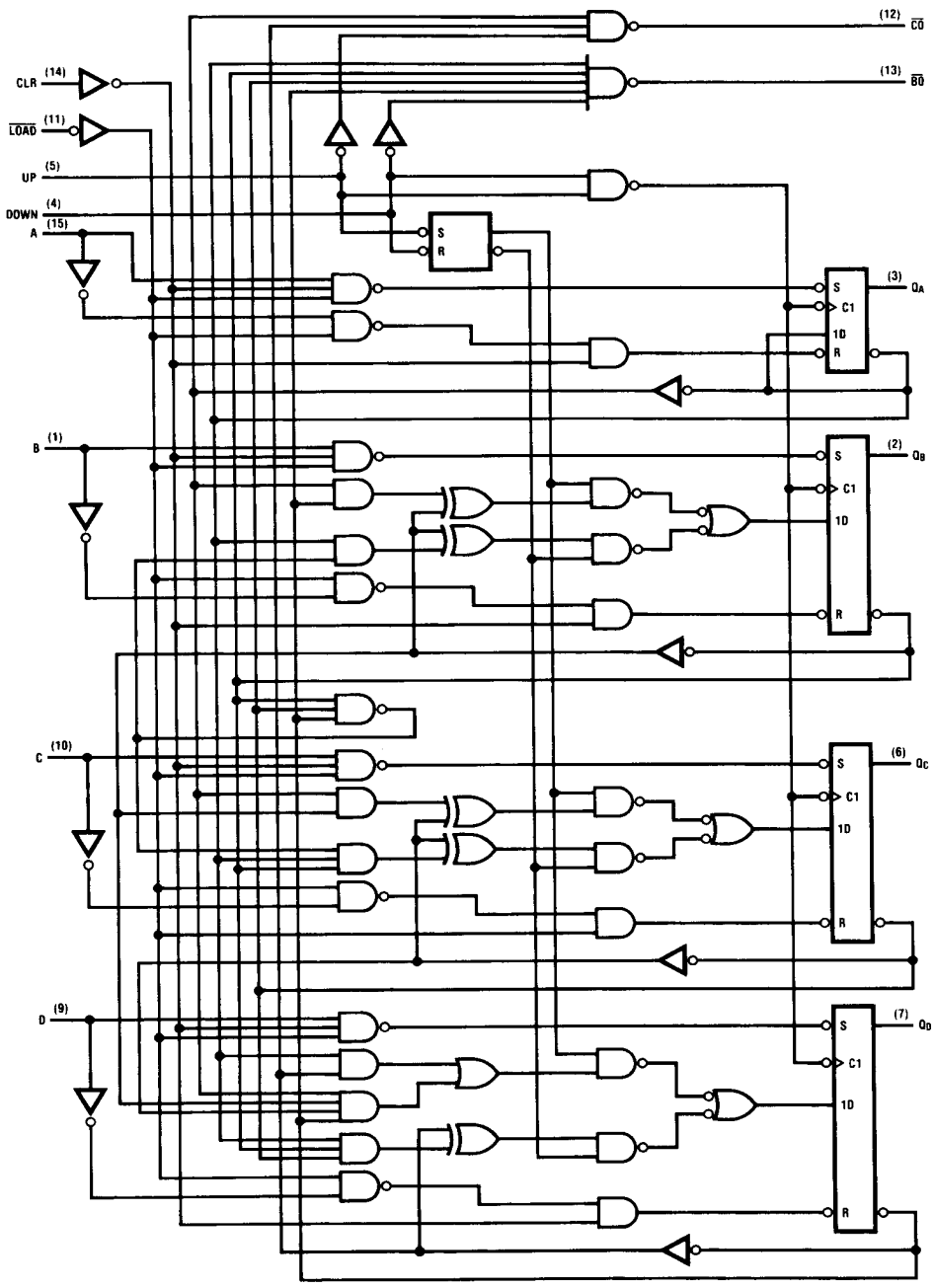
Switching Characteristics (Note 4)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM54ALS192, 193		DM74ALS192, 193		Units
					Min	Max	Min	Max	
f_{MAX}	'ALS192	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max			20		25		MHz
	'ALS193				25		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Up	C0	3	20	4	16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Up	C0	3	21	5	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Down	B0	4	20	4	16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Down	B0	5	22	5	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Up or Down	Any Q	4	27	4	19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Up or Down	Any Q	4	23	4	17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{LOAD}$	Any Q	8	38	8	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{LOAD}$	Any Q	8	37	8	28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		CLR	Any Q	5	20	5	17	ns

Note 4: See Section 1 for test waveforms and output load.

Logic Diagrams

'ALS192



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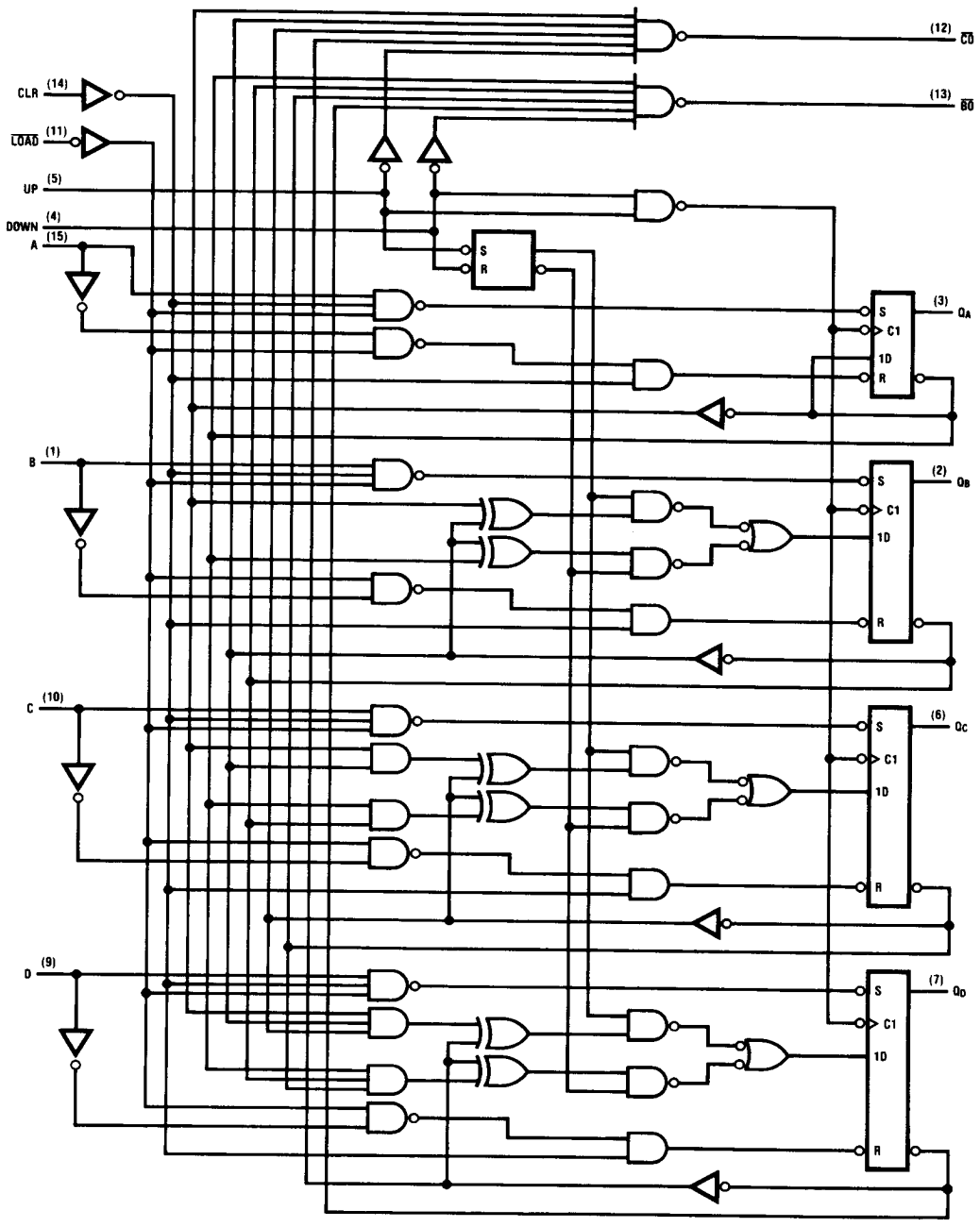
Pin numbers shown are for J and N packages.

Logic Diagrams (Continued)

'ALS193



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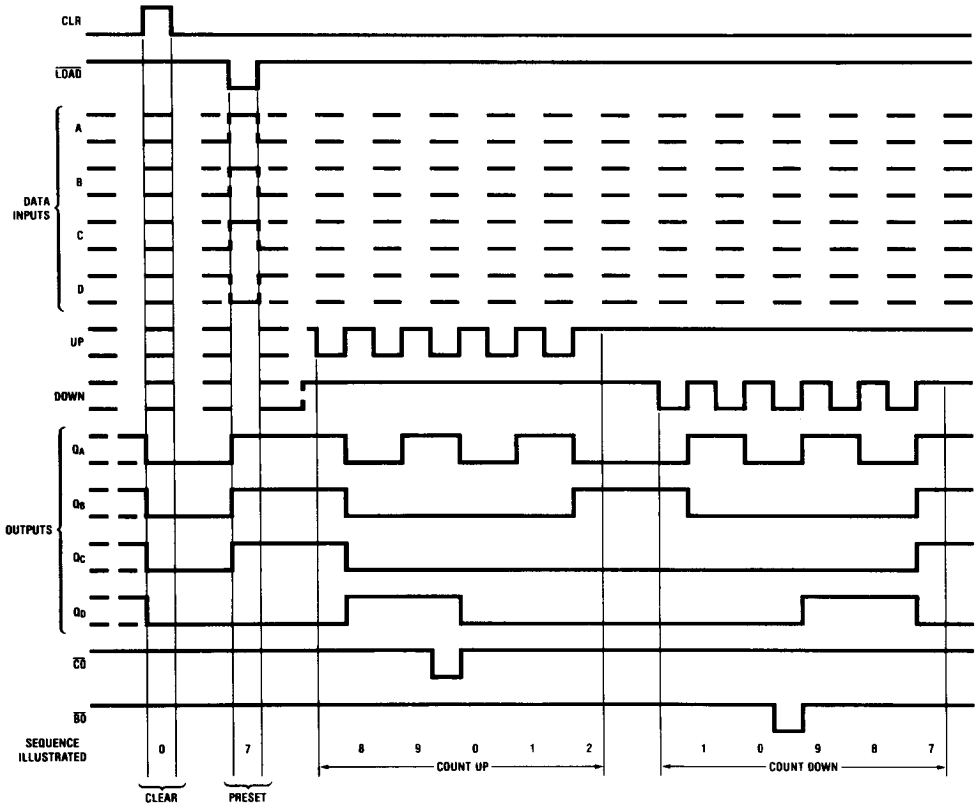
Pin numbers shown are for J and N packages.

Timing Diagrams

'ALS192 Typical Clear, Load and Count Sequences



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Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

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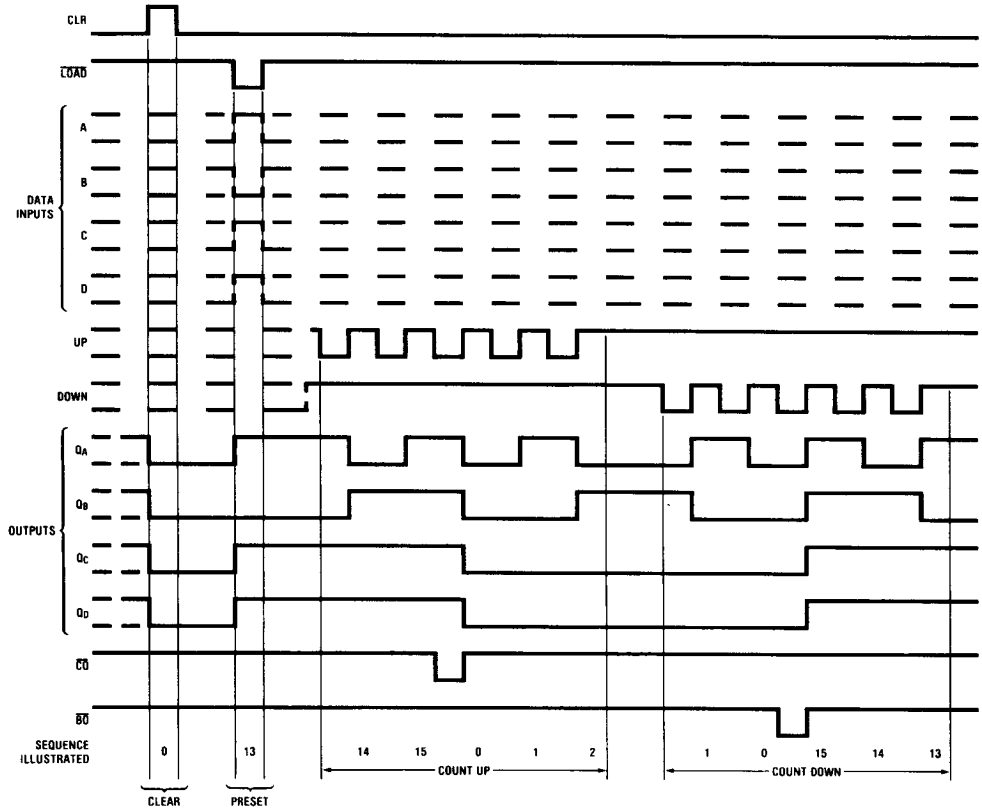
Timing Diagrams (Continued)

'ALS193 Typical Clear, Load and Count Sequences



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Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.