

1 chip GPS LSI

Description

The CXD2931R-9/GA-9 is a dedicated LSI for the GPS (Global Positioning System) satellite-based position measurement system.

This LSI contains a 32-bit RISC CPU, 2M-bit MASK ROM, RAM, UART, timer, and others.

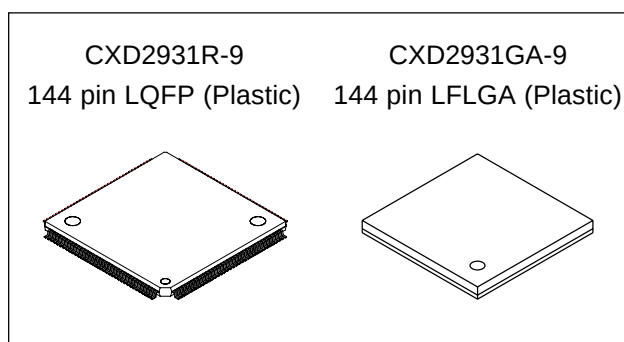
This LSI, used together with the RF LSI (CXA1951AQ), enables the configuration of a 2-chip system capable of measuring its position anywhere on the globe.

Features

- 16-channel GPS receiver capable of simultaneously receiving 16 satellites
- Supports differential GPS
 - Comforms to RTCM SC-104 Ver. 2.1
 - Supports DARC
- All-in-view measurement
- 2-satellite measurement
- Timer supporting GPS time
- High performance 32-bit RISC CPU
- 256K-byte program ROM
- 36K-byte RAM
- 3-channel UART
 - Baud rate generator
 - Supports 1.2K, 2.4K, 4.8K, 9.6K, 19.2K and 38.4K baud
 - Supports 1/2/4-byte buffer mode
- 23-bit general-purpose I/O port capable of defining input/output independently for each bit
- 8-bit successive approximation system A/D converter

Structure

Silicon gate CMOS IC



Absolute Maximum Ratings

• Supply voltage	V_{DD}	$V_{SS} - 0.5$ to 4.6	V
• Input voltage	V_I	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
• Output voltage	V_O	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
• Operating temperature	T_{opr}	-40 to $+85$	°C
• Storage temperature	T_{stg}	-50 to $+150$	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
• Operating temperature	T_{opr}	-40 to $+85$	°C

Input/Output Pin Capacitance

• Input capacitance	C_{IN}	9 (Max.)	pF
• Output capacitance	C_{OUT}	11 (Max.)	pF
• I/O capacitance	$C_{I/O}$	11 (Max.)	pF

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Performance

- 16-channel GPS receiver
- High performance 32-bit RISC CPU
- Receiver frequency: 1575.42MHz (L1 band, CA code)
- Reception sensitivity

Tracking sensitivity: -145dBm (typ.) when using the antenna of 25dBi, NF = 2dB and the RF amplifier with the 25dB gain

* Reference data using the Sony's reference board.
This value is not guaranteed, depending on the conditions.
- Time to First Fix (time until initial measurement after power-on)

Cold Start (without both ephemeris and almanac): 27 to 58s
Warm Start (without ephemeris with almanac): 23 to 45s
Hot Start (with both ephemeris and almanac): 6 to 17s

* Reference data with elevation angle of 5° or more and no interception environment on Nov., 2001.
Positioning time with 90% possibility.
These values are not guaranteed, depending on the conditions.
- Positioning accuracy

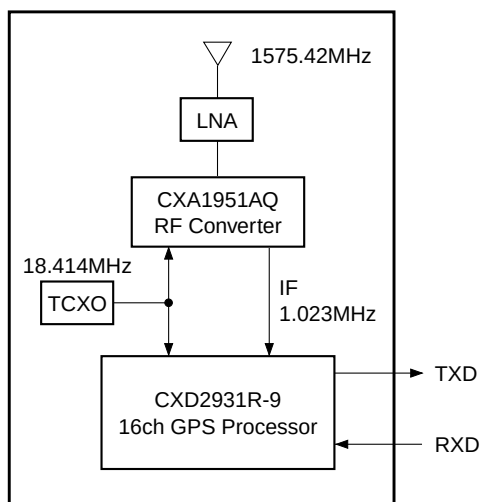
2DRMS: approx. 12m

* Reference data with elevation angle of 5° or more and no interception environment.
This value is not guaranteed, depending on the conditions.
- Measurement data update time

1s
- Interface format

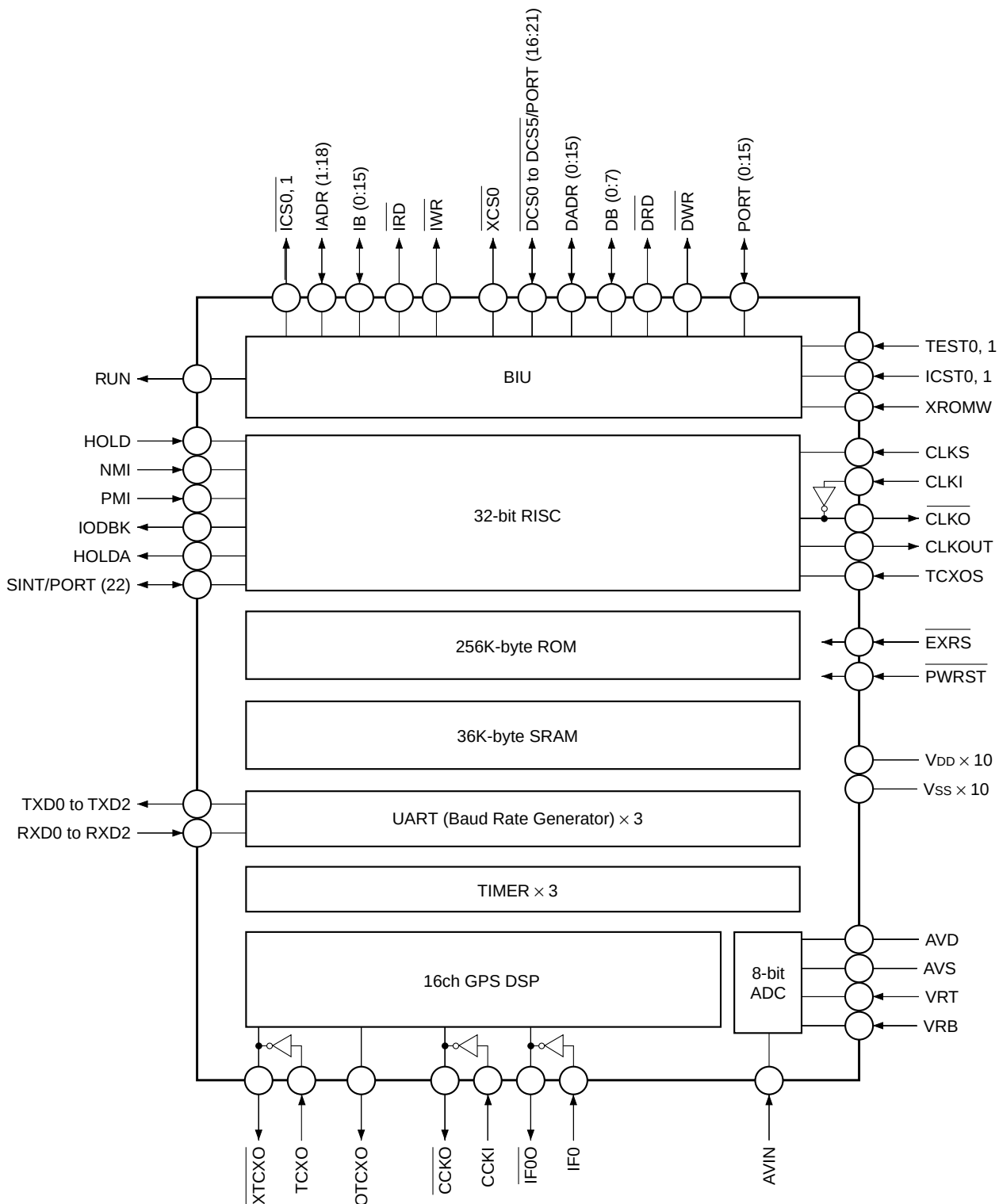
NMEA0183 (4800bps)
Sony Binary (9600bps)
- Communication method

Start-stop synchronization
- All-in-view

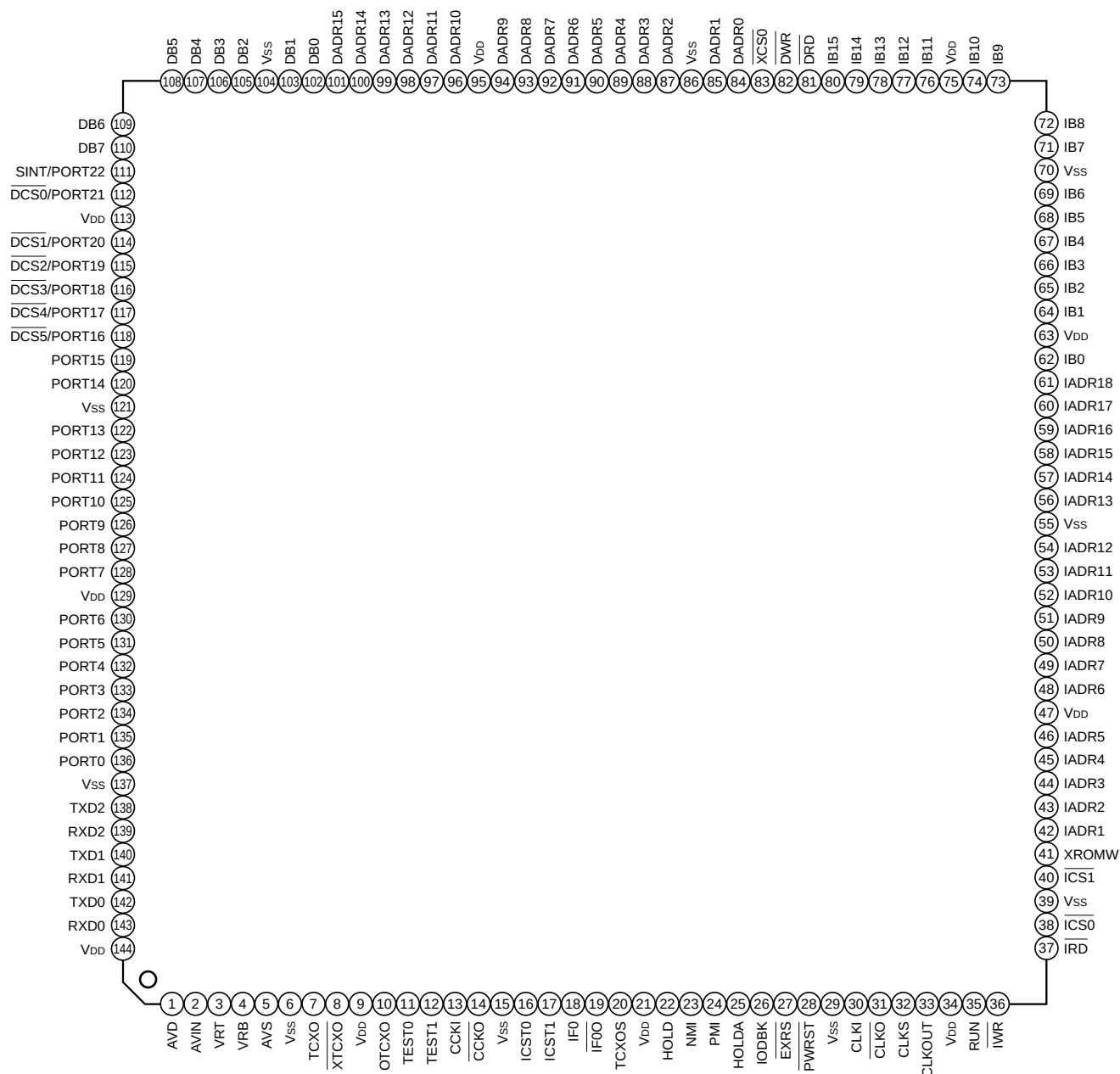


GPS receiver system block diagram using the CXD2931R-9

Block Diagram



Pin Configuration (CXD2931R-9)



Pin Configuration (CXD2931GA-9)

(70)	(67)	(64)	(62)	(59)	(58)	(55)	(54)	(51)	(50)	(47)	(45)	(42)	(39)	(34)	R
V _{SS}	IB4	IB1	IB0	IADR16	IADR15	V _{SS}	IADR12	IADR9	IADR8	V _{DD}	IADR4	IADR1	V _{SS}	V _{DD}	
(75)	(71)	(68)	(66)	(63)	(60)	(56)	(53)	(49)	(46)	(43)	(41)	(38)	(35)	(31)	P
V _{DD}	IB7	IB5	IB3	V _{DD}	IADR17	IADR13	IADR11	IADR7	IADR5	IADR2	XROMW	ICS0	RUN	CLKO	
(78)	(74)	(72)	(69)	(65)	(61)	(57)	(52)	(48)	(44)	(40)	(37)	(36)	(32)	(28)	N
IB13	IB10	IB8	IB6	IB2	IADR18	IADR14	IADR10	IADR6	IADR3	ICS1	IRD	IWR	CLKS	PWRST	
(81)	(77)	(73)										(33)	(30)	(26)	M
DRD	IB12	IB9										CLKOUT	CLKI	IODBK	
(83)	(79)	(76)										(29)	(27)	(23)	L
XCS0	IB14	IB11										V _{SS}	EXRS	NMI	
(86)	(82)	(80)										(25)	(24)	(22)	K
V _{SS}	DWR	IB15										HOLDA	PMI	HOLD	
(87)	(85)	(84)										(21)	(20)	(19)	J
DADR2	DADR1	DADR0										V _{DD}	TCXOS	IF00	
(90)	(89)	(88)										(16)	(17)	(18)	H
DADR5	DADR4	DADR3										ICST0	ICST1	IF0	
(91)	(92)	(93)										(12)	(13)	(15)	G
DADR6	DADR7	DADR8										TEST1	CCKI	V _{SS}	
(94)	(96)	(97)										(8)	(10)	(14)	F
DADR9	DADR10	DADR11										XTCXO	OTCXO	CCKO	
(95)	(99)	(101)										(4)	(7)	(11)	E
V _{DD}	DADR13	DADR15										VRB	TCXO	TEST0	
(98)	(102)	(105)										(1)	(5)	(9)	D
DADR12	DB0	DB2										AVD	AVS	V _{DD}	
(100)	(104)	(108)	(109)	(112)	(116)	(120)	(124)	(129)	(133)	(137)	(141)	(144)	(2)	(6)	C
DADR14	V _{SS}	DB5	DB6	DCS0/ PORT21	DCS3/ PORT18	PORT14	PORT11	V _{DD}	PORT3	V _{SS}	RXD1	V _{DD}	AVIN	V _{SS}	
(103)	(107)	(110)	(113)	(115)	(118)	(121)	(125)	(128)	(132)	(135)	(138)	(140)	(143)	(3)	B
DB1	DB4	DB7	V _{DD}	DCS2/ PORT19	DCS5/ PORT16	V _{SS}	PORT10	PORT7	PORT4	PORT1	TXD2	TXD1	RXD0	VRT	
(106)	(111)	(114)	(117)	(119)	(122)	(123)	(126)	(127)	(130)	(131)	(134)	(136)	(139)	(142)	A
DB3	SINT/ PORT22	DCS1/ PORT20	DCS4/ PORT17	PORT15	PORT13	PORT12	PORT9	PORT8	PORT6	PORT5	PORT2	PORT0	RXD2	TXD0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Pin Configuration

Pin No.	Symbol	I/O	Description
1	AVD	—	A/D converter power supply.
2	AVIN	I	Analog input.
3	VRT	I	Reference input.
4	VRB	I	
5	AVS	—	A/D converter GND.
6	Vss	—	GND
7	TCXO	I	TCXO binary conversion circuit/crystal oscillator.
8	$\overline{\text{XTCXO}}$	O	
9	V _{DD}	—	Power supply.
10	OTCXO	O	TCXO clock output.
11	TEST0	I	Test. (Low level fixed)
12	TEST1	I	
13	CCKI	I	Timer oscillation. (32.768kHz $\pm$ 100ppm)
14	$\overline{\text{CCKO}}$	O	
15	Vss	—	GND
16	ICST0	I	Test. (Low level fixed)
17	ICST1	I	
18	IF0	I	IF signal binary conversion circuit.
19	IF0O	O	
20	TCXOS	I	TCXO select. (Low: TCXO/2, High: TCXO through)
21	V _{DD}	—	Power supply.
22	HOLD	I	Hold input signal. (High: Hold)
23	NMI	I	Non maskable interrupt.
24	PMI	I	Program maskable interrupt.
25	HOLDA	O	Hold acknowledge signal.
26	IIOBK	O	Break signal for debugging.
27	EXRS	I	Reset input signal.
28	PWRST	I	Connect to main power supply. Leave open during backup.
29	Vss	—	GND
30	CLKI	I	CPU clock oscillation circuit.
31	$\overline{\text{CLKO}}$	O	
32	CLKS	I	CPU clock select signal. (Low: TCXO, High: CLKI)
33	CLKOUT	O	CPU clock output.
34	V _{DD}	—	Power supply.
35	RUN	O	Signal indicating CPU operating status.
36	IWR	O	Write signal for external expansion memory.
37	IRD	O	Read signal for external expansion memory.

Pin No.	Symbol	I/O	Description
38	ICS0	O	Chip select 0 for external expansion memory.
39	Vss	—	GND
40	ICS1	O	Chip select 1 for external expansion memory.
41	XROMW	I	Wait signal for external expansion memory. (High: Wait)
42	IADR1	I/O	(LSB) Address signal for external expansion memory.
43	IADR2	I/O	
44	IADR3	I/O	
45	IADR4	I/O	
46	IADR5	I/O	
47	V _{DD}	—	Power supply.
48	IADR6	I/O	Address signal for external expansion memory.
49	IADR7	I/O	
50	IADR8	I/O	
51	IADR9	I/O	
52	IADR10	I/O	
53	IADR11	I/O	
54	IADR12	I/O	
55	Vss	—	GND
56	IADR13	I/O	Address signal for external expansion memory.
57	IADR14	I/O	
58	IADR15	I/O	
59	IADR16	I/O	
60	IADR17	I/O	
61	IADR18	I/O	(MSB)
62	IB0	I/O	(LSB) Data bus I/O for external expansion memory.
63	V _{DD}	—	Power supply.
64	IB1	I/O	Data bus I/O for external expansion memory.
65	IB2	I/O	
66	IB3	I/O	
67	IB4	I/O	
68	IB5	I/O	
69	IB6	I/O	
70	Vss	—	GND
71	IB7	I/O	Data bus I/O for external expansion memory.
72	IB8	I/O	
73	IB9	I/O	
74	IB10	I/O	

Pin No.	Symbol	I/O	Description
75	V _{DD}	—	Power supply.
76	IB11	I/O	Data bus I/O for external expansion memory. (MSB)
77	IB12	I/O	
78	IB13	I/O	
79	IB14	I/O	
80	IB15	I/O	
81	DRD	O	Read signal for external expansion data memory.
82	DWR	O	Write signal for external expansion data memory.
83	XCS0	O	Chip select signal for external expansion data memory.
84	DADR0	I/O	(LSB) Address signal for external expansion data memory.
85	DADR1	I/O	
86	V _{SS}	—	GND
87	DADR2	I/O	Address signal for external expansion data memory.
88	DADR3	I/O	
89	DADR4	I/O	
90	DADR5	I/O	
91	DADR6	I/O	
92	DADR7	I/O	
93	DADR8	I/O	
94	DADR9	I/O	
95	V _{DD}	—	Power supply.
96	DADR10	I/O	Address signal for external expansion data memory. (MSB)
97	DADR11	I/O	
98	DADR12	I/O	
99	DADR13	I/O	
100	DADR14	I/O	
101	DADR15	I/O	(MSB)
102	DB0	I/O	(LSB)
103	DB1	I/O	Data bus I/O for external expansion data memory.
104	V _{SS}	—	GND
105	DB2	I/O	Data bus I/O for external expansion data memory. (MSB)
106	DB3	I/O	
107	DB4	I/O	
108	DB5	I/O	
109	DB6	I/O	
110	DB7	I/O	(MSB)

Pin No.	Symbol	I/O	Description
111	SINT/PORT22	I/O	External interrupt input signal/general-purpose I/O port. This pin can be used as a general-purpose I/O port according to the internal registers.
112	$\overline{\text{DCS0}}$ /PORT21	I/O	Chip select for external expansion data memory/general-purpose I/O port. This pin can be used as a general-purpose I/O port according to the internal registers.
113	V _{DD}	—	Power supply.
114	$\overline{\text{DCS1}}$ /PORT20	I/O	Chip select for external expansion data memory/general-purpose I/O port. These pins can be used as a general-purpose I/O port according to the internal registers.
115	$\overline{\text{DCS2}}$ /PORT19	I/O	
116	$\overline{\text{DCS3}}$ /PORT18	I/O	
117	$\overline{\text{DCS4}}$ /PORT17	I/O	
118	$\overline{\text{DCS5}}$ /PORT16	I/O	
119	PORT15	I/O	General-purpose I/O port.
120	PORT14	I/O	
121	V _{SS}	—	GND
122	PORT13	I/O	General-purpose I/O port.
123	PORT12	I/O	
124	PORT11	I/O	
125	PORT10	I/O	
126	PORT9	I/O	
127	PORT8	I/O	
128	PORT7	I/O	
129	V _{DD}	—	Power supply.
130	PORT6	I/O	General-purpose I/O port.
131	PORT5	I/O	
132	PORT4	I/O	
133	PORT3	I/O	
134	PORT2	I/O	
135	PORT1	I/O	
136	PORT0	I/O	
137	V _{SS}	—	GND
138	TXD2	O	UART transmission data output. (channel 2)
139	RXD2	I	UART reception data input. (channel 2)
140	TXD1	O	UART transmission data output. (channel 1)
141	RXD1	I	UART reception data input. (channel 1)
142	TXD0	O	UART transmission data output. (channel 0)
143	RXD0	I	UART reception data input. (channel 0)
144	V _{DD}	—	Power supply.

A/D Converter Characteristics

(0 < VRB < VIN < VRT < AVD = 3.0 to 3.6V, Topr = –40 to +85°C)

Item	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution					8	Bit
Differential linearity error (DLE)		AVD = 3.0V	–0.5		+0.5	LSB
Integral linearity error (ILE)			–2.5		+2.5	LSB
Sampling time		f = 18.414MHz	648			ns
Conversion time			864			ns
Current consumption		AVD = 3.0V		2.0		mA

Electrical Characteristics**DC Characteristics**(V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
Input voltage (1) (CMOS level)	High level	V _{IH} (1)		0.7 × V _{DD}		V _{DD}	V	*1
	Low level	V _{IL} (1)				0.2 × V _{DD}	V	
Input voltage (2) (5V interface)	High level	V _{IH} (2)		0.7 × V _{DD}		5.5	V	*2
	Low level	V _{IL} (2)				0.2 × V _{DD}	V	
Output voltage (1)	High level	V _{OH} (1)	I _{OH} = –4.0mA	V _{DD} – 0.4			V	*3
	Low level	V _{OL} (1)	I _{OL} = 4.0mA			0.4	V	
Output voltage (2)	High level	V _{OH} (2)	I _{OH} = –2.0mA	V _{DD} – 0.8			V	*4
	Low level	V _{OL} (2)	I _{OL} = 4.0mA			0.4	V	
Output voltage (3)	High level	V _{OH} (3)	I _{OH} = –2.0mA	V _{DD} – 0.8			V	*5
	Low level	V _{OL} (3)	I _{OL} = 8.0mA			0.4	V	
Current consumption in standby mode (Using external timer, +85°C)		ISTB	V _{DD} = 3.0V		20	70	μA	—
			V _{DD} = 1.8V		4	50		
Supply current		I _{DD}	f = 18.414MHz		55		mA	—

Applicable pins

*1 Pins 11, 12, 16, 17, 20, 28, 32, 41

*2 Pins 22 to 24, 27, 62, 64 to 69, 71 to 74, 76 to 80, 84, 85, 87 to 94, 96 to 103, 105 to 112, 114 to 120, 122, 128, 130 to 136, 139, 141, 143

*3 Pins 10, 25, 26, 33, 35

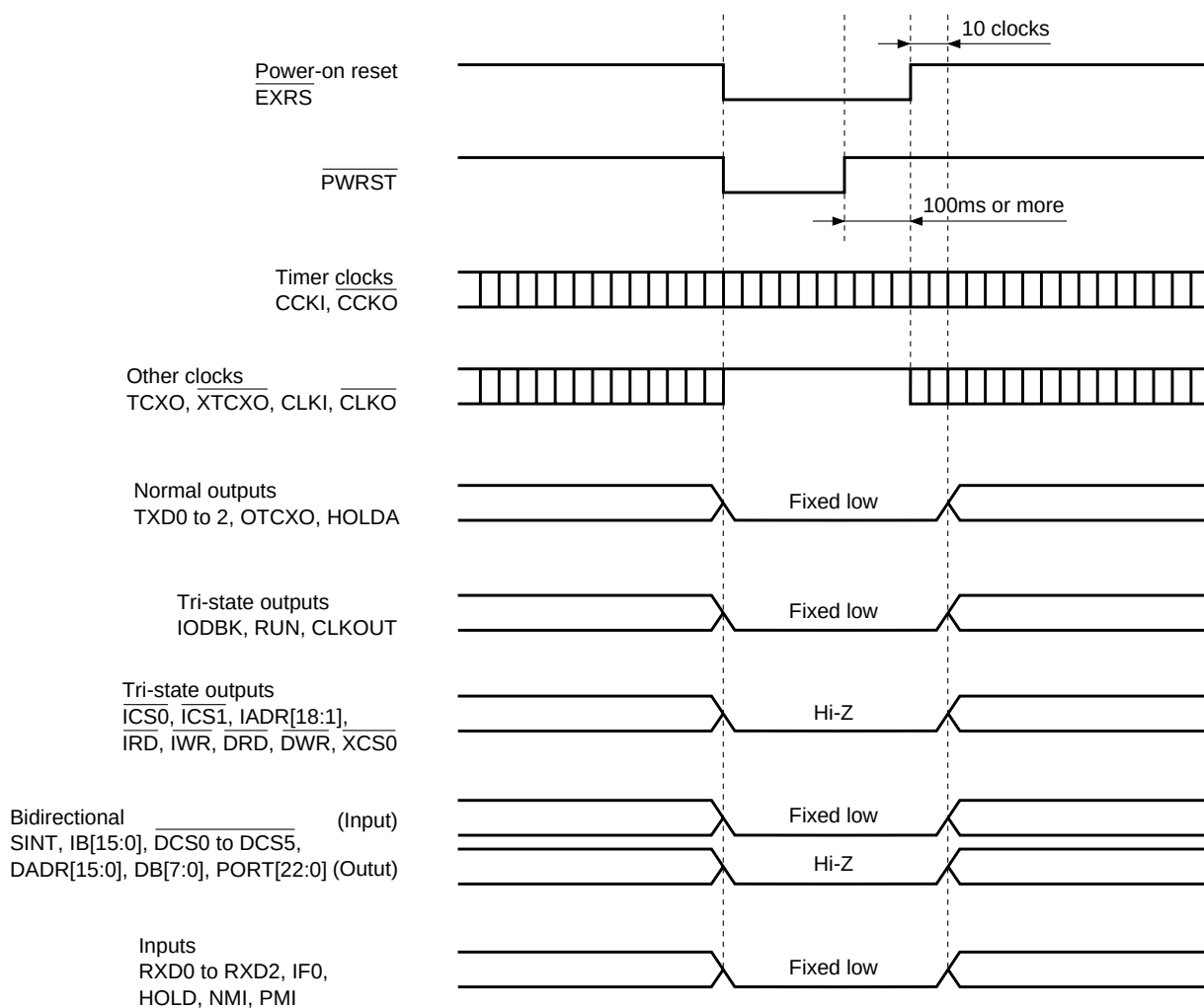
*4 Pins 38, 40, 82, 83, 138, 140, 142

*5 Pins 36, 37, 42 to 46, 48 to 54, 56 to 62, 64 to 69, 71 to 74, 76 to 81, 84, 85, 87 to 94, 96 to 103, 105 to 112, 114 to 120, 122 to 128, 130 to 136

Battery Backup Mode

The battery backup mode is activated when the power for the GPS receiver is turned off and power-on reset goes to low level. The timer clock continues to operate even when power-on reset goes low, but all other clock are fixed high and the LSI is set to the low power consumption mode. At this time, the RAM data is held and the registers are initialized.

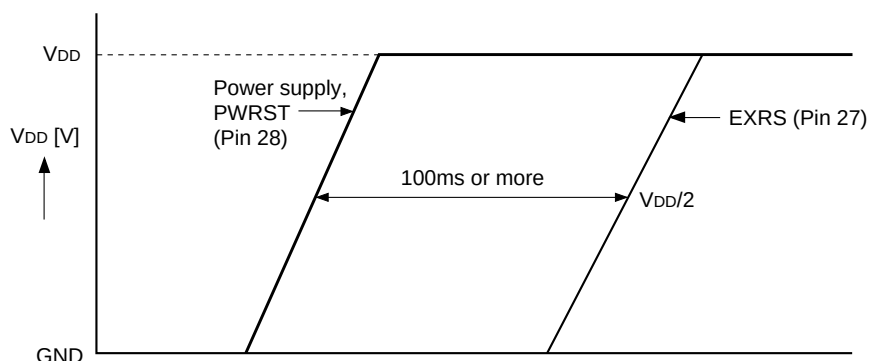
Battery backup mode is canceled by setting power-on reset to high.



CXD2931R-9/GA-9 Initialization

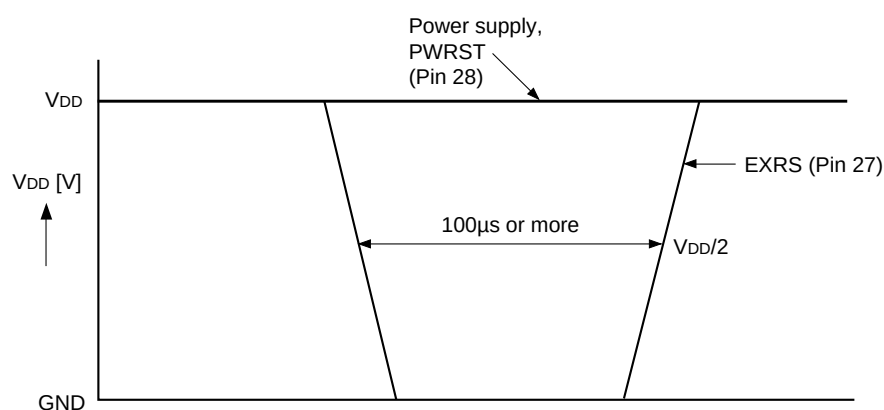
CXD2931R-9/GA-9 initialization is started by setting the reset input signal EXRS (Pin 27) to low level. The timing should satisfy the conditions noted below.

1. During power-on (power-on reset) ($V_{DD} = 3.0$ to $3.6V$, $T_{opr} = -40$ to $+85^{\circ}C$)



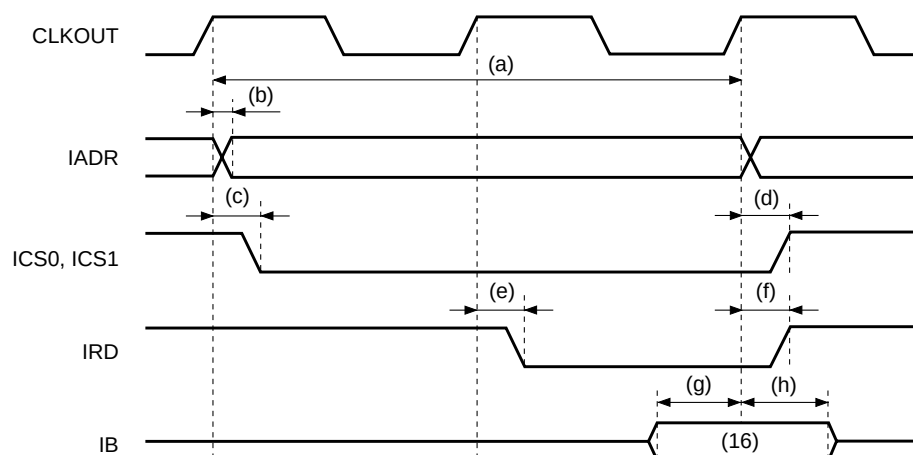
The PWRST (Pin 28) signal should rise simultaneously with the power supply. The EXRS (Pin 27) signal should rise 100ms or more after the power supply and the PWRST signal have risen. Note that the PWRST signal should be left open during battery backup.

2. Initialization during operation ($V_{DD} = 3.0$ to $3.6V$, $T_{opr} = -40$ to $+85^{\circ}C$)



The internal registers can be initialized during operation by setting the EXRS (Pin 27) signal to low level for 100μs or more. Keep the PWRST (Pin 28) signal at high level at this time.

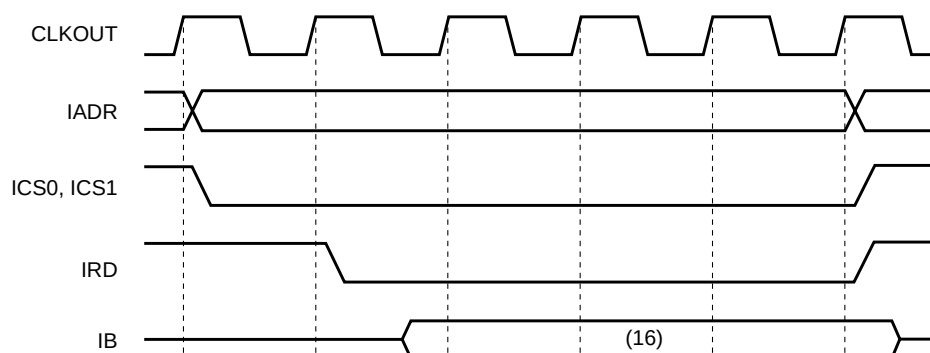
• External Command Fetch Timing (XROMW = 0)



No.	Item	Min.	Typ.	Max.	Unit
(a)	Read cycle time (Fex: @20MHz)	—	100	—	ns
(b)	Address delay time	—	—	12	ns
(c)	Chip select fall delay time	2	—	10	ns
(d)	Chip select rise delay time	2	—	10	ns
(e)	Read signal fall delay time	0	—	3	ns
(f)	Read signal rise delay time	0	—	5	ns
(g)	Read data setup time	11	—	—	ns
(h)	Read data hold time	0	—	—	ns

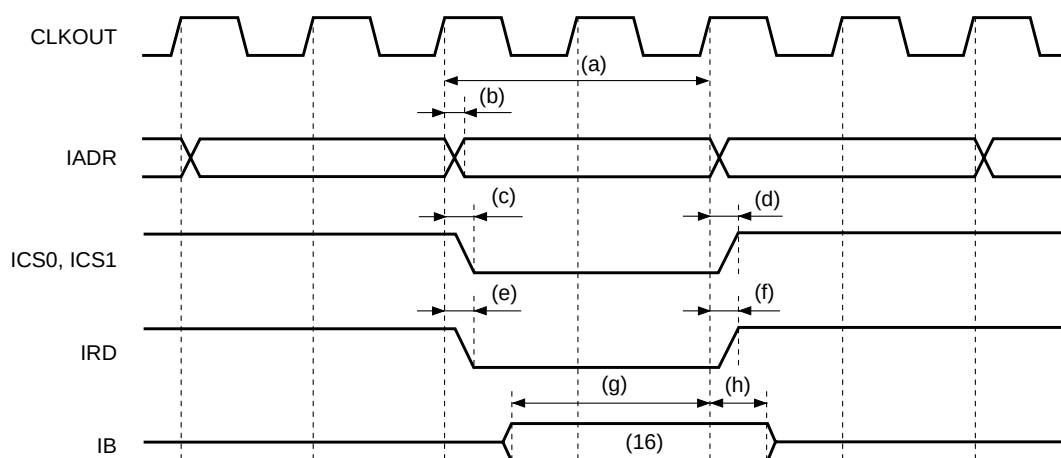
* The load capacitance = 30pF.

• External Command Fetch Timing (XROMW = 1)

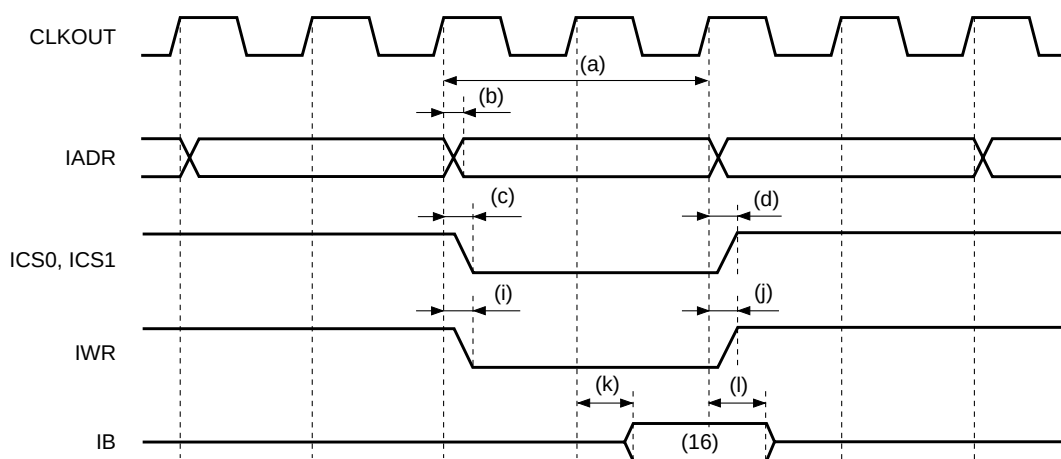


• External Data Access Timing (ICS0, ICS1/XROMW = 0)

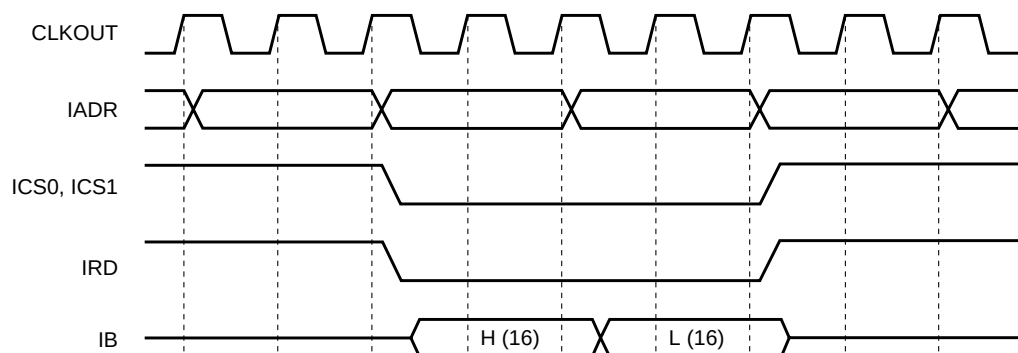
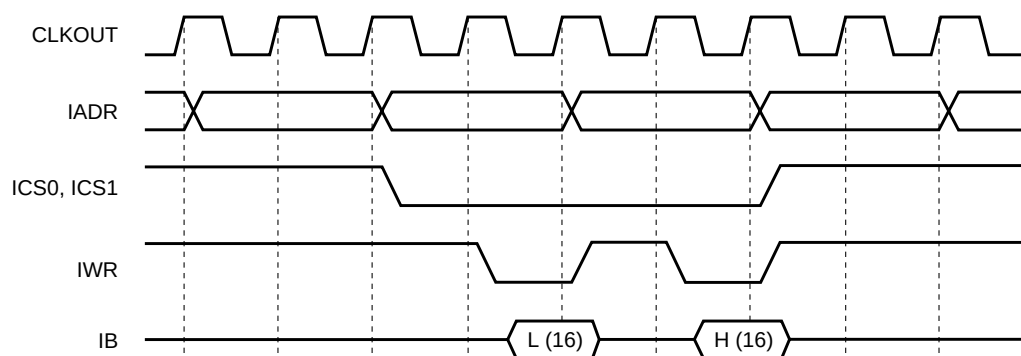
(1) Read (half-word access/XROMW = 0)



(2) Write (half-word access/XROMW = 0)

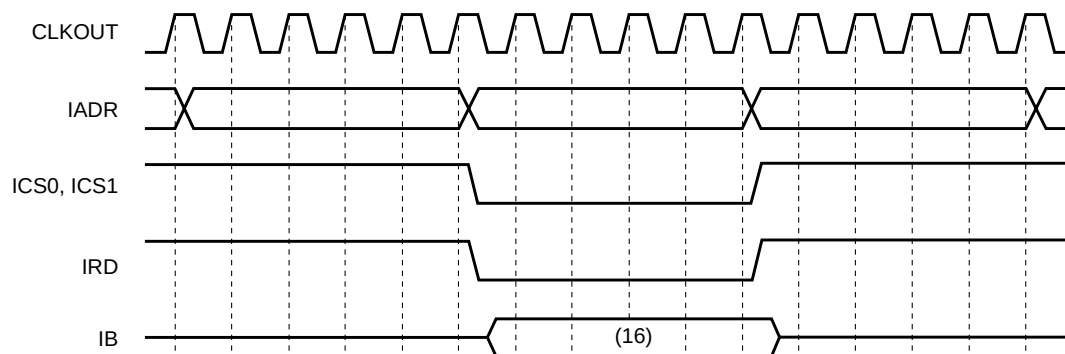


No.	Item	Min.	Typ.	Max.	Unit
(a)	Read/write cycle time (Fex: @20MHz)	—	100	—	ns
(b)	Address delay time	—	—	12	ns
(c)	Chip select fall delay time	2	—	10	ns
(d)	Chip select rise delay time	2	—	10	ns
(e)	Read signal fall delay time	0	—	3	ns
(f)	Read signal rise delay time	0	—	5	ns
(g)	Read data setup time	11	—	—	ns
(h)	Read data hold time	0	—	—	ns
(i)	Write signal fall delay time	0	—	1	ns
(j)	Write signal rise delay time	0	—	2	ns
(k)	Write data established time	—	—	5	ns
(l)	Write data hold time	5	—	—	ns

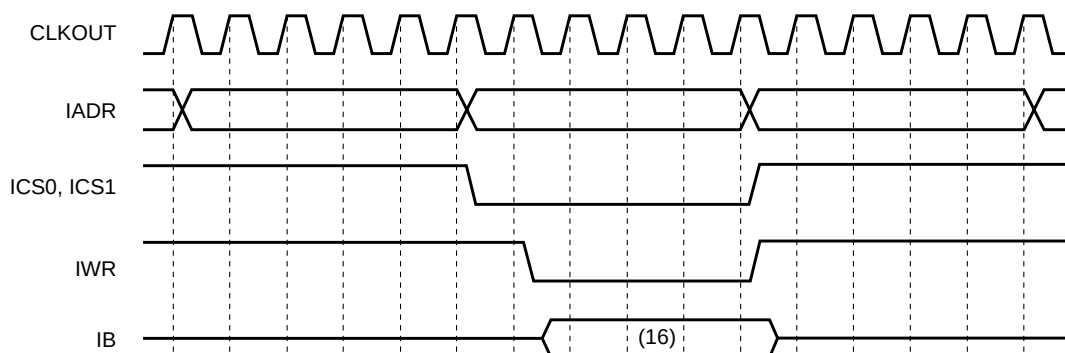
(3) Read (word access/XROMW = 0)**(4) Write (word access/XROMW = 0)**

• External Data Access Timing (ICS0, ICS1/XROMW = 1)

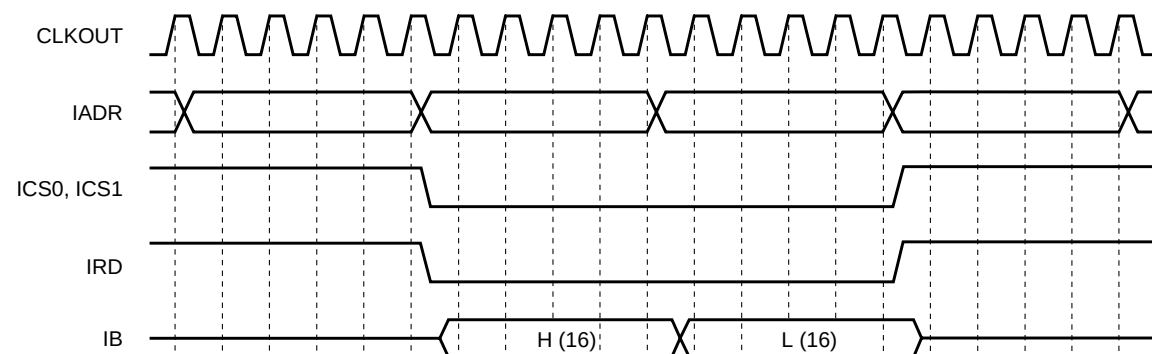
(1) Read (half-word access/XROMW = 1)



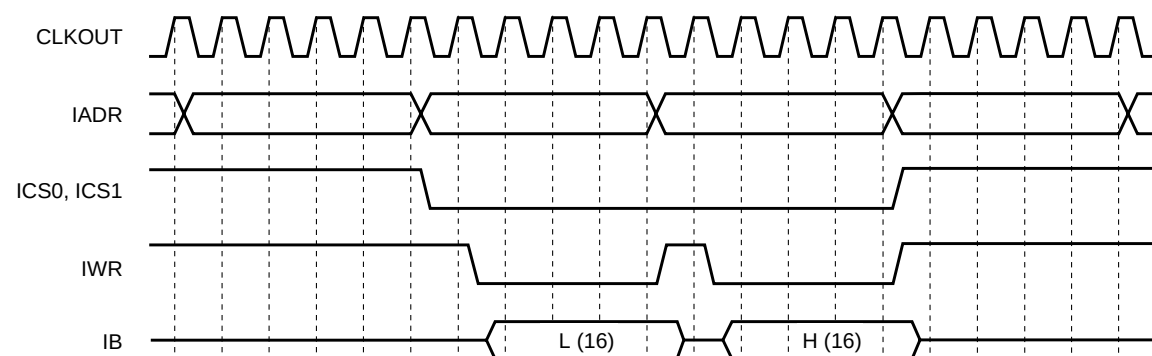
(2) Write (half-word access/XROMW = 1)



(3) Read (word access/XROMW = 1)

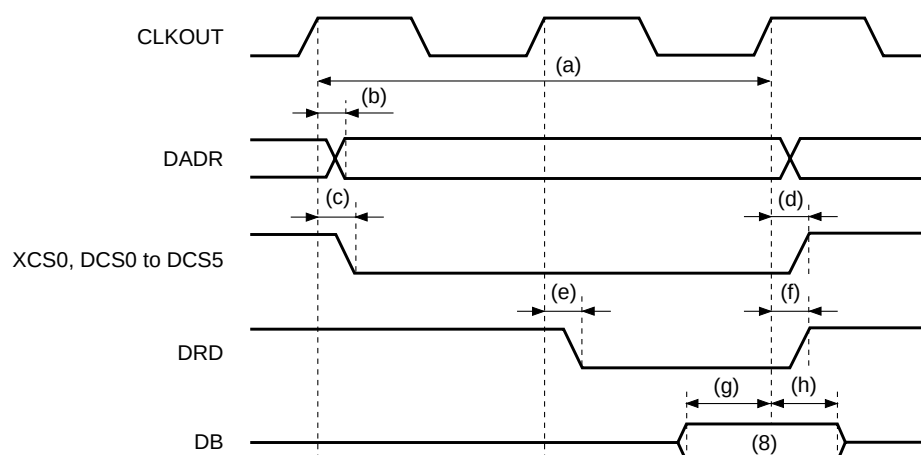


(4) Write (word access/XROMW = 1)

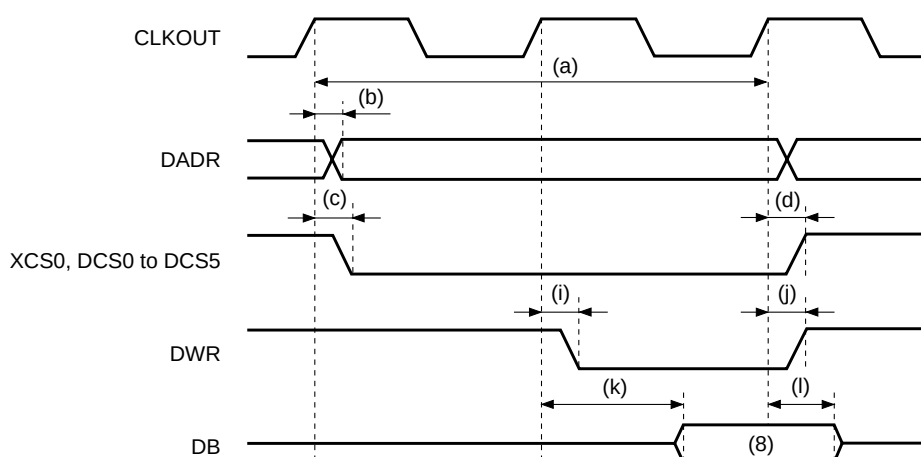


• External Data Access Timing (XCS0, DCS0 to DCS5/no data wait)

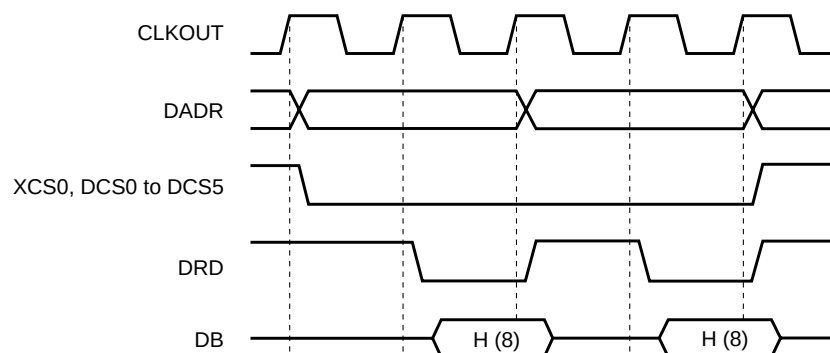
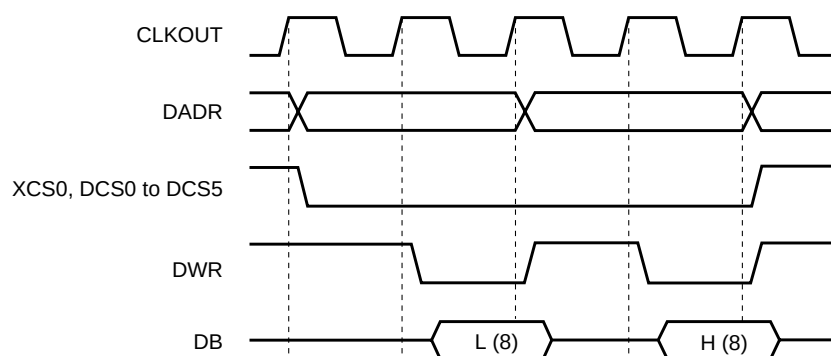
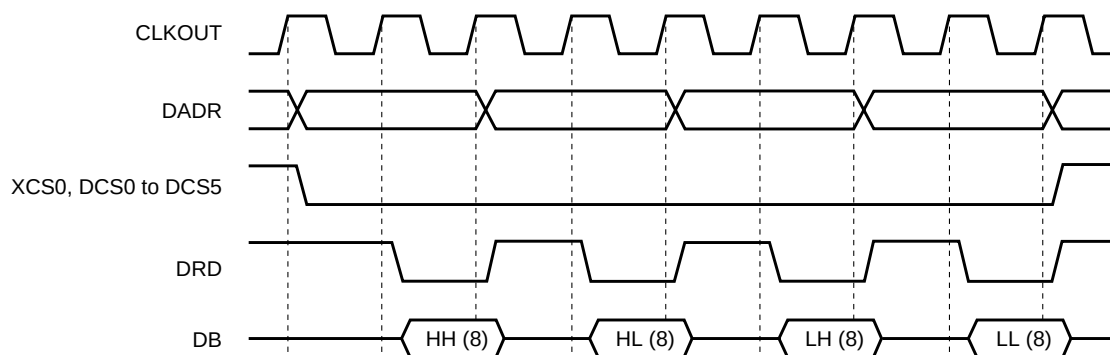
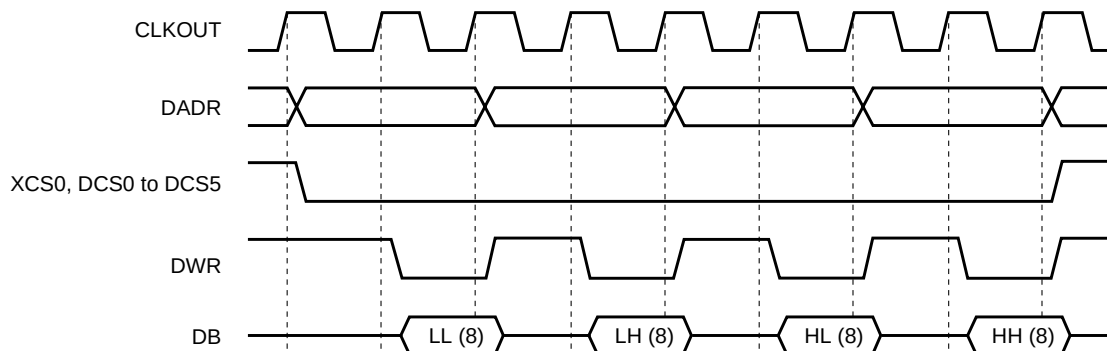
(1) Read (byte access/no data wait)



(2) Write (byte access/no data wait)

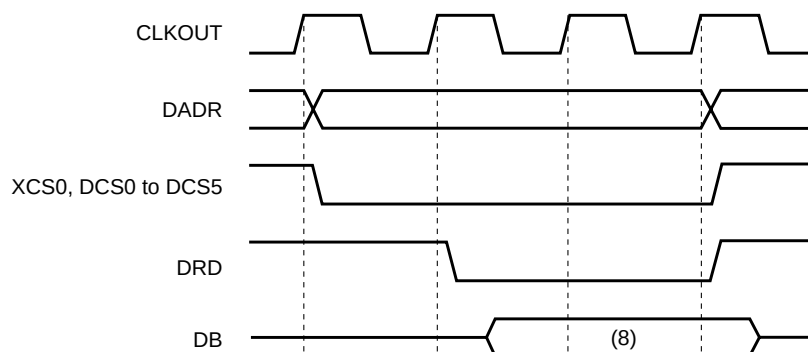


No.	Item	Min.	Typ.	Max.	Unit
(a)	Read/write cycle time (Fex: @20MHz)	—	100	—	ns
(b)	Address delay time	—	—	12	ns
(c)	Chip select fall delay time	3	—	13	ns
(d)	Chip select rise delay time	3	—	13	ns
(e)	Read signal fall delay time	2	—	8	ns
(f)	Read signal rise delay time	2	—	10	ns
(g)	Read data setup time	16	—	—	ns
(h)	Read data hold time	0	—	—	ns
(i)	Write signal fall delay time	0	—	2	ns
(j)	Write signal rise delay time	0	—	3	ns
(k)	Write data established time	—	—	12	ns
(l)	Write data hold time	5	—	—	ns

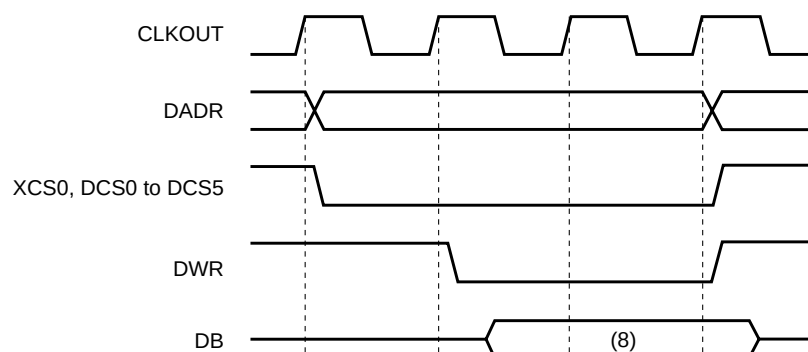
(3) Read (half-word access/no data wait)**(4) Write (half-word access/no data wait)****(5) Read (word access/no data wait)****(6) Write (word access/no data wait)**

• External Data Access Timing (XCS0, DCS0 to DCS5/data wait = 1)

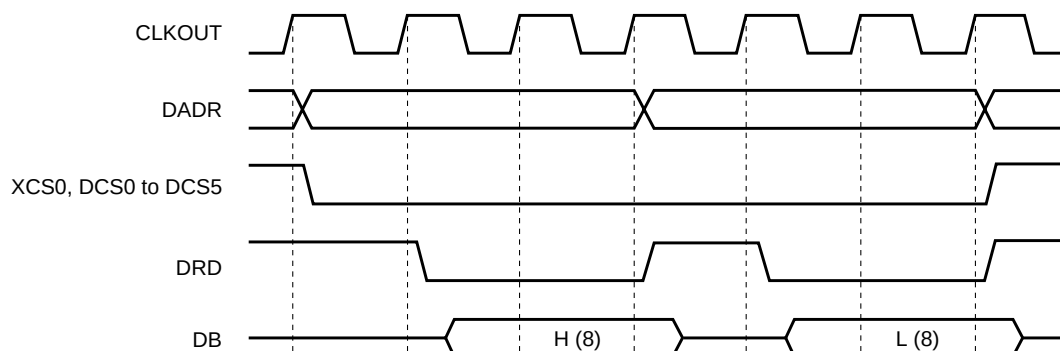
(1) Read (byte access/data wait = 1)



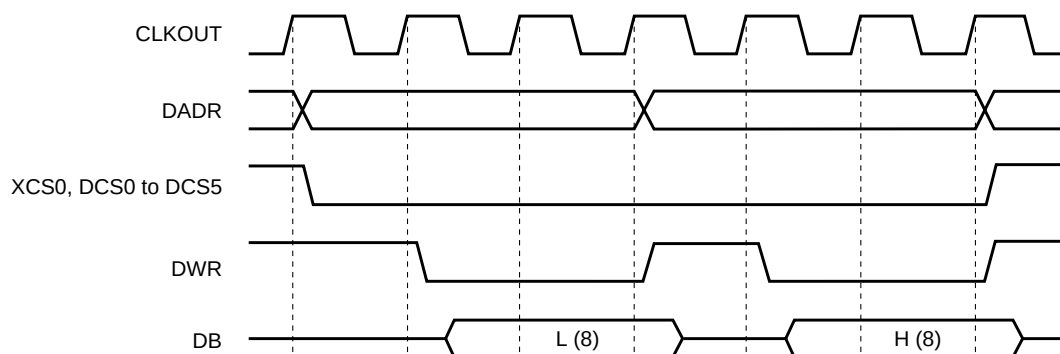
(2) Write (byte access/data wait = 1)

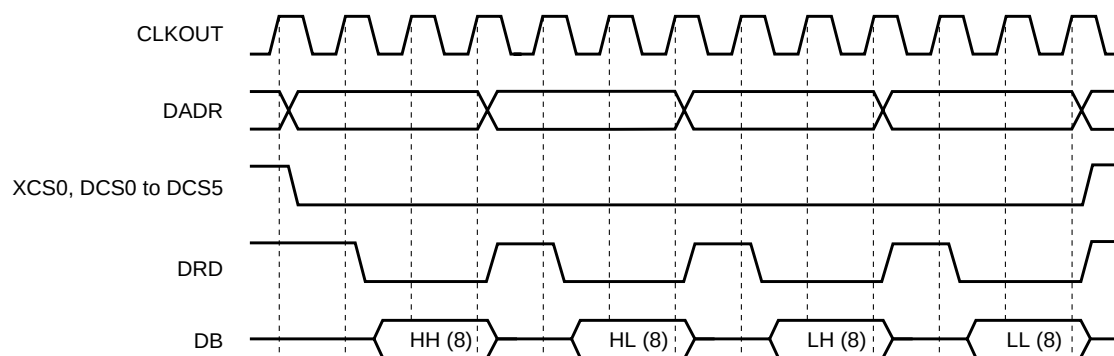
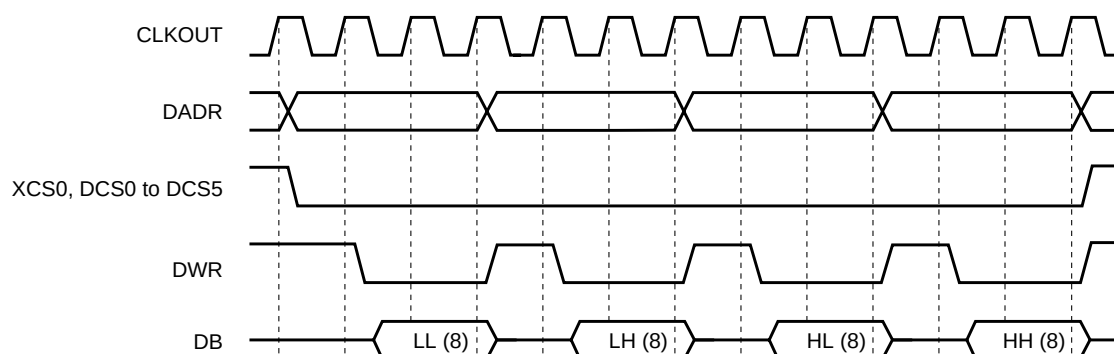
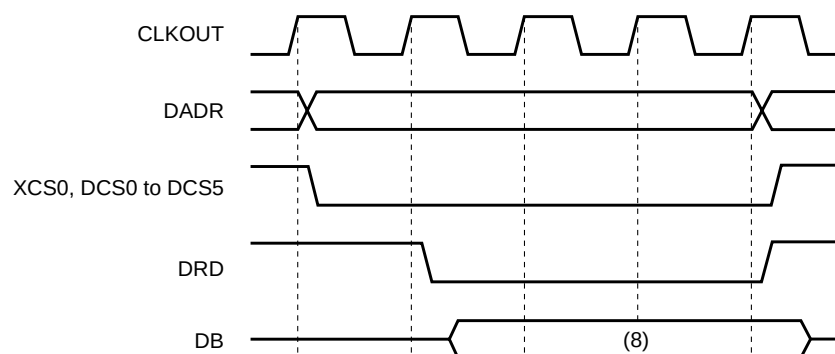
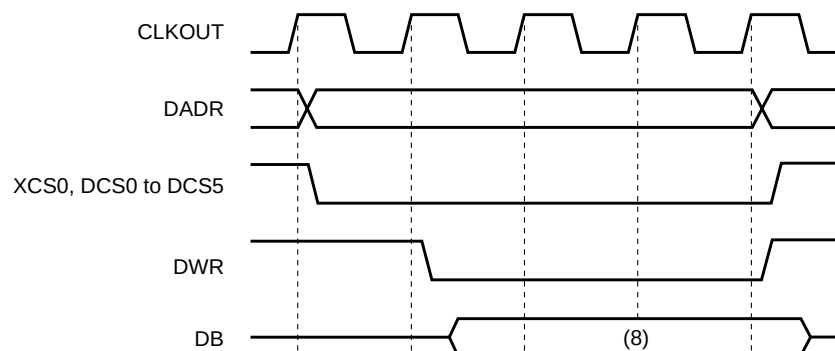


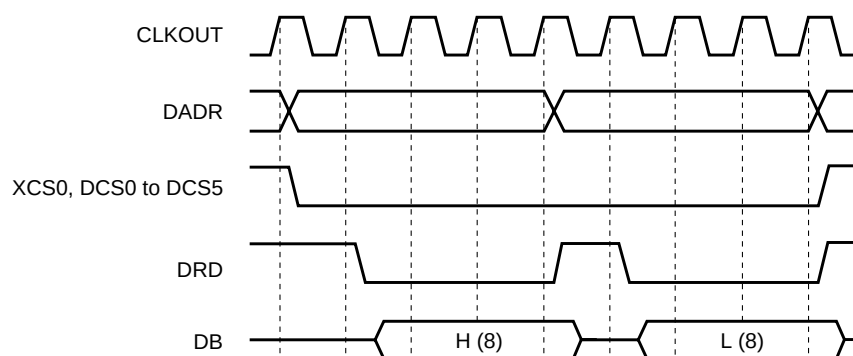
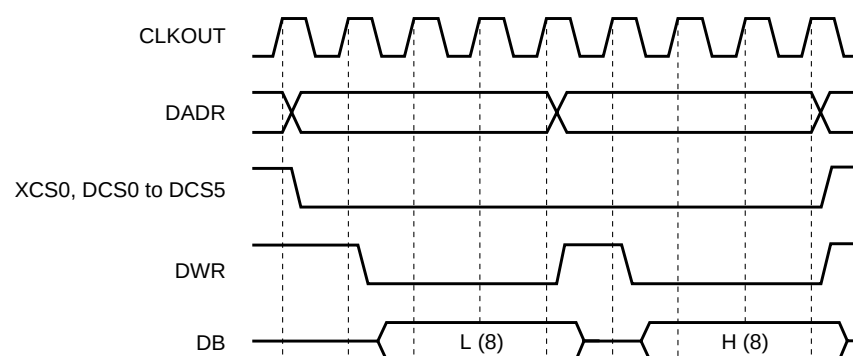
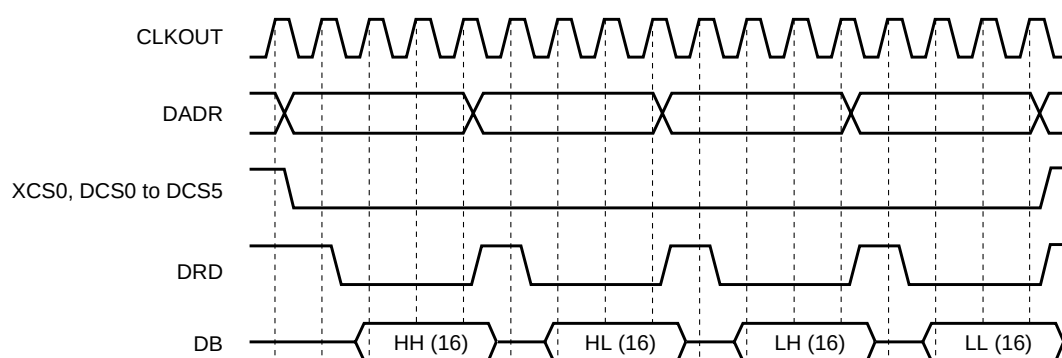
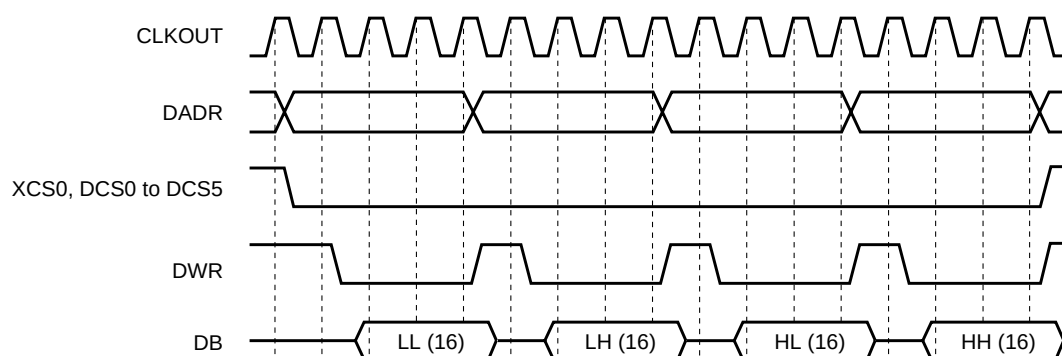
(3) Read (half-word access/data wait = 1)



(4) Write (half-word access/data wait = 1)



(5) Read (word access/data wait = 1)**(6) Write (word access/data wait = 1)****• External Data Access Timing (XCS0, DCS0 to DCS5/data wait = 2)****(1) Read (byte access/data wait = 2)****(2) Write (byte access/data wait = 2)**

(3) Read (half-word access/data wait = 2)**(4) Write (half-word access/data wait = 2)****(5) Read (word access/data wait = 2)****(6) Write (word access/data wait = 2)**

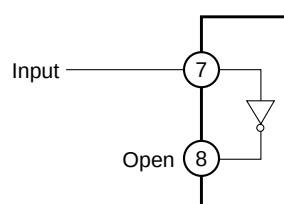
Application Notes

The constants shown in the circuits below are the examples, and do not guarantee the circuit operation.

1. TCXO input

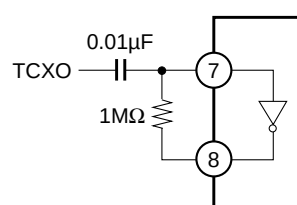
- (1) When inputting the binary-converted signal

The TCXO (Pin 7) input signal should be $18.414\text{MHz} \pm 3\text{ppm}$.



- (2) When performing the self-oscillation with the TCXO and XTCXO pins (Pins 7 and 8)

The TCXO (Pin 7) input signal should be $18.414\text{MHz} \pm 3\text{ppm}$.



2. CPU clock generation

Pin 32 is used to select that TCXO is used or that the self-oscillation is performed with the MCKI and $\overline{\text{MCKO}}$ pins (Pins 30 and 31).

- (1) TCXO solution (TCXO is used for CPU clock)

Set Pin 32 to low.

Pin 30: Low

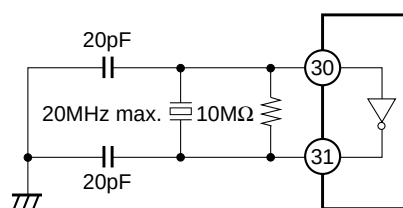
Pin 31: Open

- (2) When performing the self-oscillation with the MCKI and $\overline{\text{MCKO}}$ pins (Pins 30 and 31)

Set Pin 32 to high.

The crystal frequency should be less than 20MHz.

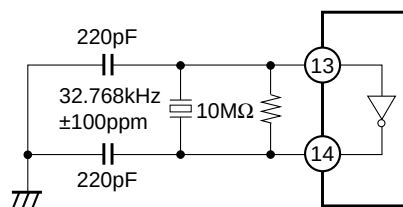
The following circuit is just a reference, and is not guaranteed.



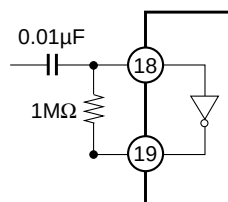
(3) Using internal clock

Set PORT5 (Pin 131) to high.

Connect the external parts as follows when performing the self-oscillation with the CCKI and CCKO pins (Pins 13 and 14).



(4) Input IF signal



Description of Application Circuit

See the Application Circuit when using the CXD2931R-9/GA-9 to configure a GPS receiver.
Points for caution are as follows.

1. Unused pins

Software processing is performed to prevent undesired current from flowing to unused pins in the circuit diagram, so leave these pins open.

2. TCXO input

The TCXO frequency is $18.414\text{MHz} \pm 3\text{ppm}$. Signals that have not been binary-converted should be input via a DC filter capacitor (C19 in the circuit diagram). Input binary-converted signals directly to Pin 7 (TCXO) without passing through C19 or R1 in the circuit diagram.

Make sure the input level at this time satisfies the Electrical Characteristics.

3. IF input

The CXD2931R-9/GA-9 interface is 1.023MHz, and does not accept other frequencies. Signals that have not been binary-converted should be input via a DC filter capacitor (C20). Input binary-converted signals directly to Pin 18 (IF0) without passing through C20 or R3 in the circuit diagram.

Make sure the input level at this time satisfies the Electrical Characteristics.

4. TXD (SIO output)

The TXD amplitude low level is 0.4V or less, and the high level is $V_{DD} - 0.4\text{V}$ ($V_{DD} = 3.0$ to 3.6V) or more. When the LSI, etc., connected to TXD operates at 5V and has a CMOS input level, perform 3 to 5V conversion before inputting the signal.

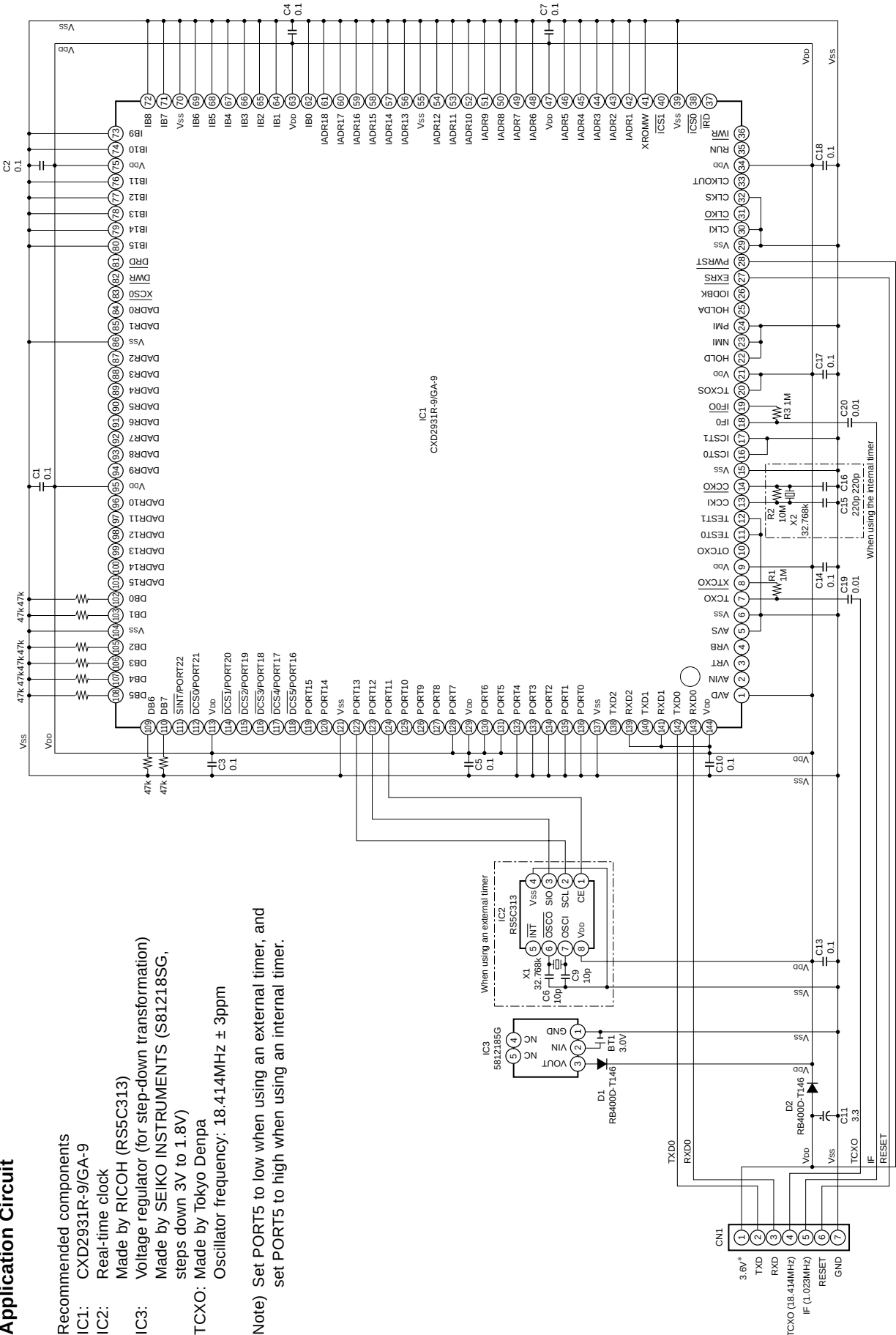
5. Real-time clock

The current software version uses an external real-time clock. Consult your Sony representative beforehand when using the internal real-time clock. When using an external real-time clock, connect Pin 13 (CCKI) to GND.

Application Circuit

- Recommended components
IC1: CXD2931R-9/GA-9
IC2: Real-time clock
Made by RICOH (RS5C313)
IC3: Voltage regulator (for step-down transformation)
Made by SEIKO INSTRUMENTS (S81218SG,
steps down 3V to 1.8V)
TCXO: Made by Tokyo Denpa
Oscillator frequency: 18.414MHz ± 3ppm

Note) Set PORT5 to low when using an external timer, and
set PORT5 to high when using an internal timer.



* Input 3.6V in consideration of voltage step-down by diode (D2).

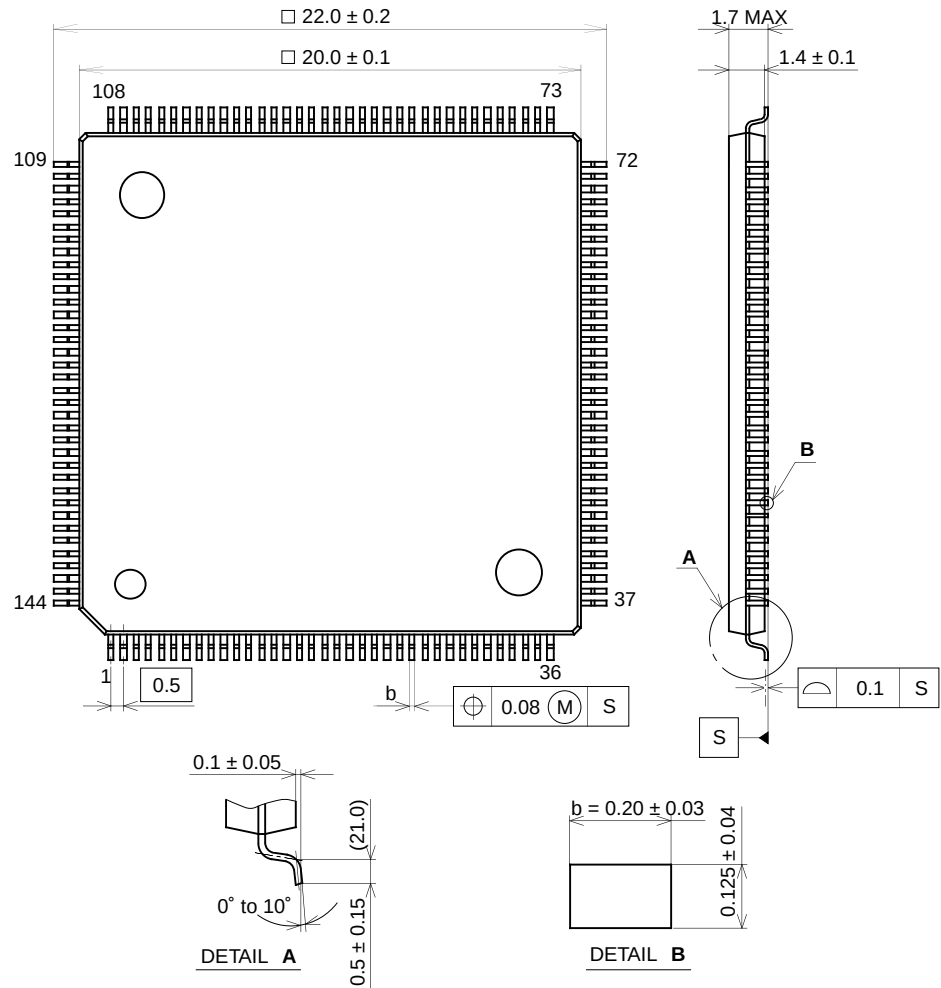
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

Unit: mm

CXD2931R-9

144PIN LQFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LQFP-144P-L01
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	_____
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.3 g

Unit: mm

CXD2931GA-9

Figure 1: Package Structure. This technical drawing shows the top, side, and detail views of a package. The top view is a square with 15x15 pins (144 total) and a 13.0mm side length. It includes a 'PIN 1 INDEX' and various dimension callouts like 0.2, 0.15, 0.55, 0.8, 0.9, and 1.4MAX. The side view shows a thickness of 0.10mm. Detail X shows a cross-section of the package with a 0.01mm gap and a 0.20mm width.

PACKAGE STRUCTURE

SONY CODE	LFLGA-144P-01
EIAJ CODE	P-LFLGA144-13x13-0.8
JEDEC CODE	_____

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	NICKEL & GOLD PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.5g