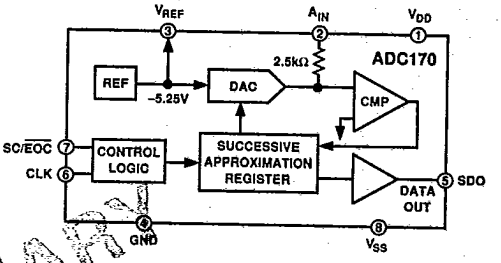
Complete, Serial-Out 5.6 µs, 12-Bit A/D Converter

T-51-10-12 **ADC-170**

FEATURES
- 8-Pin Mini-DIP Package
- Fast Conversion Time—5.6 µs
- Low Power—135 mW typical
- Internal Low Drift Bandgap Reference
- 0 to +5 V Analog Input Range
- 3-Wire Signal Interface

APPLICATIONS
- Data Acquisition Systems
- Medical Diagnostics
- Avionic and Navigation Systems
- Process Control Equipment
- Multichannel Analog I/O
- Isolated Industrial Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The ADC-170 is a complete, serial-output, 12-bit analog-to-digital converter with voltage reference, all in a space-saving 8-pin mini-DIP or 16-pin surface mount SOIC package. Operating from an external 2.5 MHz (max) clock, input signals of up to 5 V are digitized at a 5.6 µs rate. A TTL-compatible three-wire serial interface transfers the digital output data directly to the serial port of the host processor, or easily interfaces with opto isolators or transformers for high voltage isolation.

Fabricated in a complementary bipolar CMOS (CBCMOS) process, the ADC-170 utilizes a successive approximation architecture with a high speed DAC and low noise PNP-input comparator to achieve both high speed and low power operation. Operating from +5 V and −12 V to −15 V supplies, power consumption is only 135 mW. The internal voltage reference is a low drift bandgap which maintains guaranteed accuracy over the full operating temperature range of the device.

Following a start of conversion pulse, the MSB of the new digital word is available at the serial data output after 2 clock cycles, during which the new conversion results are read with the remaining 12 clock cycles. The ADC-170 can be configured for single conversion or continuous operation.

The ADC-170 provides the most complete 12-bit ADC solution available in a compact package. When combined with the serial-input DAC-8043 in the 8-pin mini-DIP package, the result is an unusually dense, high performance analog input/output port.

The ADC-170 is available in 8-pin plastic and Cerdip packages, while the SOIC-16 addresses surface mount applications. All parts are offered in the extended industrial temperature range (−40°C to +85°C). For −55°C to +125°C applications, contact your local Analog Devices sales office to obtain the ADC-170/883 data sheet.

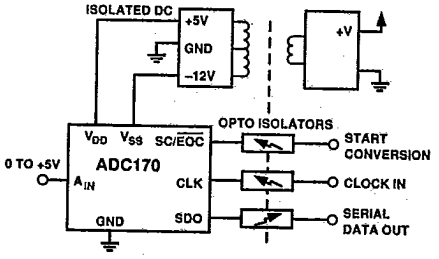

Figure 1. ADC-170 High Voltage Isolation Application

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REV. A

ADC-170—SPECIFICATIONS

T-51-10-12

ELECTRICAL CHARACTERISTICS (V_{DD} = +5 V ± 5%, V_{SS} = −11.4 V to −15.75 V; f_{CLK} = 2.5 MHz; −40°C ≤ T_A ≤ +85°C unless otherwise noted.)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
ACCURACY							
Resolution	N			12			Bits
Integral Nonlinearity	INL	T_A = +25°C	ADC170E			±1/2	LSB
			ADC170F			±1	LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic over Temp				±1	LSB
Offset Error	V_{ZSE}		ADC170E			±3	LSB
			ADC170F			±5	LSB
Full-Scale Error	V_{FSE}	T_A = +25°C				±10	LSB
Full-Scale Tempco[1]	TCV_{FS}		ADC170E			±25	ppm/°C
			ADC170F			±45	ppm/°C
Conversion Time	t_{CONV}	14 Clock Cycles			5.6		µs
ANALOG INPUT							
Input Voltage Range	A_{IN}			0		+5	V
Input Current	I_{IN}	A_{IN} = 0 V to +5 V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage	V_{REF}	T_A = 25°C		−5.2	−5.25	−5.3	V
V_{REF} Output Tempco[1]	TCV_{REF}		ADC170E		±20		ppm/°C
			ADC170F		±40		ppm/°C
Output Current Sink Capability	I_{REF}					5	mA
POWER SUPPLY REJECTION							
Positive Supply Rejection	V_{DD}	FS Change, V_{SS} = −15 V or −12 V, V_{DD} = 4.75 V to 5.25 V			±1/2		LSB
Negative Supply Rejection	V_{SS}	FS Change, V_{DD} = +5 V	V_{SS} = −14.25 V to −15.75 V		±1/8		LSB
			V_{SS} = −11.4 V to −12.6 V		±1/8		LSB
LOGIC INPUTS							
Input Low Voltage	V_{IL}					0.8	V
Input High Voltage	V_{IH}			2.4			V
Input Capacitance[1]	C_{IN}					10	pF
Input Current	I_{INL}	A_{IN} = 0 to V_{DD}	CLOCK			±10	µA
			SC/$\overline{EOC}$	±200		±500	µA
LOGIC OUTPUT							
Output Low Voltage	V_{OL}	SDO I_{SINK} = 1.6 mA				0.4	V
		SDO I_{SINK} = 6.0 mA			0.3	1.5	V
Output High Voltage	V_{OH}	SDO I_{SOURCE} = 200µA		4			V
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	±5% for Specified Performance			5		V
Negative Supply Voltage[2]	V_{SS}	±5% for Specified Performance			−15 to −12		V
Positive Supply Current	I_{DD}	SC/$\overline{EOC}$ = V_{DD}, A_{IN} = 0 V			5	8	mA
Negative Supply Current	I_{SS}	SC/$\overline{EOC}$ = V_{DD}, A_{IN} = 0 V			−6	−11	mA
Power Dissipation	P_{DISS}	V_{DD} = +5 V, V_{SS} = −15 V			135	205	mW

TIMING CHARACTERISTICS[3] (V_{DD} = +5 V, V_{SS} = −12 V or −15 V; −40°C ≤ T_A ≤ +85°C)

CLOCK Pulse Width	t_{CH}	CLK HIGH		40			ns
	t_{CL}	CLK LOW		60			ns
SC/$\overline{EOC}$ Pulse Width	t_{SH}	SC/$\overline{EOC}$ HIGH		40			ns
	t_{SL}	SC/$\overline{EOC}$ LOW		60			ns
SC/$\overline{EOC}$ to CLK Skew	t_{SC0}	Leading CLK				40	ns
	t_{SC1}	Leading CLK + 1		200			ns
CLK to SDO Delay	t_{PD}			25		80	ns

NOTES
[1]Guaranteed by design, not subject to test.
[2]Specified performance with −12 V supply is guaranteed by testing offset and full-scale errors.
[3]Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with t_R = t_F = 5 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.
Specifications subject to change without notice.