REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 11. Change limits I_{CC} and I_{CCDR1} in table I.	98-06-22	K. A. Cottongim

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A								
SHEET	15	16	17	18	19	20	21	22	23	24	25								

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary Zahn

CHECKED BY
Michael C. Jones

APPROVED BY
Kendall A. Cottongim

DRAWING APPROVAL DATE
96-10-30

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
P. O. BOX 3990
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, MEMORY, DIGITAL, STATIC RANDOM ACCESS MEMORY, CMOS, 128K x 8-BIT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96691**

SHEET 1 OF 25

DSCC FORM 2233
APR 97

5962-E379-98

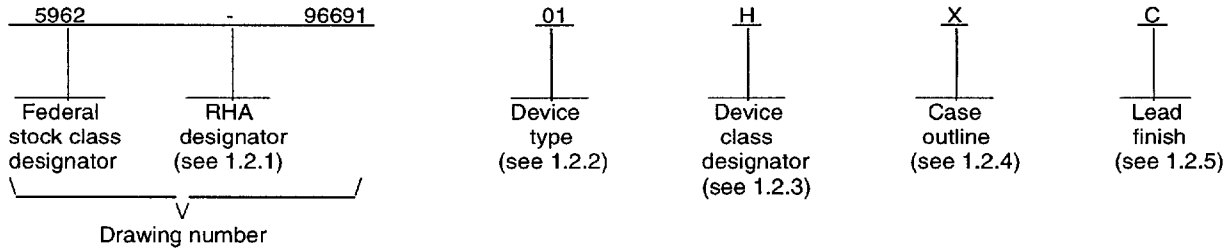
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0036813 665

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WMS128K8-120	SRAM, 128K X 8-bit	120 ns
02	WMS128K8-100	SRAM, 128K X 8-bit	100 ns
03	WMS128K8-85	SRAM, 128K X 8-bit	85 ns
04	WMS128K8-70	SRAM, 128K X 8-bit	70 ns
05	WMS128K8-55	SRAM, 128K X 8-bit	55 ns
06	WMS128K8-45	SRAM, 128K X 8-bit	45 ns
07	WMS128K8-35	SRAM, 128K X 8-bit	35 ns
08	WMS128K8-25	SRAM, 128K X 8-bit	25 ns
09	WMS128K8-20	SRAM, 128K X 8-bit	20 ns
10	WMS128K8-17	SRAM, 128K X 8-bit	17 ns
11	WMS128K8-15	SRAM, 128K X 8-bit	15 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	32	Co-fired ceramic SOJ, revolutionary
T	See figure 1	32	Co-fired ceramic SOJ, evolutionary
X	See figure 1	36	Co-fired ceramic flatpack, revolutionary
Y	See figure 1	32	Co-fired ceramic dual-in-line, evolutionary
Z	See figure 1	36	Co-fired ceramic SOJ, revolutionary

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Signal voltage range (V_G)	-0.5 V dc to V_{CC} +0.5 V dc
Power dissipation (P_D)	0.88 W Max.
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.3 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} + 0.3 V dc
Case operating temperature (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figure 4 and 5.

3.2.5 Block diagram(s). The block diagrams shall be as specified on figure 6.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC parameters							
Input leakage current	I_{LI}	V_{IL} = 5.5 V dc, V_{IN} = GND to V_{CC}	1,2,3	All		10	µA
Output leakage current	I_{LO}	$\overline{CS} = \overline{OE} = V_{IH}$, V_{OUT} = GND to V_{CC}	1,2,3	All		10	µA
Operating supply current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V_{CC} = 5.5 V dc	1,2,3	01,02 03,04 05,06 07,08 09,10, 11		30 30 150 150 150	mA
Standby current	I_{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V_{CC} = 5.5 V dc	1,2,3	01,02 03,04 05,06 07,08 09,10, 11		0.6 1.0 15 15 20	mA
Input low level	V_{IL}		1,2,3	All		0.8	V
Input high level	V_{IH}		1,2,3	All	2.2		V
Output low voltage	V_{OL}	Device types 01 through 07 V_{CC} = 4.5 V, I_{OL} = 2.1 mA Device types 08 through 11 V_{CC} = 4.5 V, I_{OL} = 8.0 mA	1,2,3	All		0.4	V
Output high voltage	V_{OH}	Device types 01 through 07 V_{CC} = 4.5 V, I_{OL} = -1.0 mA Device types 08 through 11 V_{CC} = 4.5 V, I_{OL} = -4.0 mA	1,2,3	All	2.4		V
Dynamic characteristics							
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz T_A = +25°C	4	All		20	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic characteristics - Continued.							
Output capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1.0 MHz T_A = +25°C	4	All		20	pF
Data Retention Characteristics							
Data retention supply voltage	V_{DR}	$\overline{CS} \ge V_{CC}$ - 0.2 V	1,2,3	All	2.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0 V	1,2,3	01-04 05-08 09-10, 11		0.4 2.9 2.9	mA
Functional testing							
Functional tests		See 4.3.1c	7,8A,8B	All			
Read cycle AC timing characteristics							
Read cycle time	t_{RC}	See figure 4	9,10,11	01 02 03 04 05 06 07 08 09 10 11	120 100 85 70 55 45 35 25 20 17 15		ns
Address access time	t_{AA}	See figure 4	9,10,11	01 02 03 04 05 06 07 08 09 10 11		120 100 85 70 55 45 35 25 20 17 15	ns
Output hold from address change	t_{OH}	See figure 4	9,10,11	01-04 05-11	5 0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle AC timing characteristics - Continued.							
Chip select access time	t_{ACS}	See figure 4	9,10,11	01 02 03 04 05 06 07 08 09 10 11		120 100 85 70 55 45 35 25 20 17 15	ns
Output enable to output valid	t_{OE}	See figure 4	9,10,11	01 02 03 04 05 06 07 08 09 10 11		60 50 45 35 30 25 20 15 12 10 10	ns
Chip select to Output in Low Z 3/	t_{CLZ}	See figure 4	9,10,11	01-04 05-11	5 3		ns
Output enable to Output in Low Z 3/	t_{OLZ}	See figure 4	9,10,11	01-04 05-11	5 0		ns
Chip select to Output in High Z 3/	t_{CHZ}	See figure 4	9,10,11	01,02 03,04 05-07 08 09-10, 11		35 25 20 12 10	ns
Output disableto Output in High Z 3/	t_{OHZ}	See figure 4	9,10,11	01,02 03,04 05-07 08 09-10, 11		35 25 20 12 10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle AC timing characteristics							
Write cycle time	t_{WC}	See figure 5	9,10,11	01	120		ns
				02	100		
				03	85		
				04	70		
				05	55		
				06	45		
				07	35		
				08	25		
				09	20		
				10	17		
				11	15		
Chip select to end of write	t_{CW}	See figure 6	9,10,11	01	100		ns
				02	80		
				03	75		
				04	60		
				05	45		
				06	30		
				07	25		
				08	20		
				09	15		
				10	14		
				11	14		
Address valid to end of write	t_{AW}	See figure 6	9,10,11	01	100		ns
				02	80		
				03	75		
				04	60		
				05	45		
				06	30		
				07	25		
				08	20		
				09	15		
				10	15		
				11	14		
Data valid to end of write	t_{DW}	See figure 6	9,10,11	01	50		ns
				02	40		
				03	35		
				04	30		
				05	25		
				06	25		
				07	20		
				08	15		
				09	12		
				10	10		
				11	10		

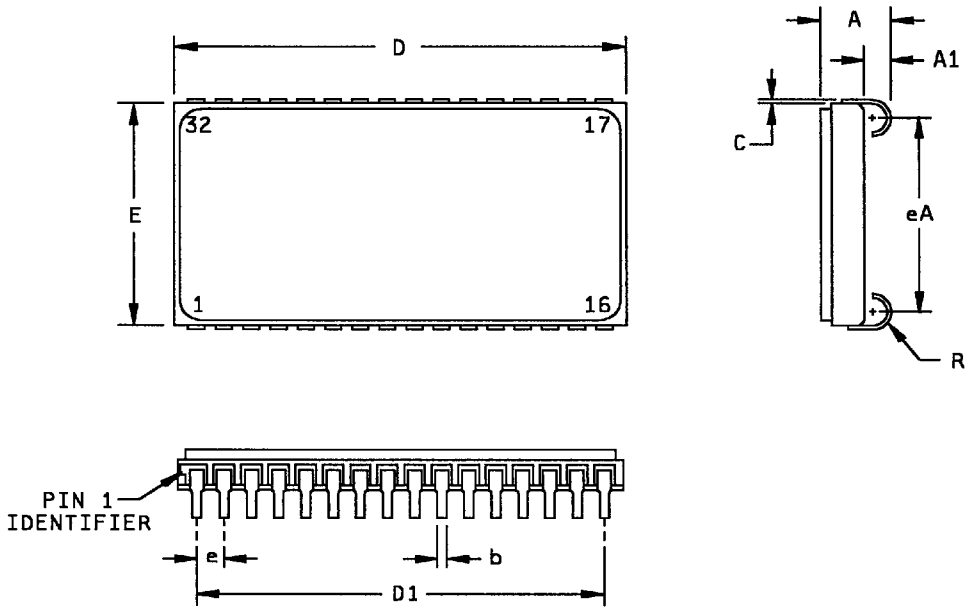
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle AC timing characteristics - Continued.							
Write pulse width	t_{WP}	See figure 6	9,10,11	01 02 03 04 05 06 07 08 09 10 11	80 70 55 50 45 30 25 20 15 14 14		ns
Address set-up time	t_{AS}	See figure 6	9,10,11	All	0		ns
Address hold time	t_{AH}	See figure 6	9,10,11	01-04 05-11	5 0		ns
Output active from end of write 3/	t_{OW}	See figure 6	9,10,11	01-04 05-07 08-11	5 4 3		ns
Data hold time	t_{DH}	See figure 6	9,10,11	All	0		ns

1/ Unless otherwise specified, 4.5 V dc $\le V_{CC} \ge$ 5.5 V dc and V_{SS} = 0 V.
2/ Unless otherwise specified, the DC test conditions are as follows:
Input pulse levels: $V_{IH} = V_{CC}$ - 0.3 V and V_{IL} = 0.3V.
Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
Input rise and fall times: 5 nanoseconds
Input and output timing reference levels: 1.5 V
3/ Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be to the limits specified in table 1 for all lots not specifically tested.

Case outlines U and T.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.69	3.96	0.106	0.156
A1	1.02	1.52	0.040	0.060
b	0.38	0.48	0.015	0.019
C	0.15	0.25	0.006	0.010
D	20.83	21.35	0.820	0.840
D1	18.92	19.18	0.745	0.755
E	10.80	11.05	0.425	0.435
e	1.27 TYP.		0.050 TYP.	
eA	9.30	9.80	0.366	0.386
R	0.89 TYP.		0.035 TYP.	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines(s).

Case outline X.

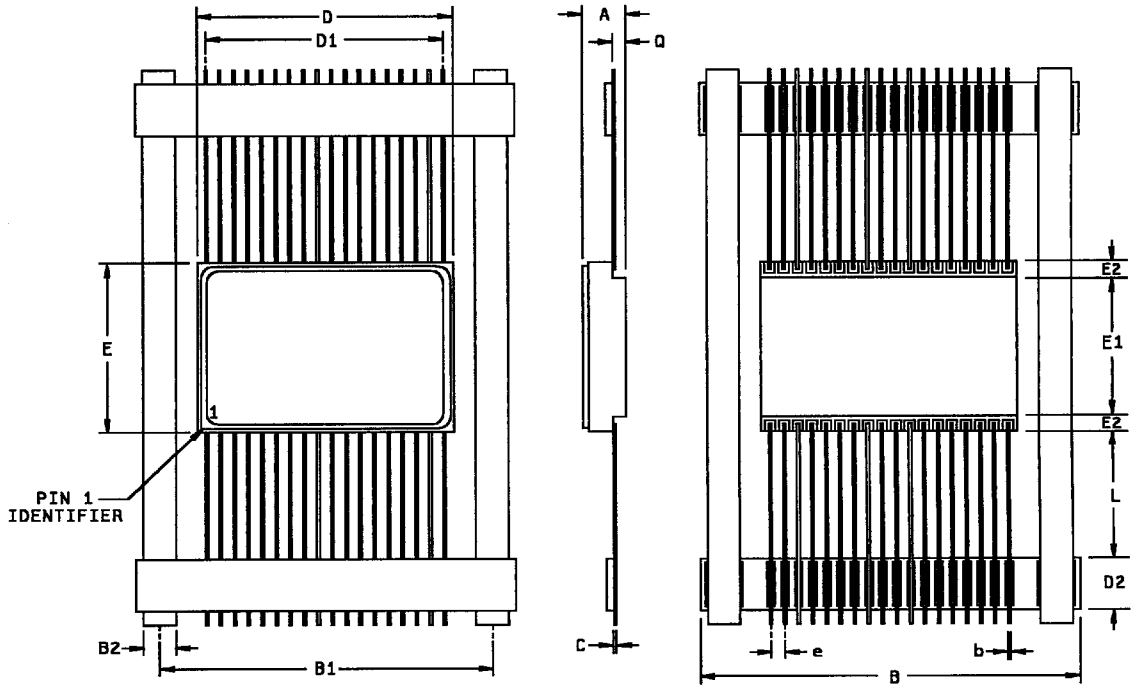


Figure 1. Case outline(s) - Continued.

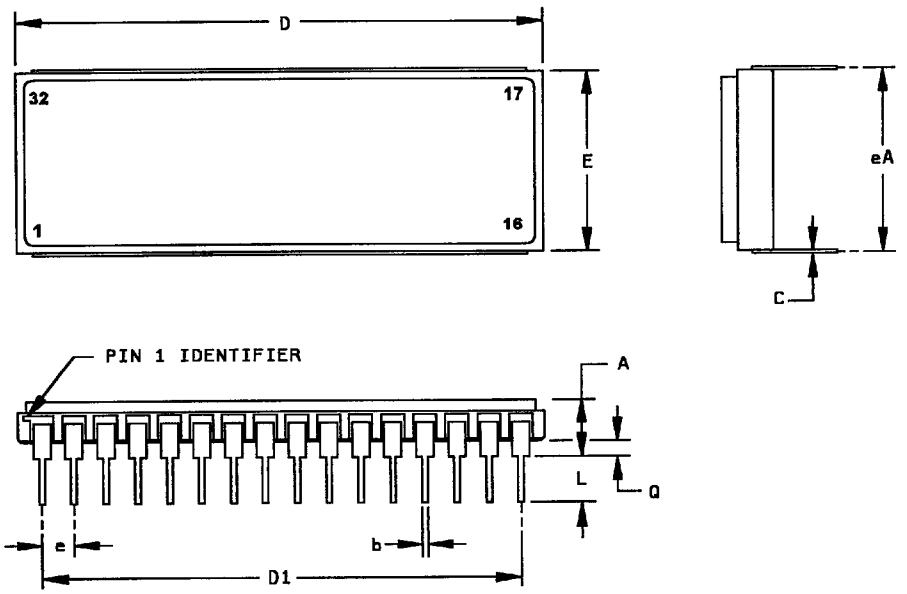
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.31	3.18	0.091	0.125
b	0.38	0.48	0.015	0.019
B	37.70	38.50	1.485	1.515
B1	32.64 TYP.		1.285 TYP.	
B2	3.80 TYP.		0.150 TYP.	
C	0.08	0.18	0.003	0.007
D	23.11	23.62	0.910	0.930
D1	21.46	21.72	0.845	0.855
D2	4.83	5.33	0.190	0.210
e	1.27 BSC		0.050 BSC	
E	12.83	13.08	0.505	0.515
E1	9.78	10.03	0.385	0.395
E2	1.40	1.65	0.055	0.065
L	12.19	13.21	0.480	0.520
Q	0.38	0.64	0.015	0.025

NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline Y.

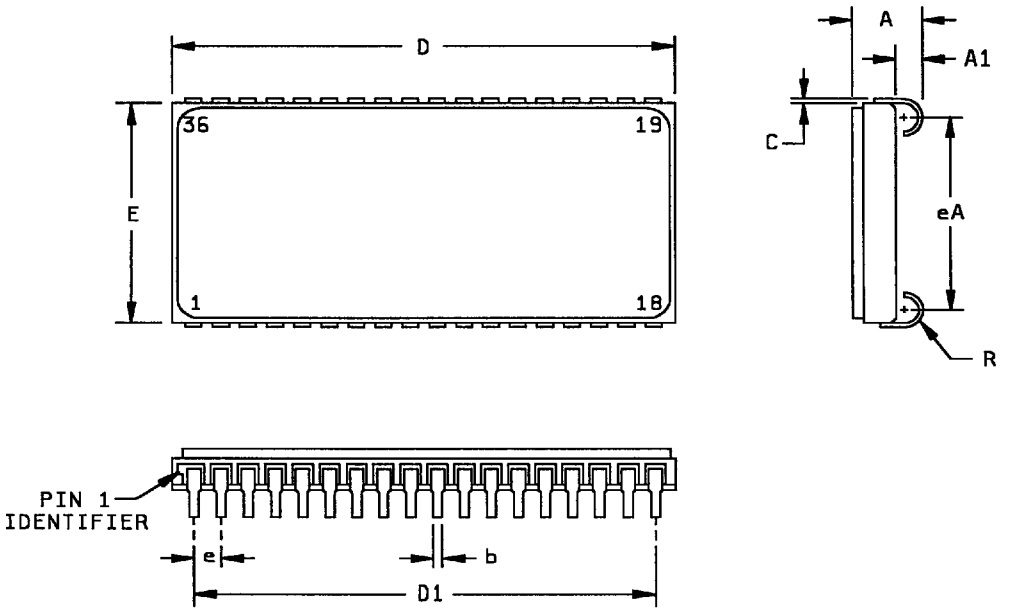


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.70	5.10	0.144	0.200
b	0.41	0.51	0.016	0.020
c	0.20	0.30	0.008	0.012
D	42.00	42.80	1.654	1.686
D1	37.90	38.30	1.492	1.508
E	14.80	15.40	0.581	0.605
e	2.50 BSC		0.100 BSC	
eA	15.00	15.50	0.590	0.610
L	3.18	4.90	0.125	0.193
Q	0.48	1.19	0.019	0.047

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - continued.

Case outline Z.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.45	4.67	0.136	0.184
A1	1.02	1.52	0.040	0.060
b	0.38	0.48	0.015	0.019
C	0.15	0.25	0.006	0.010
D	23.12	23.62	0.910	0.930
D1	21.46	21.72	0.845	0.855
E	10.08	11.05	0.425	0.435
e	1.27 TYP.		0.050 TYP.	
eA	9.30	9.80	0.366	0.386
R	0.89 TYP.		0.035 TYP.	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines(s) - Continued.

Device type	All	Device type	All
Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	17	A8
2	A1	18	A9
3	A2	19	A10
4	A3	20	A11
5	$\overline{CS}$	21	A12
6	I/O0	22	I/O4
7	I/O1	23	I/O5
8	V_{CC}	24	V_{CC}
9	GND	25	GND
10	I/O2	26	I/O6
11	I/O3	27	I/O7
12	$\overline{WE}$	28	$\overline{OE}$
13	A4	29	A13
14	A5	30	A14
15	A6	31	A15
16	A7	32	A16

FIGURE 2. Terminal connections.

Device type	All	Device type	All
Case outlines	T,Y	Case outlines	T,Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	17	I/O3
2	A16	18	I/O4
3	A14	19	I/O5
4	A12	20	I/O6
5	A7	21	I/O7
6	A6	22	$\overline{CS}$
7	A5	23	A10
8	A4	24	$\overline{OE}$
9	A3	25	A11
10	A2	26	A9
11	A1	27	A8
12	A0	28	A13
13	I/O0	29	$\overline{WE}$
14	I/01	30	NC
15	I/02	31	A15
16	GND	32	V_{CC}

FIGURE 2. Terminal connections - Continued.

Device type	05 - 11	Device type	05 - 11
Case outlines	X,Z	Case outlines	X,Z
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	19	NC
2	A0	20	A8
3	A1	21	A9
4	A2	22	A10
5	A3	23	A11
6	$\overline{CS}$	24	A12
7	I/O0	25	I/O4
8	I/O1	26	I/O5
9	V_{CC}	27	V_{CC}
10	GND	28	GND
11	I/O2	29	I/O6
12	I/O3	30	I/O7
13	$\overline{WE}$	31	$\overline{OE}$
14	A4	32	A13
15	A5	33	A14
16	A6	34	A15
17	A7	35	A16
18	NC	36	NC

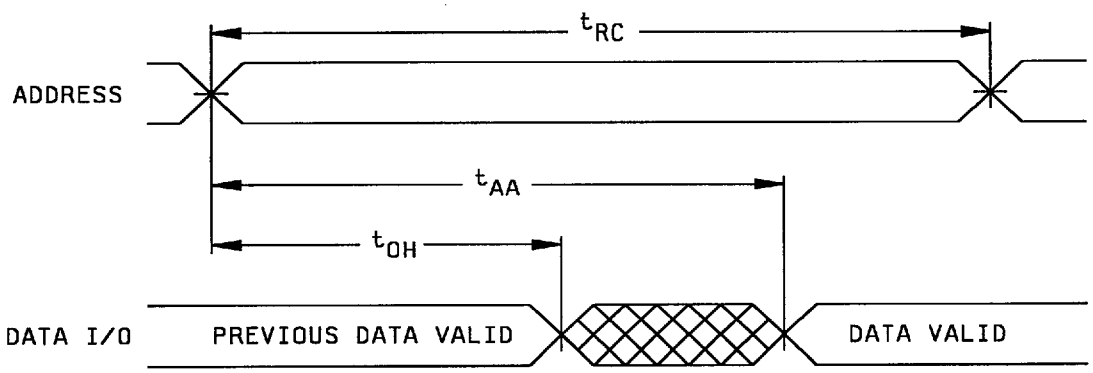
FIGURE 2. Terminal connections - Continued.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Output Disable	High Z	Active

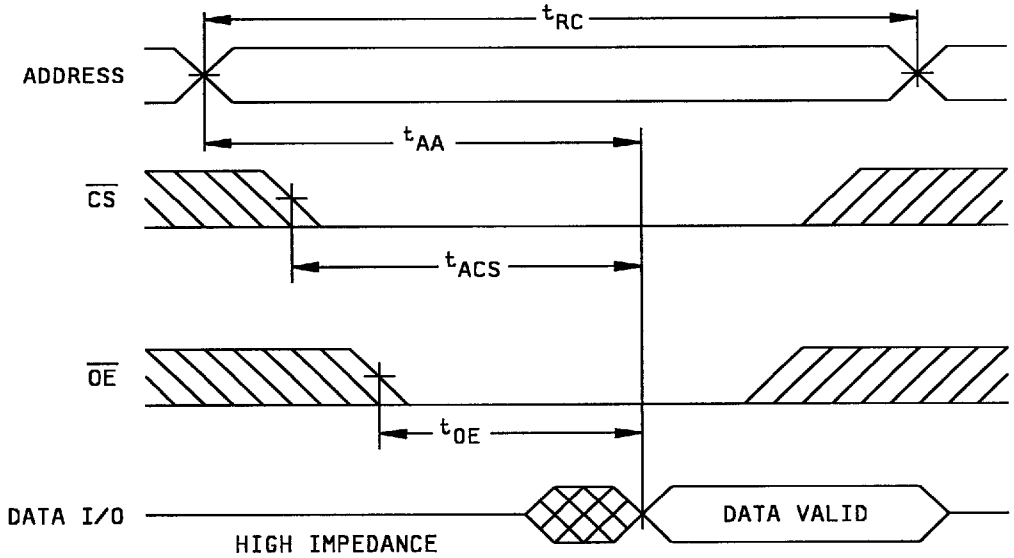
NOTES:

1. H = V_{IH} = High Logic Level
2. L = V_{IL} = Low Logic Level
3. X = Do no care (either high or low)
4. High Z = High Impedance State

FIGURE 3. Truth table.

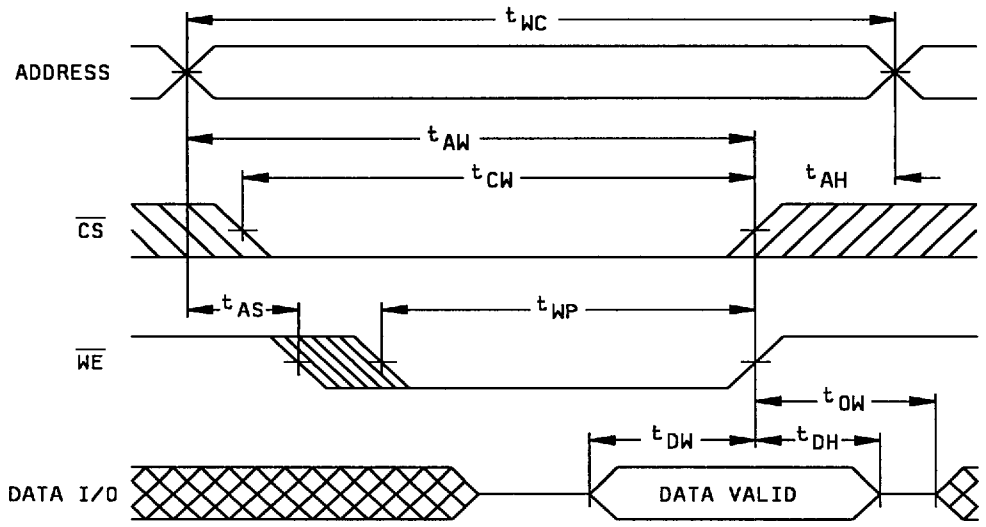


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

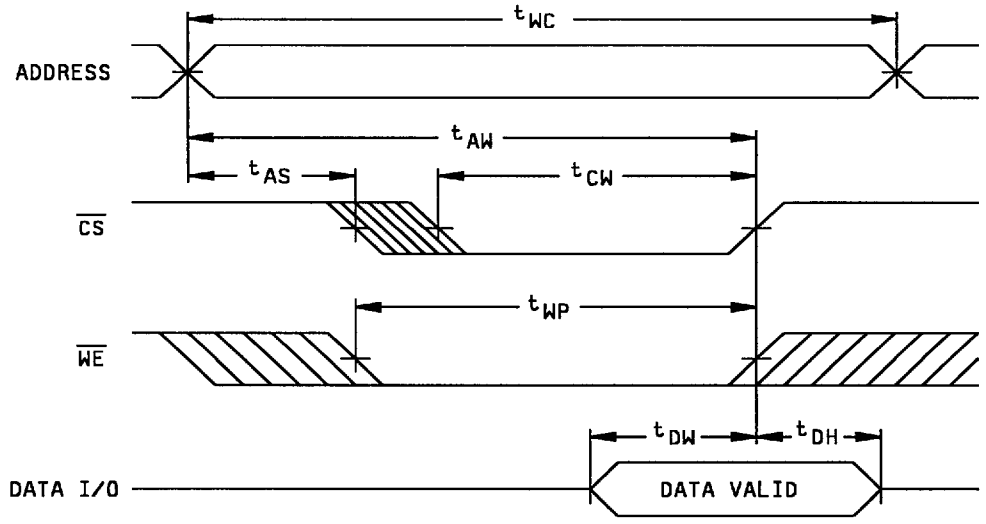


READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIGURE 4. Read cycle timing diagram.



WRITE CYCLE 1 $\overline{WE}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED

FIGURE 5. Write cycle timing diagram.

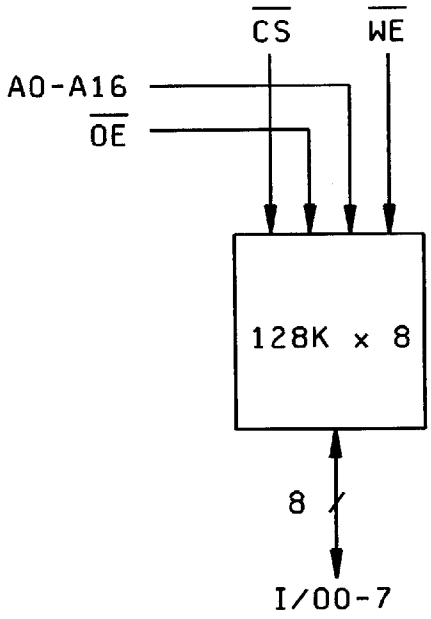
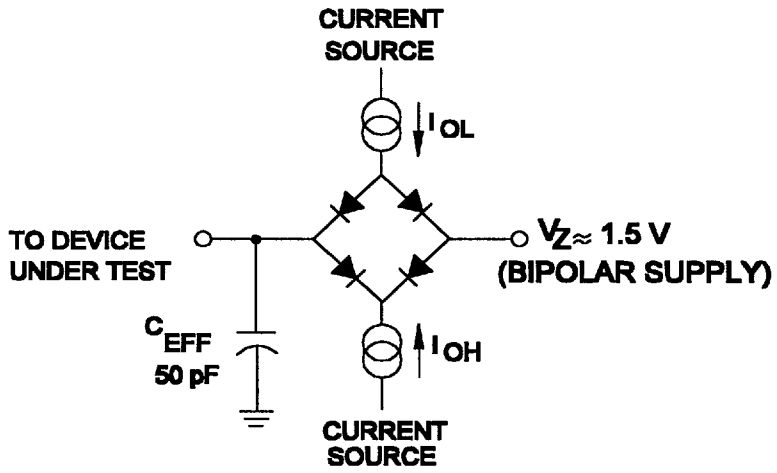


FIGURE 6. Block diagram.



Parameter	Typ.	Unit
Input pulse level	0 - 3.0	V
Input rise and fall	5	ns
Input and output reference level	1.5	V
Output load capacitance	50	pF

NOTES:
1. V_Z is programmable from +2 V to +7 V.
2. I_{OL} and I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance is $Z_0 = 75$ ohms.
4. V_Z is typically the midpoint of V_{OH} and V_{OH}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 7. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*,2,3,4,7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. The devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-06-22

Approved sources of supply for SMD 5962-96691 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9669101HTC	54230	WMS128K8-120DE
5962-9669101HTA	54230	WMS128K8-120DE
5962-9669101HUC	54230	WMS128K8-120DR
5962-9669101HUA	54230	WMS128K8-120DR
5962-9669101HYC	54230	WMS128K8-120C
5962-9669101HYA	54230	WMS128K8-120C
5962-9669102HTC	54230	WMS128K8-100DE
5962-9669102HTA	54230	WMS128K8-100DE
5962-9669102HUC	54230	WMS128K8-100DR
5962-9669102HUA	54230	WMS128K8-100DR
5962-9669102HYC	54230	WMS128K8-100C
5962-9669102HYA	54230	WMS128K8-100C
5962-9669103HTC	54230	WMS128K8-85DE
5962-9669103HTA	54230	WMS128K8-85DE
5962-9669103HUC	54230	WMS128K8-85DR
5962-9669103HUA	54230	WMS128K8-85DR
5962-9669103HYC	54230	WMS128K8-85C
5962-9669103HYA	54230	WMS128K8-85C
5962-9669104HTC	54230	WMS128K8-70DE
5962-9669104HTA	54230	WMS128K8-70DE
5962-9669104HUC	54230	WMS128K8-70DR
5962-9669104HUA	54230	WMS128K8-70DR
5962-9669104HYC	54230	WMS128K8-70C
5962-9669104HYA	54230	WMS128K8-70C

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9669105HTC	54230	WMS128K8-55DE
5962-9669105HTA	54230	WMS128K8-55DE
5962-9669105HUC	54230	WMS128K8-55DR
5962-9669105HUA	54230	WMS128K8-55DR
5962-9669105HXC	54230	WMS128K8-55F
5962-9669105HYC	54230	WMS128K8-55C
5962-9669105HYA	54230	WMS128K8-55C
5962-9669105HZC	54230	WMS128K8-55DJ
5962-9669105HZA	54230	WMS128K8-55DJ
5962-9669106HTC	54230	WMS128K8-45DE
5962-9669106HTA	54230	WMS128K8-45DE
5962-9669106HUC	54230	WMS128K8-45DR
5962-9669106HUA	54230	WMS128K8-45DR
5962-9669106HXC	54230	WMS128K8-45F
5962-9669106HYC	54230	WMS128K8-45C
5962-9669106HYA	54230	WMS128K8-45C
5962-9669106HZC	54230	WMS128K8-45DJ
5962-9669106HZA	54230	WMS128K8-45DJ
5962-9669107HTC	54230	WMS128K8-35DE
5962-9669107HTA	54230	WMS128K8-35DE
5962-9669107HUC	54230	WMS128K8-35DR
5962-9669107HUA	54230	WMS128K8-35DR
5962-9669107HXC	54230	WMS128K8-35F
5962-9669107HYC	54230	WMS128K8-35C
5962-9669107HYA	54230	WMS128K8-35C
5962-9669107HZC	54230	WMS128K8-35DJ
5962-9669107HZA	54230	WMS128K8-35DJ
5962-9669108HTC	54230	WMS128K8-25DE
5962-9669108HTA	54230	WMS128K8-25DE
5962-9669108HUC	54230	WMS128K8-25DR
5962-9669108HUA	54230	WMS128K8-25DR
5962-9669108HXC	54230	WMS128K8-25F
5962-9669108HYC	54230	WMS128K8-25C
5962-9669108HYA	54230	WMS128K8-25C
5962-9669108HZC	54230	WMS128K8-25DJ
5962-9669108HZA	54230	WMS128K8-25DJ

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9669109HTC	54230	WMS128K8-20DE
5962-9669109HTA	54230	WMS128K8-20DE
5962-9669109HUC	54230	WMS128K8-20DR
5962-9669109HUA	54230	WMS128K8-20DR
5962-9669109HXC	54230	WMS128K8-20F
5962-9669109HYC	54230	WMS128K8-20C
5962-9669109HYA	54230	WMS128K8-20C
5962-9669109HZC	54230	WMS128K8-20DJ
5962-9669109HZA	54230	WMS128K8-20DJ
5962-9669110HTC	54230	WMS128K8-17DE
5962-9669110HTA	54230	WMS128K8-17DE
5962-9669110HUC	54230	WMS128K8-17DR
5962-9669110HUA	54230	WMS128K8-17DR
5962-9669110HXC	54230	WMS128K8-17F
5962-9669110HYC	54230	WMS128K8-17C
5962-9669110HYA	54230	WMS128K8-17C
5962-9669110HZC	54230	WMS128K8-17DJ
5962-9669110HZA	54230	WMS128K8-17DJ
5962-9669111HTC	54230	WMS128K8-15DE
5962-9669111HTA	54230	WMS128K8-15DE
5962-9669111HUC	54230	WMS128K8-15DR
5962-9669111HUA	54230	WMS128K8-15DR
5962-9669111HXC	54230	WMS128K8-15F
5962-9669111HYC	54230	WMS128K8-15C
5962-9669111HYA	54230	WMS128K8-15C
5962-9669111HZC	54230	WMS128K8-15DJ
5962-9669111HZA	54230	WMS128K8-15DJ

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
54230	Bowmar Instrument Corporation White Microelectronics Division 3601 East University Drive Phoenix, AZ 85034-7217

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.