Preliminary Information   Low Power, Battery Backup, 2-Wire™

XICOR®

Real Time Clock/Calendar with Event/Timestamp Detection & Alarms   X1209
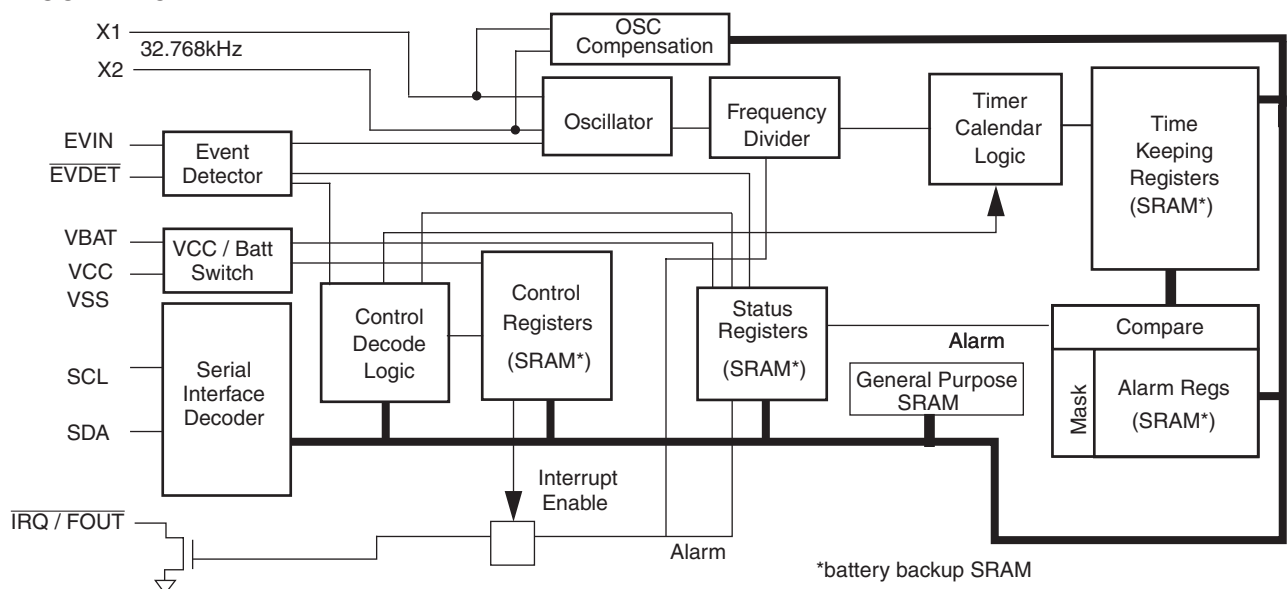
FEATURES

- **Real Time Clock/Calendar**
  - **—Tracks time in Hours, Minutes, and Seconds**
  - **—Day of the Week, Day, Month, and Year**
- **Security and Event Functions**
  - **—Tamper detection with Time stamp**
  - **—Event alarm operation to 1.8V**
  - **—Low power operations. Selectable sampling rates.**
  - **—Selectable Glitch filter on Event Monitor Input**
- **Pulse Interrupt for periodic IRQ**
- **Selectable Dividers for Various Frequency Output**
- **1 Polled Alarm**
  - **—Settable on the Second, Minute, Hour, Day of the Week, Day, or Month**
  - **—Pulse Interrupt for periodic IRQ**
- **Battery Switch or Super Cap Input**
- **Battery Backup SRAM Timing and Alarm Registers**
- **Power Failure Detection**
- **Oscillator Compensation on chip**
- **2 Bytes General Purpose SRAM**
- **2-Wire™ Interface**
  - **—400kHz data transfer rate**
- **Low Power CMOS**
  - **—< 1µA Operating Current**
- **Small Package Options**
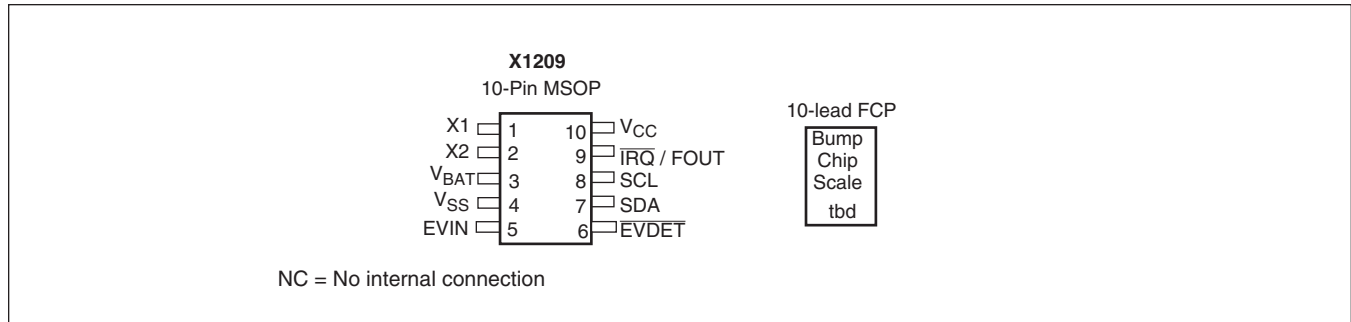 - **—10-Lead MSOP and FCP (Flip chip)**

APPLICATIONS

- **Security or Anti-Tampering Applications**
- **Panel / Enclosure Status**
- **Warranty Reporting**
- **Time Stamping Applications**
- **Event Recording / Data Logging**
- **Patrol/Security Checkpoint Management**
- **Facility Safety Check (Fire or Light Equipment)**
- **Production Line Check & Management**
- **Vending Machine Management**
- **Other: Utility Meters, HVAC Equipment, Audio / Video Components, Set Top Box / Television, Modems, Network Routers, Hubs, Switches, Bridges, Cellular Infrastructure Equipment, Fixed Broadband Wireless Equipment, Pagers / PDA, POS Equipment, Test Meters / Fixtures, Data Acquisition Systems, Office Automation (Copiers, Fax), Home Appliances, Computer Products, Other Industrial / Medical / Automotive**

BLOCK DIAGRAM

PIN DESCRIPTIONS

X1209
10-Pin MSOP

```
X1   ⊏ 1      10 ⊐ V_CC
X2   ⊏ 2       9 ⊐ IRQ / FOUT
V_BAT ⊏ 3      8 ⊐ SCL
V_SS ⊏ 4       7 ⊐ SDA
EVIN ⊏ 5       6 ⊐ EVDET
```

10-lead FCP

```
┌──────┐
│Bump  │
│Chip  │
│Scale │
│ tbd  │
└──────┘
```

NC = No internal connection

PIN ASSIGNMENTS

Pin Number		Symbol	Brief Description
MSOP	FCP		
1		X1	**X1.** The X1 pin is the input of an inverting amplifier. An external 32.768kHz quartz crystal is used with the X1209 to supply a timebase for the real time clock. The device can also be driven directly from a 32.768kHz source. Internal compensation circuitry is included to form a complete oscillator circuit with accuracy over the operating temperature range from -40C to +85C. The oscillator compensation network can be used either calibrate the crystal pull-over accuracy over temperature during manufacturing calibration or used with external temperature sensor and microcontroller for active compensation.
2		X2	**X2.** The X2 pin is the output of an inverting amplifier. An external 32.768kHz quartz crystal is used with the X1209 to supply a timebase for the real time clock. The device can also be driven directly from a 32.768kHz source. Internal compensation circuitry is included to form a complete oscillator circuit with accuracy over the operating temperature range from -40C to +85C. The oscillator compensation network can be used either calibrate the crystal pull-over accuracy over temperature during manufacturing calibration or used with external temperature sensor and microcontroller for active compensation.
3		V_{BAT}	**V_{BAT}.** This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event the V_{CC} supply fails. This pin can be connected to a battery, a Supercap or tied to ground if not used.
4		V_{SS}	**Chip ground pin**
5		EVIN	**Event Input (EVIN).** The EVIN is an input pin that is used to detect an externally monitored event. When a high signal is present at the EVIN pin an "event" is detected. Upon a valid detection, the X1209 has the option to 1) provide a flag signal at the EVDET pin (open drain, active low), 2) record a time stamp when the event occurred, 3) set a status bit (EVT bit). Note that on detection the EVT bit is set then the EVDET pin is pulled low. The EVIN pin can be optionally connected (see EVINEB bit) to an internal pull up current source that operates to 1uA (always on mode). User selectable event sampling modes are also available for low power applications with 1/4-Hz, 1-Hz and 2-Hz sample detection rates. The EVIN input is pulsed ON/OFF when in sampling mode for power savings advantages.
6		EVDET	
7		SDA	**Serial Data (SDA).** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. The input buffer is always active (not gated). An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz 2-wire interface speeds. Disabled when the backup power supply on the V_{BAT} pin is activated.

| Pin Number | | Symbol | Brief Description |
MSOP	FCP		
8		SCL	**Serial Clock (SCL).** The SCL input is used to clock all data into and out of the device. The input buffer on this pin is always active (not gated). Disabled when the backup power supply on the V_{BAT} pin is activated.
9		$\overline{IRQ}$/ FOUT	**Interrupt Output – $\overline{IRQ}$, Frequency Output– FOUT.** Multi-functional pin set via configuration register that can be used as interrupt or frequency output pin. Interrupt Mode. This is an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active low output.This mode is selected via the frequency out control bits. Frequency Output Mode. This is an frequency output pin. The frequency output is user selectable and enabled via the 2-wire bus. This mode is selected via the frequency out control bits.
10		V_{CC}	**Chip supply pin.**

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .... -65°C to +135°C
Storage Temperature......................... -65°C to +150°C
Voltage on V_{CC}, VBAT and $\overline{IRQ}$
pin (respect to ground) ....-0.5V to 7.0V
Voltage on SCL, SDA, X1 and X2
pin (respect to ground) .... -0.5V to 7.0V or 0.5V
Lead Temperature (Soldering, 10 sec) ....300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS - RTC (Temperature = -40°C to +85°C, unless otherwise stated.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{CC}	Main Power Supply		2.0		5.5	V	
VBAT	Backup Power Supply		1.8		5.5	V	
V_{MW}	Voltage Trip Memory Write Valid			2.0		V	Trip point for supply switch over
V_{CB}	Switch to Backup Supply	$V_{CC} < V_{MW}$	VBAT - 50		VBAT + 50	mV	
V_{BC}	Switch to Main Supply	$V_{CC} > V_{MW}$	VBAT		VBAT + 50	mV	
V_{HYST1}	Voltage Hysteresis			±50		mV	Vcc to Vbat
V_{HYST2}	Voltage Hysteresis			+50		mV	Vbat to Vcc

OPERATING CHARACTERISTICS - RTC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
I_{CC1}	Active Supply Current (SRAM Read)	V_{CC} = 2.0V			1	µA	1, 5, 7, 14
		V_{CC} = 2.7V			1	µA	
		V_{CC} = 5.0V			1	µA	
I_{CC2}	Active Supply Current (SRAM Write)	V_{CC} = 2.0V			2		
		V_{CC} = 2.7V			2	mA	2, 5, 7, 14
		V_{CC} = 5.0V			2	mA	
I_{CC3}	Main Timekeeping Current	V_{CC} = 2.0V		500	700	nA	
		V_{CC} = 2.7V		500	700	nA	3, 7, 8, 14, 15
		V_{CC} = 5.0V		500	700	nA	
I_{BACK}	Timekeeping Current (during V_{BAT} supply ON)	VBAT = 1.8V		250	500	nA	3, 6, 9, 14, 15
		VBAT = 3.0V		250	500	nA	
I_{LB}	VBAT Leakage Current	VBAT = 1.8V		25	50	nA	
		VBAT = 3.0V		25	50		
I_{LI}	Input Leakage Current				10	µA	10
I_{LO}	Output Leakage Current				10	µA	10
V_{IL}	Input LOW Voltage		-0.5		V_{CC} x 0.2 or VBAT x 0.2	V	13
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7 or VBAT x 0.7		V_{CC} + 0.5 or VBAT + 0.5	V	13
V_{OL}	Output LOW Voltage for SDA/$\overline{IRQ}$	V_{CC} = 2.7V			0.4	V	11
		V_{CC} = 5.5V			0.4		

DC OPERATING CHARACTERISTICS - EVENT DETECTION CIRCUITS
(Temperature = -40°C to +85°C, unless otherwise stated.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{IH}	Voltage Input Logic High for EVIN pin					V	
V_{IL}	Voltage Input Logic Low for EVIN pin					V	
V_{OH}	Voltage Output Logic High for EVDET pin					V	
V_{OL}	Voltage Output Logic High for EVDET pin					V	
R_{SW}	Switch Resistance on EVIN pin					ohm	

OPERATING CHARACTERISTICS - EVENT DETECTION CIRCUITS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
I_{CC4}	Active Supply Current (Sampled Event Detection)	EVIN always on		1.25		µA	
		EVIN: 1/4 Hz				µA	
		EVIN: 1 Hz				µA	
		EVIN: 2 Hz				µA	
I_{CC5}	Standby Current (EVIN)	EVIN disabled				nA	
I_L	Input Leakage Current $\overline{EVDET}$ pin						
t_{EVT1}	Time EVIN valid high to EVT bit valid high	VCC =		$x + t_{HYS}$			
		VBAT =		$y + t_{HYS}$			
t_{EVT2}	Time EVT bit valid high to EVDET pin valid low	VCC =					
		VBAT =					
t_{EVT3}	Time from EVT bit valid high to RTC stamp valid	VCC =					
		VBAT =					
t_{HYS}	Time based hysteresis on EVIN pin			0		ms	
				3.9			
				15.625			
				31.25			
						%	
t_{PULSE}	Sample Rate of EVIN pin			0		Hz	
				0.25			
				1			
				2			
						%	

Notes: (1) The device enters the Active state after any start, and remains active: for 9 clock cycles if the Device Select Bits in the Slave Address Byte are incorrect or until 200nS after a stop ending a read or write operation.
    (2) The device enters the Program state 200nS after a stop ending a write operation and continues for t_{WC}.
    (3) The device goes into the Timekeeping state 200nS after any stop; or 9 clock cycles after any start that is not followed by the correct Device Select Bits in the Slave Address Byte.
    (4) For reference only and not tested.
    (5) $V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9, f_{SCL} = 400KHz
    (6) V_{CC} = 0V
    (7) VBAT = 0V
    (8) $V_{SDA} = V_{SCL} = V_{CC}$, Others = GND or V_{CC}
    (9) $V_{SDA} = V_{SCL}$=VBAT, Others = GND or VBAT, Note SDA and SCL disabled internally when V_{BAT} supply is ON
    (10) V_{SDA} = GND or V_{CC}, V_{SCL} = GND or V_{CC}
    (11) I_{OL} = 3.0mA at 5V, 1mA at 2.7V
    (13) Threshold voltages based on the higher of Vcc or VBAT.
    (14) Using recommended crystal and oscillator network applied to X1 and X2 (25°C).
    (15) Typical values are for T_A = 25°C

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C_{OUT}[1]	Output Capacitance (SDA, $\overline{IRQ}$)	10	pF	V_{OUT} = 0V
C_{IN}[1]	Input Capacitance (SCL)	10	pF	V_{IN} = 0V

Notes: (1) This parameter is not 100% tested.
    (2) The input capacitance between x1 and x2 pins can be varied between 5pF and 19.75pF by using analog trimming registers

AC CHARACTERISTICS - SERIAL BUS

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5
Output Load	Standard Output Load

### Figure 1. Standard Output Load for testing the device with V_{CC} = 5.0V

Equivalent AC Output Load Circuit for V_{CC} = 5V
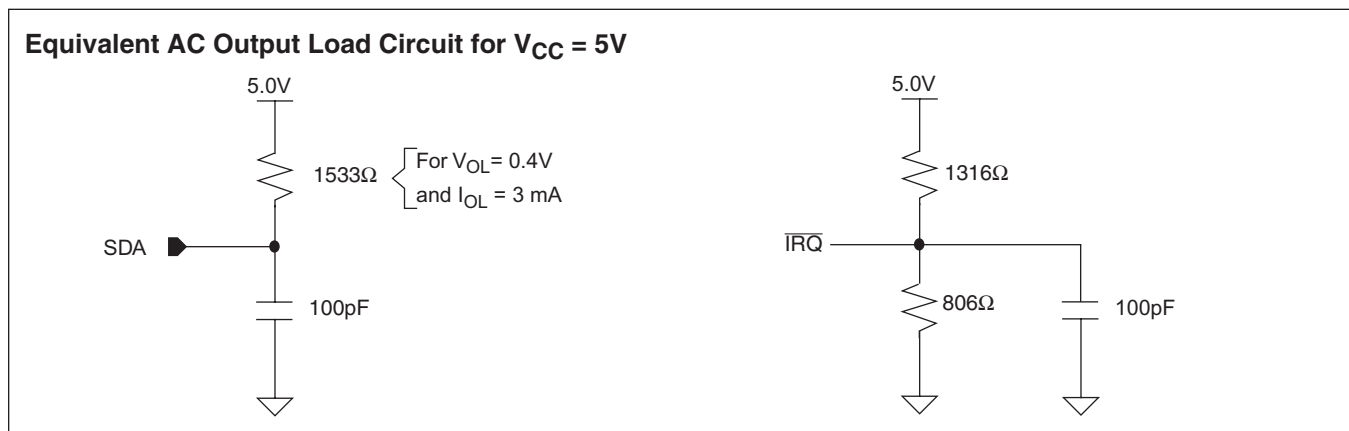
AC Specifications - Serial Bus (T_A = -40°C to +85°C, V_{CC} = +2.7V to +5.5V, unless otherwise specified.)

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency		400	kHz
t_{IN}	Pulse width Suppression Time at inputs	50[1]		ns
t_{AA}	SCL LOW to SDA Data Out Valid		0.9	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		μs
t_{LOW}	Clock LOW Time	1.3		μs
t_{HIGH}	Clock HIGH Time	0.6		μs
$t_{SU:STA}$	Start Condition Setup Time	0.6		μs
$t_{HD:STA}$	Start Condition Hold Time	0.6		μs
$t_{SU:DAT}$	Data In Setup Time	100		ns
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:STO}$	Stop Condition Setup Time	0.6		μs
t_{DH}	Data Output Hold Time	50		ns
t_R	SDA and SCL Rise Time	20 +.1Cb[1][2]	300	ns
t_F	SDA and SCL Fall Time	20 +.1Cb[1][2]	300	ns
Cb	Capacitive load for each bus line		400	pF

Notes: (1) This parameter is not 100% tested.
        (2) Cb = total capacitance of one bus line in pF.

TIMING DIAGRAMS

Bus Timing
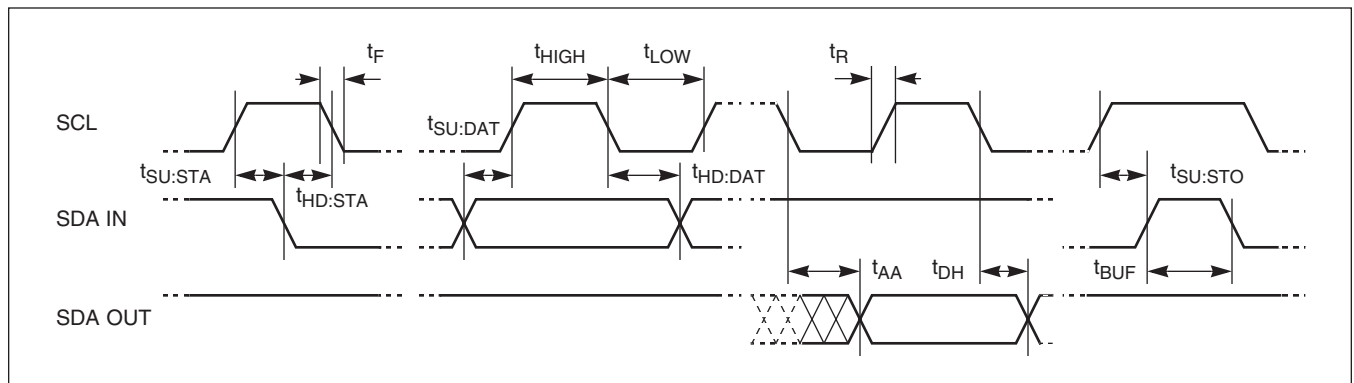
Write Cycle Timing
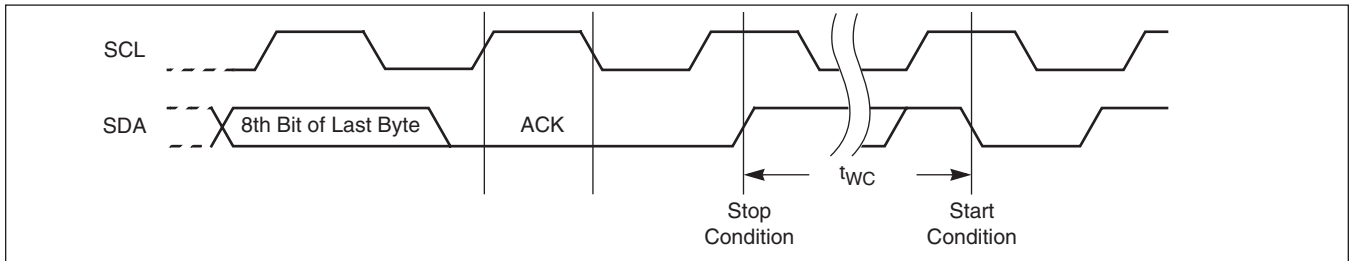
Power Up Timing

Symbol	Parameter	Min.	Typ.[2]	Max.	Units
t_{PUR}[1]	Time from Power Up to Read			1	ms
t_{PUW}[1]	Time from Power Up to Write			5	ms

Notes: (1) Delays are measured from the time V_{CC} is stable until the specified operation can be initiated. These parameters are not 100% tested. V_{CC} slew rate should be between 0.2mV/μsec and 50mV/μsec.
(2) Typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$

DESCRIPTION

The X1209 device is a low power Real Time Clock with crystal and timing compensation, tamper or event detection, clock/calendar, one polled alarm, power indicator, periodic and polled alarms and battery backup switch.

The oscillator uses an external, low-cost 32.768kHz crystal. The Real-Time Clock keeps track of time with separate registers for Hours, Minutes, and Seconds. The Calendar has separate registers for Date, Month, Year and Day-of-week. The calendar is correct through 2099, with automatic leap year correction.

The powerful alarm can be set to any Clock/Calendar value for a match. For instance, every minute, every Tuesday, or 5:23 AM on March 21. The alarm can be polled in the Status Register or provide a hardware interrupt ($\overline{IRQ}$ Pin). There is a repeat mode for the alarms allowing a periodic interrupt of 60-seconds, 1-hour, 1-day, once-a-week, etc.

The device offers a backup power input pin. This VBAT pin allows the device to be backed up by battery or SuperCap. The entire X1209 device is fully operational from 2.0V to 5.5 volts and the clock/calendar portion of the X1209 device remains fully operational down to 1.8 volts (Standby Mode).

The event detection function can be used for tamper detection, security or other chassis or generic system monitoring. Upon a valid event detection, the X1209 provides the following options: 1) to issue an event output signal pin ($\overline{EVDET}$), 2) to sets an event detection bit (EVT bit) in the status register and 3) to store the timestamp when the event occured. The event monitor can function in both main VCC and battery backup modes. For low power savings the event monitor can be configured for various input detection rates. The event input monitor pin (EVIN) also has a selectable glitch filter to avoid switch de-bouncing.

PIN DESCRIPTION

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device. The input buffer on this pin is always active (not gated). Disabled when the backup power supply on the V_{BAT} pin is activated.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. The input buffer is always active (not gated).

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz 2-wire interface speeds. Disabled when the backup power supply on the V_{BAT} pin is activated.

V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event the V_{CC} supply fails. This pin can be connected to a battery, a Supercap or tied to ground if not used.

Interrupt Output – $\overline{IRQ}$, Frequency Output– FOUT

Multi-functional pin set via configuration register that can be used as interrupt or frequency output pin.

Interrupt Mode. This is an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active low output. This mode is selected via the frequency out control bits.

Frequency Output Mode. This is an frequency output pin. The frequency output is user selectable and enabled via the 2-wire bus. This mode is selected via the frequency out control bits.

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the X1209 to supply a timebase for the real time clock. The device can also be driven directly from a 32.768kHz source. Internal compensation circuitry is included to form a complete oscillator circuit with accuracy over the operating temperature range from -40C to +85C. The oscillator compensation network can be used either calibrate the crystal pull-over accuracy over temperature during manufacturing calibration or used with external temperature sensor and microcontroller for active compensation.

Event Input (EVIN)

The EVIN is an input pin that is used to detect an externally monitored event. When a high signal is present at the EVIN pin an "event" is detected. Upon a valid detection, the X1209 has the option to 1) provide a flag signal at the $\overline{EVDET}$ pin (open drain, active low), 2) record a time stamp when the event occurred, 3) set a status bit (EVT bit). Note that on detection the EVT bit is set then the $\overline{EVDET}$ pin is pulled low.

The EVIN pin can be optionally connected (see EVINEB bit) to an internal pull up current source that operates to 1uA (always on mode). User selectable event sampling modes are also available for low power applications with 1/4-Hz, 1-Hz and 2-Hz sample detection rates. The EVIN input is pulsed ON/OFF when in sampling mode for power savings advantages.

The EVIN also has a user selectable time based hystersis filter (see EHYS bits) to "filter out" circuit debouncing and noise during an event detection. The EVIN signal must be high for the duration of the time filter. The time filter can be selected from 0 time delay (no time based hysteresis) to 3.9ms (2048Hz), 15.625ms (512Hz), or 31.25ms (256Hz).

The event detection circuit can be user enabled/disabled (see EVEN bit) and has the option to be operational in battery backup modes (see EVBATB bit). When the event detection is disabled the EVIN pin is gated OFF. See Functional Description for more details.
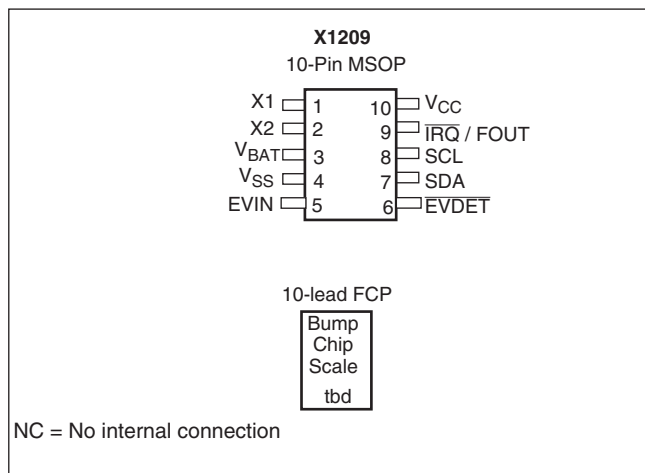
Figure 2. Recommended Crystal connection
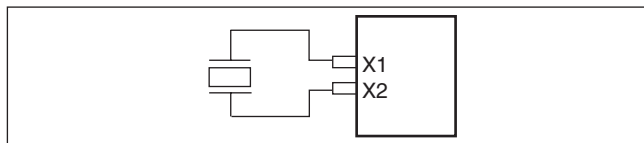
VCC, VSS

Chip supply and ground pins.

PIN OUT

NC = No internal connection

FUNCTIONAL DESCRIPTION

POWER CONTROL OPERATION

The power control circuit accepts a V_{CC} and a VBAT input. Many types of batteries can be used with the Xicor RTC products. 3.0V or 3.6V Lithium batteries are appropriate, and sizes are available that can power a Xicor RTC device for up to 10 years. Another option is to use a supercapacitor for applications where Vcc may disappear intermittently for short periods of time. See application for more information.

Normal Mode (V_{CC}) to Battery Backup Mode (V_{BAT}).

To transition from VCC to VBAT source, the following conditions must exist:

Condition 1: $V_{CC} < V_{BAT} - V_{HYS}$, where V_{HYS1} is +/- 50mV.

and

Condition 2: $V_{CC} < V_{MW}$, where V_{MW} is ~1.8V.

Battery Backup Mode (V_{BAT}) to Normal Mode (V_{CC}).

To transition from VBAT to VCC source, the following conditions must exist:

$V_{CC} > V_{MW} + V_{HYS2}$, where V_{HYS2} is + 50mV.

Power Failure Detection.

The X1209 provides a Real Time Clock Failure Bit (RTCF) to detect total power failure

Low Power Modes.

The X1209...

Other Notes.

The 2-wire bus is inactive in battery backup mode. The Status Register and the Alarm Registers are operational during battery backup mode. All the inputs and outputs of the X1209 are active during battery backup mode unless disabled via the control register. The User SRAM is operational in battery backup mode down to 1.8V.

POWER RAMP RATE

The power ramp rate recommended is....

REAL TIME CLOCK OPERATION

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day, date, month, and year. The RTC has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the X1209 powers up after the loss of both V_{CC} and VBAT, the clock will not operate until at least one byte is written to the clock register.

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal's nominal frequency. For example, a >20ppm frequency deviation translates into an accuracy of >1 minute per month. These parameters are available from the crystal manufacturer. Xicor's RTC family provides on-chip crystal compensation networks to adjust load-capacitance to tune oscillator frequency from +185 ppm to –94 ppm (calculated). For more detail information see the Application Notes.

Standard and Pulse Interrupt Alarm Modes

The alarm mode is enabled via the ALME bit. Choosing standard and pulse (repetitive) interrupt alarm mode is selected via the IM bit. Note that when the frequency output function is enabled the alarm function is disabled.

The standard alarm allows for time alarms for time, date, day of the week and year. When a time alarm occurs a $\overline{IRQ}$ pin will be pulled low and the alarm status bit (ALM) will be set to "1".

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence an repetitive or recurring alarm can be set for every n^{th} second, or n^{th} minute, or n^{th} hour, or n^{th} date, or for the same day of the week. The pulsed interrupt mode can be considered a repetitive interrupt mode, with the repetition rate set by the time setting of the alarm. During a pulsed interrupt mode, the $\overline{IRQ}$ pin will be pulled low for 250ms and the alarm status bit (ALM) will be set to "1".

Note the ALM bit can be reset by the user or cleared automatically using the auto reset mode (see ARST bit).

The alarm function can be enabled / disable during battery backup mode using the FOBATB bit.

Frequency Output Mode

The X1209 has the option to provide a frequency output signal using the $\overline{IRQ}$ / FOUT pin. The frequency output mode is bit by configuring the using the FO bits to select 16 possible output frequency values from 0 Hz to 32 kHz. The frequency output can enabled / disable during battery backup mode using the FOBATB bit.

General Purpose User SRAM

The X1209 provides 2 bytes of user SRAM. The SRAM will also operate in battery backup mode. However the 2-wire bus is disabled in battery backup mode.

2-wire Serial Interface

The X1209 provides a 2-wire serial bus interface provides access to the control and status registers, and the user SRAM. The 2-wire serial interface is compatible with other industry 2-wire serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

Oscillator Compensation

The X1209 provides the option of timing correction due to temperature variation of the crystal oscillator for either manufacturing calibration or active calibration. The total possible compensation is +167ppm to -94ppm (calculated). Compensation can be implemented using the following:

1) The X1209 provides a digital trimming register (DTR register) that can be used for adjust the timing counter by ±60 ppm.

2) In addition, the X1209 provides an analog trimming (ATR) registers that can be used to adjust an on-chip digital capacitor for oscillator capacitance trimming. The digital capacitor is selectable from a range of 9pF to 40.5pF (based upon 32.758 kHz) this translates to calculated compensation from approximately +127 ppm to -34 ppm.

An optional circuit is provided to allow for capacitance adjustment of the crystal capacitance when the X1209 switches from V_{CC} to battery backup mode.

Event / Tamper Monitor and Detection

The X1209 provides a event detection and alarm function to be used in a wide variety of applications ranging from security, warranty monitoring, data collection and recording.

The tamper detect input pin, EVIN, can be used as a event or tamper detection input of an external switch (mechanical or electronic). When the EVIN pin is a valid HIGH, the X1209 provides the following detection options: 1) record the time of the event detection, 2) issue a event detection alarm (via the $\overline{EVDET}$ pin) and/ or 3) set an event detection bit (EVT bit) in the status register.

To allow for flexibility of external switches used at the EVIN pin, the internal pullup (~1uA in full on mode) can be disabled/enabled. This will allow for external pullup currents and allow more flexibility depending on the capacitive and resistive loading at the EVIN pin.

A noise filter option is also provided for the event monitor circuit. The EVIN pin has a time base filter where the EVIN signal must be stable for the given time filter to trigger a valid detection. The time hysteresis filter can vary from 0, 3.9ms, 15.62ms or 31.25ms.

For low power applications, the event monitor can be sampled at a user selectable rate. The EVIN pin can be always ON or periodically sampled every 1/4, 1, or 2 Hz.

The X1209 can operate independently or in conjunction with a microcontroller for low power operation modes or in battery backup modes.

The event detection circuits operate is either main Vcc power or battery backup mode.

REGISTER DESCRIPTION

CLOCK/CONTROL REGISTERS (CCR)

The Control/Clock Registers are located in an area accessible following a slave byte of "1101111x" and reads or writes to addresses [0000h:0013h]. (Note: 014:015h are reserved for manufacturing purposes) The defined addresses and default values are described in the Table 1. Writing to and reading from the undefined addresses are not recommended.

CCR access

The contents of the CCR can be modified by performing a byte or a page write operation directly to any address in the CCR. Prior to writing to the CCR (except the status register).

The CCR is divided into 5 sections. These are:

1. Real Time Clock (7 bytes): 00h to 06h addresses.
2. Control and Status (5 bytes): 07h to 0B addresses.
3. Alarm (6 bytes): 0Ch to 11h addresses.
4. User SRAM (2 bytes): 12h to 13h addresses.
5. Reserved for manufacturing (2 byte): 14h to 15h addresses.

Each register is read and written through buffers. SRAM write capability is allowable into the RTC registers (00h to 06h) only when the WRTC bit is set after a valid write operation and stop bit. A sequential read or page write operation provides access to the contents of only one section of the CCR per operation. Access to another section requires a new operation. Continued reads or writes, once reaching the end of a section, will wrap around to the start of the section. A read or write can begin at any address in the CCR.

It is not necessary to set the WRTC bit prior to writing into the control and status, alarm, and user SRAM registers. The device supports a single byte read or write only. Continued reads or writes from this section terminates the operation.

Table 1. Register Memory Map - Clock and Control Registers (CCR)

Addr.	Type	Reg Name	Bit 7	6	5	4	3	2	1	0	Range	Default
00	RTC (SRAM)	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0-59	00h
01		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0-59	00h
02		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0-23	00h
03		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1-31	00h
04		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1-31	00h
05		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0-99	00h
06		DW	0	0	0	0	0	DW2	DW1	DW0	0-6	00h
07	Control / Status	SR	ARST	XTOSCB	reserved	WRTC	EVT	ALM	BAT	RTCF	N/A	01h
08		INT	IM	ALME	LPMODE	FOBATB	FO3	FO2	FO1	FO0	N/A	00h
09		EV	EVIENB	EVBATB	RTCHLT	EVEN	EHYS1	EHYS0	ESMP1	ESMP0	N/A	00h
0A		ATR	BMATR1	BMATR0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0	N/A	00h
0B		DTR	reserved	reserved	reserved	reserved	reserved	DTR2	DTR1	DTR0	N/A	00h
0C	Alarm	SCA	ESCA	ASC22	ASC21	ASC20	ASC13	ASC12	ASC11	ASC10	00-59	00h
0D		MNA	EMNA	AMN22	AMN21	AMN20	AMN13	AMN12	AMN11	AMN10	00-59	00h
0E		HRA	EHRA	0	AHR21	AHR20	AHR13	AHR12	AHR11	AHR10	0-23	00h
0F		DTA	EDTA	0	ADT21	ADT20	ADT13	ADT12	ADT11	ADT10	0-31	00h
10		MOA	EMOA	0	0	AMO20	AMO13	AMO12	AMO11	AMO10	1-12	00h
11		DWA	EDWA	0	0	0	0	ADW12	ADW11	ADW10	0-6	00h
12	User	USR1	USR17	USR16	USR15	USR14	USR13	USR12	USR11	USR10	N/A	00h
13		USR2	USR27	USR26	USR25	USR24	USR23	USR22	USR21	USR20	N/A	00h
14	Reserved		For internal Use Only									
15												

The state of the CCR can be read by performing a random read at any address in the CCR at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. The read instruction latches all Clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read of the CCR will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read of the CCR, the address remains at the previous address +1 so the user can execute a current address read of the CCR and continue reading the next Register.

REAL TIME CLOCK REGISTERS

Addresses [00 hex to 06hex]

Clock/Calendar Registers (SC, MN, HR, DT, MO, YR)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 00 to 59, HR (Hour) can be either a 12-hour or 24-hour mode, (MIL bit = 0) the HR provides 1 to 12 with an AM or PM indicator (H21 bit) or 0 to 23 (with MIL bit = 1), DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99.

Date of the Week Register (DW)

This register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as '0'.

24 Hour Time

If the MIL bit of the HR register is 1, the RTC uses a 24-hour format. If the MIL bit is 0, the RTC uses a 12-hour format and H21 bit functions as an AM/PM indicator with a '1' representing PM. The clock defaults to standard time with H21=0.

Leap Years

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The X1209 does not correct for the leap year in the year 2100.

CONTROL AND STATUS REGISTERS

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register, Event Detection, Analog Trimming and Digital Trimming Registers.

STATUS REGISTER (SR)

The Status Register is located in the CCR memory map at address 07h. This is a volatile register only and provides either control or status of RTC failure, battery mode, alarm trigger, event detection, write protection of clock counter, crystal oscillator enable and auto reset of status bits.

Table 2. Status Register (SR)

Addr	7	6	5	4	3	2	1	0
07h	ARST	XTOSCB	reserved	WRTC	EVT	ALM	BAT	RTCF
Default	0	0	0	0	0	0	0	1

RTCF: Real Time Clock Fail Bit—Volatile

This bit is set to a '1' after a total power failure. This is a read only bit that is set by hardware (X1209 internally) when the device powers up after having lost all power to the device. The bit is set regardless of whether V_{CC} or VBAT is applied first. The loss of only one of the supplies does not result in setting the RTCF bit. The first valid write to the RTC after a complete power failure (writing one byte is sufficient) resets the RTCF bit to '0'.

BAT: Battery Supply—Volatile

This bit set to "1" indicates that the device is operating from supply from the V_{BAT} pin and not the V_{CC} pin. This bit can be reset either manually by the user (note this bit can only be manually cleared to 0) or automatically reset by enabling the auto-reset bit (see ARST bit).

AL: Alarm bit—Volatile

These bits announce if the alarm matches the real time clock. If there is a match, the respective bit is set to '1'. This bit can be reset either manually by the user (note this bit can only be manually cleared to 0) or automatically reset by enabling the auto-reset bit (see ARST bit).

An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

EVT: Event Detection bit —Volatile

The event detection bit provides status of the event input pin (EVIN). When the EVIN pin is triggered the EVT bit is set to 1 to indicate a detection of an event input. This bit can be reset either manually by the user (note this bit can only be manually cleared to 0) or automatically reset by enabling the auto-reset bit (see ARST bit).

When an high signal is present at the EVIN pin, an "event" is detected. On detection a corresponding bit in the status register (EVT bit) is set high and the $\overline{EVDET}$ pin, open drain, is activated (pulled low).

WRTC: Write RTC Enable Bit—Volatile

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is "0". Upon initialization or power up, the WRTC must be set to "1" to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1 Hz signal is synchronized to the STOP condition during a valid write cycle.

XTOSCB: Crystal Oscillator Enable Bit —Volatile

This bit enables / disables the internal crystal oscillator. When the XTOSCB is set to "1", the oscillator is disabled. When the XTOSCB is cleared to "0", the X1 pin allows for an external 32kHz signal to drive the RTC.

ARST: Auto Reset Enable Bit —Volatile

This bit enables / disables the automatic reset of the following status bits only: BAT, ALM, EVT. When ARST bit is set to "1", the participating status bits are reset to "0" after a valid read of the status register (STOP condition). When the ARST is cleared to "0" the user must manually reset the ARST bit.

INTERRUPT CONTROL REGISTER (INT)

Table 3. Interrupt Control Register (INT)

Addr	7	6	5	4	3	2	1	0
08h	IM	ALME	LPMODE	FOBATB	FO3	FO2	FO1	FO0
Default	0	0	0	0	0	0	0	1

FO<3:0>: Frequency Out Control Bits - Volatile

These bits enable / disable the frequency output function and selects the output frequency at the $\overline{IRQ}$ / FOUT pin. See Table 3 for frequency selection. When the frequency mode is enabled it will override the alarm mode at the $\overline{IRQ}$ / FOUT pin.

Table 4. Frequency Selection of FOUT pin

Frequency, FOUT	Units	FO3	FO2	FO1	FO0
Default	0	0	0	0	0
0	Hz	0	0	0	0
32	kHz	0	0	0	1
4096	Hz	0	0	1	0
1024	Hz	0	0	1	1
64	Hz	0	1	0	0
32	Hz	0	1	0	1
16	Hz	0	1	1	0
8	Hz	0	1	1	1
4	Hz	1	0	0	0
2	Hz	1	0	0	1
1	Hz	1	0	1	0
1/2	Hz	1	0	1	1
1/4	Hz	1	1	0	0
1/8	Hz	1	1	0	1
1/16	Hz	1	1	1	0
1/32	Hz	1	1	1	1

FOBATB: Frequency Output and Interrrupt bit - Volatile

This bit enables / disables the FOUT / $\overline{IRQ}$ pin during battery backup mode (i.e. V_{BAT} power source active). When the FOBATB is set to "1" the FOUT / $\overline{IRQ}$ pin is disabled during battery backup mode. When the FOBATB is cleared to "0" the FOUT / $\overline{IRQ}$ pin is enabled during battery backup mode.

LPMODE: Low Power Mode Bit - Volatile

This bit

ALME: Alarm Enable Bit - Volatile

This bit enables / disables the alarm function. When the ALME bit is set to "1", the alarm function is enabled. When the ALME is cleared to "0", the alarm function is disabled. The alarm function can operate in either a single event alarm or a periodic interrupt alarm (see IM bit). Note: When the frequency output mode is enabled, the alarm function is disabled.

IM: Interrupt / Alarm Mode Bit - Volatile

This bit enables / disables the interrupt mode of the alarm function. When the IM bit is set to "1", the alarm will operate in the interrupt mode, where an active low pulse width of 250ms will appear at the $\overline{IRQ}$ / FOUT pin when the RTC is triggered by the alarm as defined by alarm registers (0Ch to 11h). When the IM bit is cleared to "0", the alarm will operate in standard mode, where the $\overline{IRQ}$ / FOUT pin will be tied low until the ALM status bit is cleared to "0".

IM Bit	Interrupt / Alarm Frequency
0	Single Time Event Set By Alarm
1	Repetitive / Recurring Time Event Set By Alarm

EVENT DETECTION REGISTER (EV)

The X1209 provides a simple event and tamper detection circuit. The Event Detection Register configures the functionality of the event detection circuits.

ESMP<1:0>: Event Input Sampling Selection Bits - Volatile

These two bits select the rate of sampling of the EVIN pin to trigger an event detection. For example, a 1 Hz sampling rate would configure the X1209 to check the status of the EV pin once a second.

ESMP1	ESMP0	Event Sampling Rate
0	0	Always ON
0	1	2 Hz
1	0	1 Hz
1	1	1 / 4 Hz

EHSY<1:0>: Event Input Hysteresis Selection Bits - Volatile

These two bits select the amount of hysteresis (time based de-bouncing filter) of the EVIN pin to prevent de-bouncing or noise of external event detection circuits. The time hysteresis can be set between 0 to 31.25 ms.

For example, a 32.25ms would provide....

EHSY1	EHSY1	Input Hysteresis
0	0	0 (pullup always on)
0	1	3.9 ms
1	0	15.625 ms
1	1	32.25 ms

EVEN: Event Mode Enable Bit - Volatile

This bit enables / disables the Event Detection Mode of the X1209. When this bit is set to "1", the event mode is active. When this bit is cleared to "0", the event mode is disabled.

RTCHLT: RTC Halt on Event Detection Bit - Volatile

This bit selects whether the RTC is to continue of halt counting upon an event detection triggered by the EV pin. When RTCHLT is set to "1", the RTC will discontinue incrementing if an event is detected. Counting will resume when there is a valid write to the to the RTC registers (i.e. time set). When the RTCHLT is cleared to "0", the RTC will continue counting if an event is detected.

Note 1: This function requires that the event detection is enabled (see EVEN bit).

Note 2: In both cases, upon an event detection, the $\overline{EVDET}$ pin will be pulled low and the EV detection bit will be set to "1".

EVBATB: Event Output Battery Mode Enable Bit - Volatile

This bit enables / disables the $\overline{EVDET}$ pin during battery backup mode (i.e. V_{BAT} pin supply ON). When the EVBATB is set to "1", the $\overline{EVDET}$ pin will be disabled in battery backup mode. When the EVBATB is cleared to "0", the $\overline{EVDET}$ pin will be enabled in battery backup mode.

EVIENB: Event Current Source Enable Bit - Volatile

This bit enables / disables the internal pullup current source used for the EVIN pin. When the EVIENB bit is set to "1", the pullup current source is always disabled. When the EVIENB bit is cleared to "0", the pullup current source is enabled (current source is approximately 1 µA).

ANALOG TRIMMING REGISTER (ATR)

ATR<5:0>: Analog Trimming Register - Volatile

The X1209 contains two digitally controlled capacitors connected from both X1 pin and X2 pin to the ground pin. The amount capacitance can be selected via the ATR register.

Six analog trimming Bits from **ATR5** to **ATR0** are provided to adjust the on-chip loading capacitance range. The on-chip load capacitance ranges from 4.5 pF to 20.25 pF. Each bit has a different weight for capacitance adjustment. In addition, using a Citizen CFS-206 crystal with different ATR bit combinations provides an estimated ppm range from +125 ppm to –34 ppm to the nominal frequency compensation. The combination of digital and analog trimming can give up to +185 to –94 ppm adjustment.

The on-chip capacitance can be calculated as follows:

C_{ATR} = [(ATR value, decimal) x 0.5pF] + 9.0pF

Note that the ATR values are in two's complement, for example, ATR(000000) = 25pF, ATR(100000) = 9pF, and ATR(011111) = 40.5pF. The entire range runs from 4.5pF to 20.25pF in 0.5pF steps.

The effective load capacitance is the parallel combination of the two capacitances at each pin. The values calculated above are typical, and total load capacitance seen by the crystal will include approximately 2pF of package and board capacitance in addition to the ATR value.

BMATR<1:0>: Battery Mode ATR Selection - Volatile

Since accuracy of the crystal oscillator is dependent on the Vcc/Vbat operation, the X1209 provides the capability to adjust the capacitance when the devices switches between power sources.

BMATR1	BMATR0	Delta Capacitance (Cbat to Cvcc)
0	0	0 pF
0	1	- 0.5 pF (~ + 2ppm)
1	0	+ 0.5 pF (~ -2ppm)
1	1	+ 1 pF (~ -4ppm)

DIGITAL TRIMMING REGISTER (DTR)

DTR<2:0>: Digital Trimming Register - Volatile

The digital trimming Bits **DTR2**, **DTR1** and **DTR0** adjust the number of counts per second and average the ppm error to achieve better accuracy.

DTR2 is a sign bit. DTR2=0 means frequency compensation is > 0. DTR2=1 means frequency compensation is < 0.

DTR1 and DTR0 are scale bits. DTR1 gives _____ ppm adjustment and DTR0 gives _____ ppm adjustment.

A range from -60 ppm to +60 ppm can be represented by using three bits above.

Table 5. Digital Trimming Registers

DTR Register			Estimated frequency PPM
DTR2	DTR1	DTR0	
0	0	0	0 (default)
0	0	1	+20
0	1	0	+40
0	1	1	+60
1	0	0	0
1	1	1	-20
1	1	0	-40
1	1	1	-60

ALARM REGISTER

Addresses [0C hex to 11hex]

The alarm register contents mimic the contents of the RTC register, but add enable bits and exclude the 24 hour time selection bit. The enable bits specify which registers to use in the comparison between the Alarm and Real Time Registers. For example:

– Setting the Enable Month Bit (EMNA) bit in combination with other enable bits and a specific alarm time, the user can establish an alarm that triggers at the same time once a year.

When there is a match, an alarm flag (ALM) is set. The occurrence of an alarm can be determined by polling the ALM bit or by enabling the $\overline{IRQ}$ output, using it as hardware flag.

The alarm enable bits are located in the MSB of the particular register. When all enable bits are set to '0', there are no alarms.

– The user can set the X1209 to alarm every Wednesday at 8:00 AM by setting the EDWA, the EHRA and EMNA enable bits to '1' and setting the DWA, HRA and MNA Alarm registers to 8:00AM Wednesday.

– A daily alarm for 9:30PM results when the EHRA and EMNA enable bits are set to '1' and the HRA and MNA registers are set to 9:30PM.

USER REGISTER (USER)

Addresses [12 hex to 13 hex]

These registers are available for (2 bytes) user memory storage.

SERIAL COMMUNICATION

Interface Conventions

The device supports a bidirectional bus oriented proto-col. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 3.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 4.

Stop Condition

All communications must be terminated by a stop con-dition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Fig-ure 4.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 5.

The device will respond with an acknowledge after rec-ognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for:

– The Slave Address Byte when the Device Identifier and/or Select bits are incorrect

– All Data Bytes of a write when the WRTC in the Write Protect Register is LOW

– The 2nd Data Byte of a Status Register Write Operation (only 1 data byte is allowed)

Figure 3. Valid Data Changes on the SDA Bus
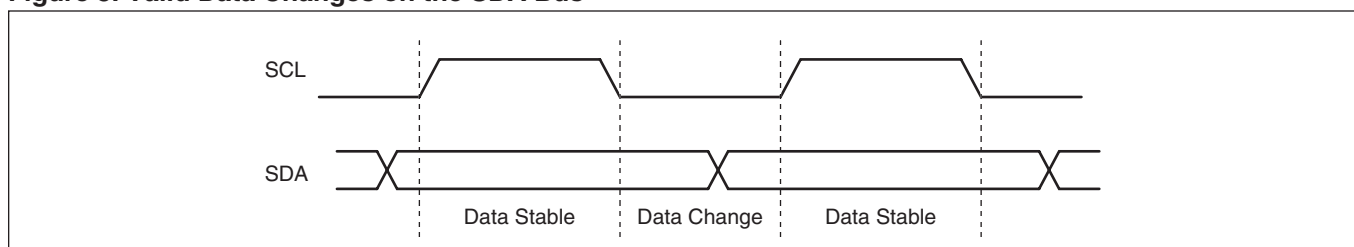
Figure 4. Valid Start and Stop Conditions
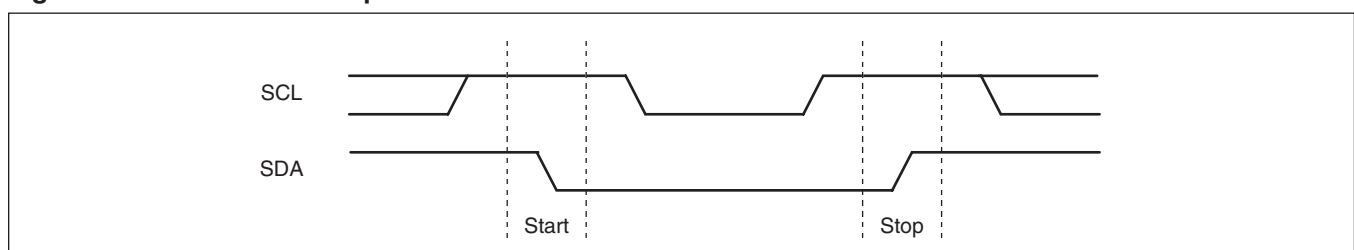
Figure 5. Acknowledge Response From Receiver
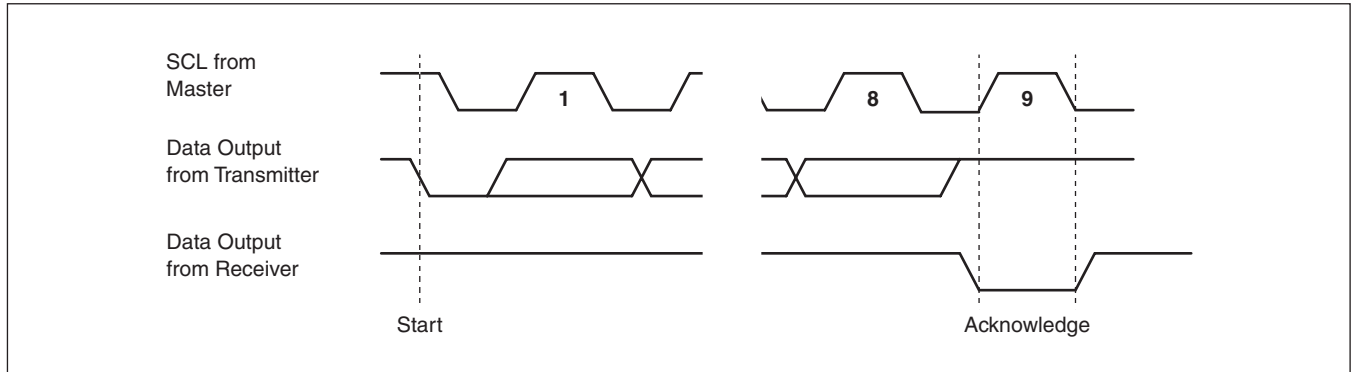
DEVICE ADDRESSING

Following a start condition, the master must output a Slave Address Byte. Slave bits '1101' access the CCR.

Bit 3 through Bit 1 of the slave byte specify the device select bits. These are set to '111'.

The last bit of the Slave Address Byte defines the operation to be performed. When this R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 6.

After loading the entire Slave Address Byte from the SDA bus, the X1209 compares the device identifier and device select bits with '1101111'. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a two byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power up the internal address counter is set to address 0H, so a current address read of the CCR array starts at address 0. When required, as part of a random read, the master must supply the 2 Word Address Bytes as shown in Figure 6.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the Clock/Control Registers, the slave byte must be 1101111x in both places.

Figure 6. Slave Address, Word Address, and Data Bytes
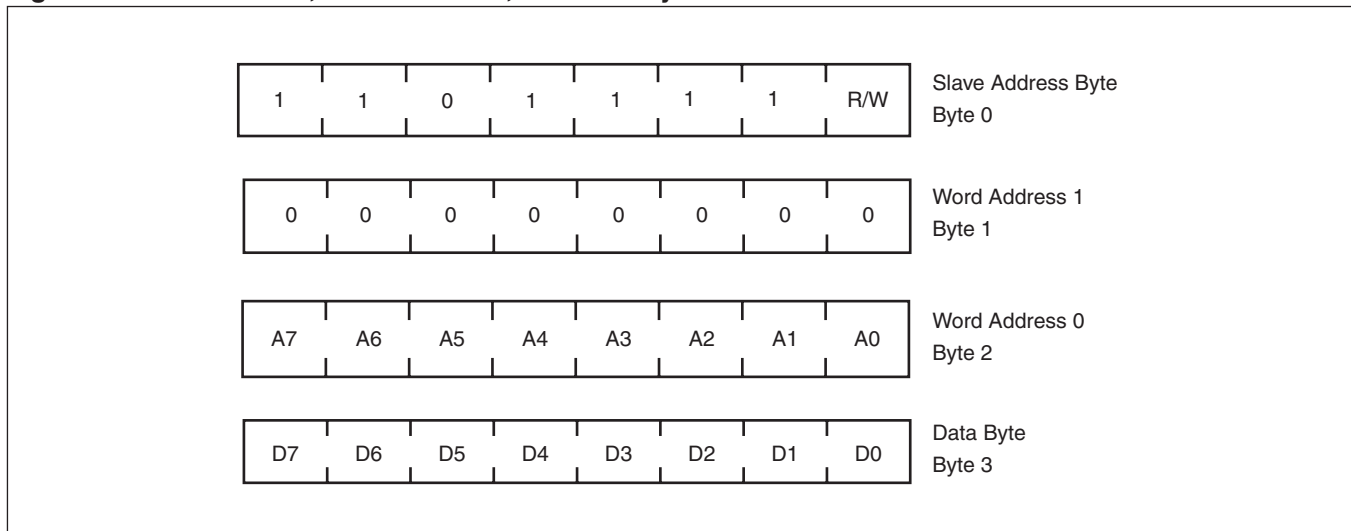
WRITING OR READING TO THE CLOCK/CONTROL REGISTERS

Changing any of the volatile bits of the clock/control register requires the following steps:

– Write one to 8 bytes to the Clock/Control Registers with the desired clock, alarm, or control data. This sequence starts with a start bit, requires a slave byte of "11011110" and an address within the CCR and is terminated by a stop bit. A write to the CCR changes volatile register values.

– A read operation occurring between any of the previous operations will not interrupt the register write operation.

– The WRTC bit enables or disables write capability into the RTC Timing Registers. Upon initialization or power up, the WRTC must be set to "1" to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting.

– Writing and Reading capability is disable during battery backup mode.

Write Operations

Byte Write

For a write operation, the device requires the Slave Address Byte and the Word Address Bytes. This gives the master access to any one of the words in the CCR. Upon receipt of each address byte, the X1209 responds with an acknowledge. After receiving both address bytes the X1209 awaits the eight bits of data. After receiving the 8 data bits, the X1209 again responds with an acknowledge. The master then terminates the transfer by generating a stop condition. The X1209 then begins an internal write cycle of the data to the nonvolatile memory. During the internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 7.

Stop and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and it's associated ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the X1209 resets itself without performing the write. The contents of the array are not affected.

Acknowledge Polling

Once the stop condition is issued to indicate the end of the master's byte load operation, the X1209 initiates the internal nonvolatile write cycle. Acknowledge polling can begin immediately. To do this, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the X1209 is still busy with the nonvolatile write cycle then no ACK will be returned. When the X1209 has completed the write operation, an ACK is returned and the host can proceed with the read or write operation. Refer to the flow chart in Figure 9.

Reading the Real Time Clock

The RTC is read by initiating a Read command and specifying the address corresponding to the register of the Real Time Clock. The RTC Registers can then be read in a Sequential Read Mode. Since the clock runs continuously and a read takes a finite amount of time, there is the possibility that the clock could change during the course of a read operation. In this device, the time is latched by the read command (falling edge of the clock on the ACK bit prior to RTC data output) into a separate latch to avoid time changes during the read operation. The clock continues to run. Alarms occurring during a read are unaffected by the read operation.

Writing to the Real Time Clock

The time and date may be set by writing to the RTC registers. To avoid changing the current time by an uncompleted write operation, the current time value is loaded into a separate buffer at the falling edge of the clock on the ACK bit before the RTC data input bytes, the clock continues to run. The new serial input data replaces the values in the buffer. This new RTC value is loaded back into the RTC Register by a stop bit at the end of a valid write sequence. An invalid write operation aborts the time update procedure and the contents of the buffer are discarded. After a valid write operation the RTC will reflect the newly loaded data beginning with the next "one second clock cycle" after the stop bit is written. The RTC continues to update the time while an RTC register write is in progress and the RTC continues to run during any nonvolatile write sequences. A single byte may be written to the RTC without affecting the other bytes

Figure 7. Byte Write Sequence
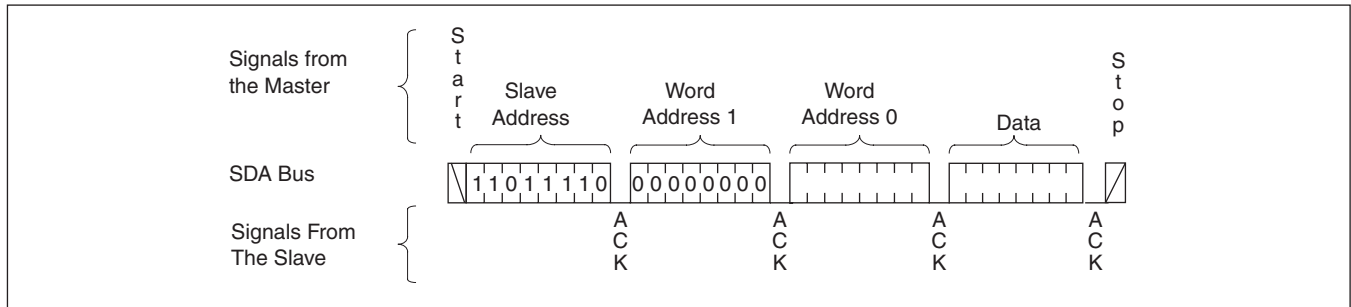
Read Operations

There are three basic read operations: Current Address Read, Random Read, and Sequential Read.

Current Address Read

Internally the X1209 contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. Upon receipt of the Slave Address Byte with the R/$\overline{\text{W}}$ bit set to one, the X1209 issues an acknowledge, then transmits eight data bits. The master terminates the read operation by not responding with an acknowledge during the ninth clock and issuing a stop condition. Refer to Figure 8 for the address, acknowledge, and data transfer sequence.

Figure 8. Current Address Read Sequence
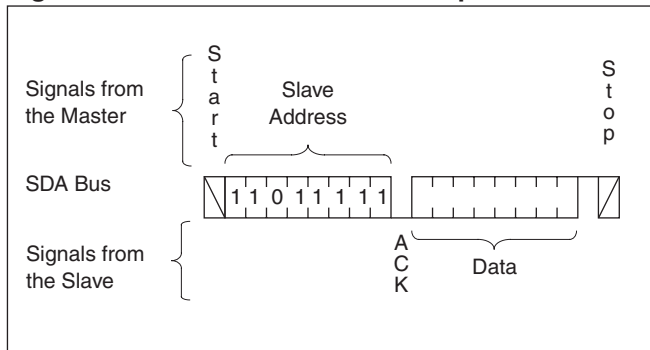
Figure 9. Acknowledge Polling Sequence
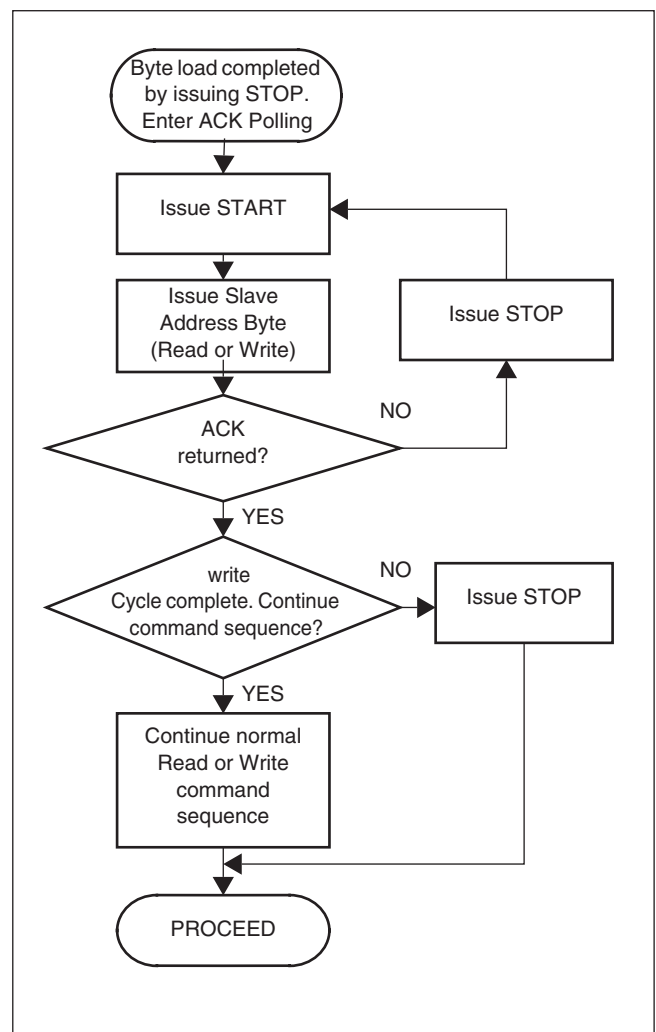
It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Random Read

Random read operations allow the master to access any location in the X1209. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to zero, the master must first perform a "dummy" write operation.

The master issues the start condition and the slave address byte, receives an acknowledge, then issues the word address bytes. After acknowledging receipt of each word address byte, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 10 for the address, acknowledge, and data transfer sequence.

In a similar operation called "Set Current Address," the device sets the address if a stop is issued instead of the second start shown in Figure 10. The X1209 then goes into standby mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next Current Address Read operation will read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first data byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. Refer to Figure 11 for the acknowledge and data transfer sequence.

Figure 10. Random Address Read Sequence
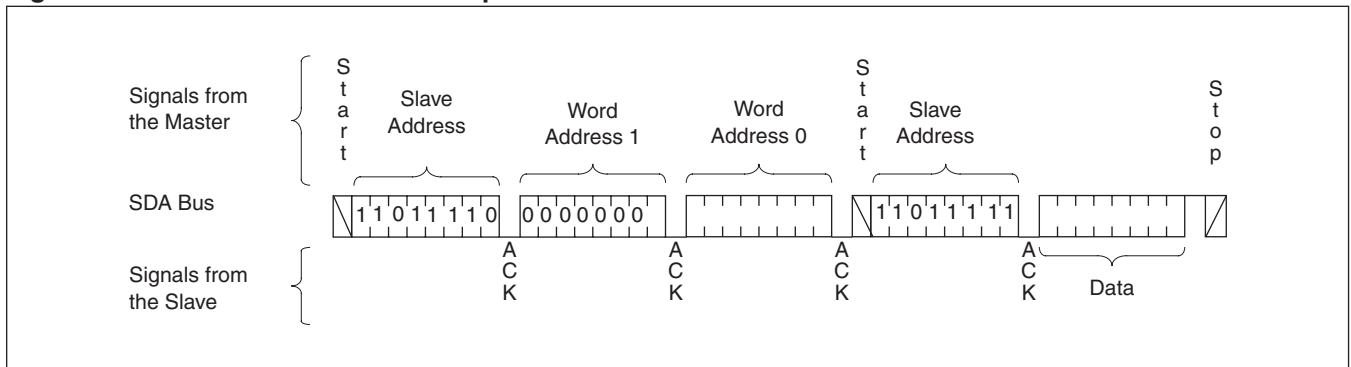
Figure 11. Sequential Read Sequence
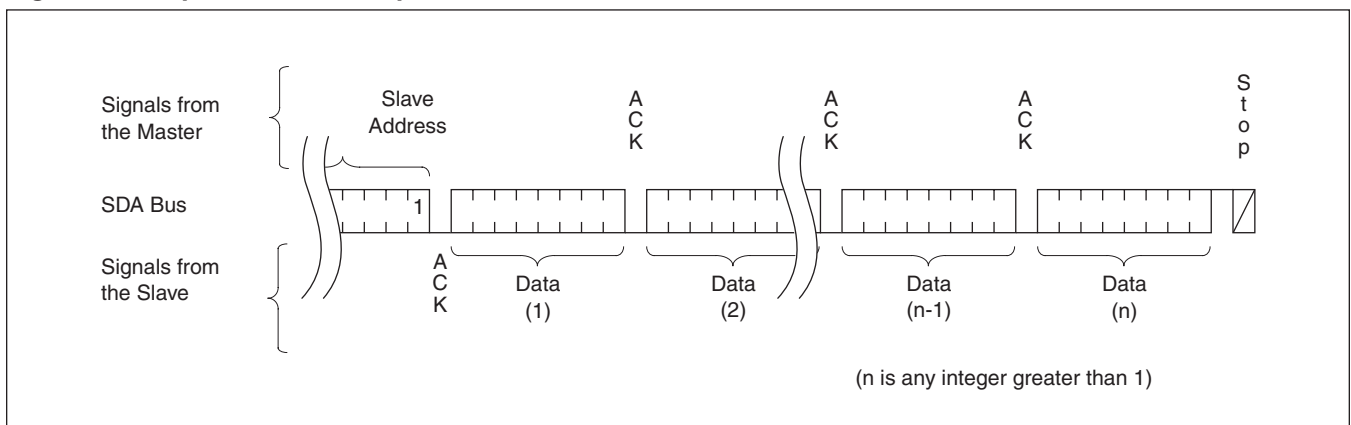
APPLICATION SECTION

CRYSTAL OSCILLATOR AND TEMPERATURE COMPENSATION

Xicor has now integrated the oscillator compensation circuit

Layout Considerations

The crystal

Assembly

Most electronic

Oscillator Measurements

When a proper crystal i

Backup Battery Operation

Many types of batteries can be used with the Xicor RTC products. 3.0V or 3.6V Lithium batteries are appropriate, and sizes are available that can power a Xicor RTC device for up to 10 years. Another option is to use a supercapacitor for applications where Vcc may disappear intermittently for short periods of time.

Depending on the value of supercapacitor used, backup time can last from a few days to two weeks (with >1F). A simple silicon or Schottky barrier diode can be used in series with Vcc to charge the supercapacitor, which is connected to the VBAT pin. Do not use the diode to charge a battery (especially lithium batteries!).

Figure 12. Supercapactor charging circuit
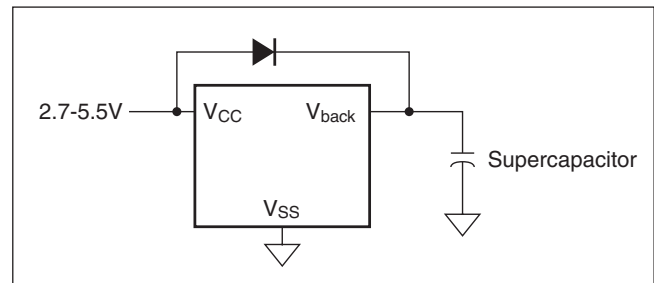
Since the battery switchover occurs at .... (see Figure xx), ...

The summary of conditions for backup battery operation is given in Table 6:

Table 6. Battery Backup Operation

1. Example Application, Vcc=5V, VBAT=3.0V

Condition	Vcc	VBAT	Vtrip	Iback	Notes
a. Normal Operation					
b. Vcc on with no battery					
c. Backup Mode					

2. Example Application, Vcc=3.3V,VBAT=3.0V

Condition	Vcc	VBAT	Vtrip	Iback	
a. Normal Operation					
b. Vcc on with no battery					
c. Backup Mode					
d.					

3. Example Application, Vcc=3.3V,VBAT=5.0V

a. Normal Operation					
b. Vcc on with no battery					
c. Backup Mode					

PACKAGING INFORMATION

10-Lead Miniature Small Outline Gull Wing Package Type M

10 BUMP FCP PACKAGE

	Symbol	Min	Nominal	Max
			Millimeters	
Package Width	A			
Package Length	B			
Package Height	C			
Body Thickness	D			
Ball Height	E			
Ball Diameter	F			

	Bump Name	X coordinate, μm	Y coordinate, μm
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			