N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV$_{DSS}$ / BV$_{DGS}$	R$_{DS(ON)}$ (max)	I$_{D(ON)}$ (min)	Order Number / Package
			TO-92
60V	7.5Ω	0.75A	VN2222LL

Features

❏ Free from secondary breakdown

❏ Low power drive requirement

❏ Ease of paralleling

❏ Low C$_{ISS}$ and fast switching speeds

❏ Excellent thermal stability

❏ Integral Source-Drain diode

❏ High input impedance and high gain

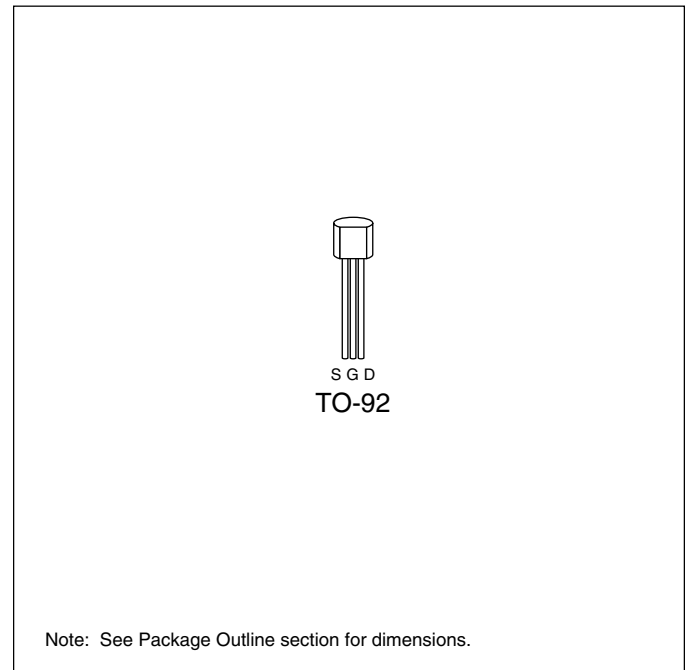❏ Complementary N- and P-channel devices

Applications

❏ Motor controls

❏ Converters

❏ Amplifiers

❏ Switches

❏ Power supply circuits

❏ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV$_{DSS}$
Drain-to-Gate Voltage	BV$_{DGS}$
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option

S G D

TO-92

Note: See Package Outline section for dimensions.

Thermal Characteristics

Package	I$_D$ (continuous)*	I$_D$ (pulsed)	Power Dissipation @ T$_C$ = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I$_{DR}$*	I$_{DRM}$
TO-92	0.23A	1.0A	1W	125	170	0.23A	1.0A

* I$_D$ (continuous) is limited by max rated T$_j$.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV$_{DSS}$	Drain-to-Source Breakdown Voltage	60			V	V$_{GS}$ = 0V, I$_D$= 100μA
V$_{GS(th)}$	Gate Threshold Voltage	0.6		2.5	V	V$_{GS}$ = V$_{DS}$, I$_D$ = 1mA
I$_{GSS}$	Gate Body Leakage			100	nA	V$_{GS}$ = ±20V, V$_{DS}$ = 0V
I$_{DSS}$	Zero Gate Voltage Drain Current			10		V$_{GS}$ = 0V, V$_{DS}$ = Max Rating
				500	μA	V$_{GS}$ = 0V, V$_{DS}$ = 48V T$_A$ = 125°C
I$_{D(ON)}$	ON-State Drain Current	0.75			A	V$_{GS}$ = 10V, V$_{DS}$ = 10V
R$_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			7.5	Ω	V$_{GS}$ = 5V, I$_D$ = 0.2A
				7.5	Ω	V$_{GS}$ = 10V, I$_D$ = 0.5A
G$_{FS}$	Forward Transconductance	100			m℧	V$_{DS}$ = 10V, I$_D$ = 0.5A
C$_{ISS}$	Input Capacitance			60		V$_{GS}$ = 0V, V$_{DS}$ = 25V f = 1 MHz
C$_{OSS}$	Common Source Output Capacitance			25	pF	
C$_{RSS}$	Reverse Transfer Capacitance			8		
t$_{(ON)}$	Turn-ON Time			10	ns	V$_{DD}$ = 15V, I$_D$ = 0.6A R$_{GEN}$ = 25Ω
t$_{(OFF)}$	Turn-OFF Time			10		
V$_{SD}$	Diode Forward Voltage Drop		0.85		V	V$_{GS}$ = 0V, I$_{SD}$ = 0.2A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

11/12/01

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