Advance Data Sheet

AT&T Microelectronics

ATT7C340 High-Speed CMOS 1 Mbit (128K x 8) SRAM Synchronous, Pipelined Architecture TTL Compatible Common I/O

Features

- 128K by 8-bit synchronous registered SRAM with common I/O
- Internal self-timed write pulse generation
- Fast clock access times: 10 ns max
- Fast read/write cycle times: 20 ns min (50 MHz)
- Fully pipelined architecture
- Ideally suited as high-speed cache memory for RISC applications
- Registered addresses, data I/O, $\overline{WE}$, $\overline{CE}$, and $\overline{OE}$
- TTL compatible common I/O
- Data retention at 2 V for battery backup operations
- Low-power operation
- Advanced 0.5 µm CMOS technology
- Surface-mount, 32-pin, plastic SOJ (J-lead) package

Description

The ATT7C340 device is high-performance, CMOS static RAM organized as 131,072 words by 8 bits. The data-in and data-out signals share I/O pins. The device has single chip enable and an output enable. The output is 3-stated when either chip enable or output enable is high.

The address (A0—A16), data in (I/O0—I/O7), write enable ($\overline{WE}$), chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) are latched, positive edge-triggered registers.

Output registers provide full pipelined operation. At the rising edge of the clock, the output from previous cycle is presented.

Inputs and outputs are TTL compatible. Operation is from a single 5 V power supply. Power consumption is 625 mW (typical) at 20 ns cycle time. Dissipation drops to 500 µW (typical) when the memory is in standby mode.

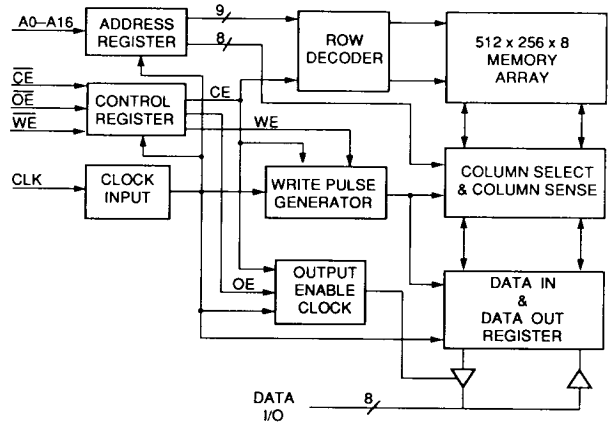

Figure 1. Block Diagram

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Pin Information

Table 1. Pin Descriptions

Pin	Function
A0—A16	Address Inputs
I/O0—I/O7	Data Input/Output
CLK	Clock Input
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
GND	Ground
Vcc	+5 V Supply
NC	No Connection

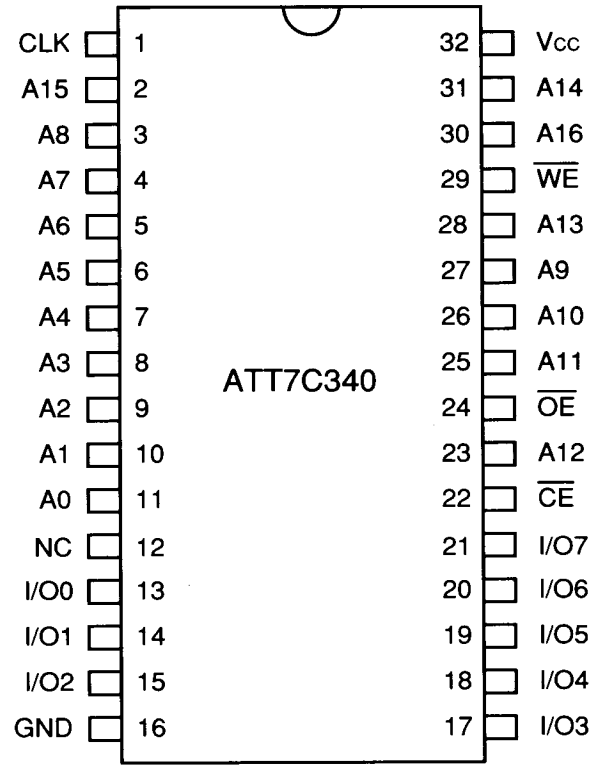


Figure 2. Pin Diagram

Absolute Maximum Ratings

Stresses exceeding the values listed under Absolute Maximum Ratings can cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
Operating Ambient Temperature	T_A	–55	125	°C
Supply Voltage with Respect to Ground	Vcc	–0.5	7.0	V
Input Signal with Respect to Ground	—	–3.0	7.0	V
Signal Applied to High-impedance Output	—	–3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latchup Current	—	> 200	—	mA

Handling Precautions

The ATT7C340 device includes internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress values.

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation	0 °C to 70 °C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention	0 °C to 70 °C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over all Recommended Operating Conditions

Table 2. General Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA , V_{CC} = 4.5 V	—	—	0.4	V
Input Voltage:						
High	V_{IH}	—	2.0	—	V_{CC} + 0.3	V
Low	V_{IL}	—	–1.0	—	0.8	V
Input Current	I_{IX}	Ground ≤ V_{IN} ≤ V_{CC}	–10	—	10	µA
Output Leakage Current	I_{OZ}	$\overline{CE}$ is high	–10	—	10	µA
V_{CC} Current:						
Active	I_{CC1}	See note 1	—	125	200	mA
Inactive	I_{CC2}	See note 2	—	25	50	mA
Standby	I_{CC3}	See note 3	—	100	500	µA
Capacitance:						
Input	C_I	—	—	—	5	pF
Output	C_O	—	—	—	7	pF

Notes:

1. Tested with outputs open, all address and data inputs at TTL level, and the clock running at maximum cycle rate. The device is continously enabled for writing, i.e., $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ ≤ V_{IL}.
2. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or ground. Clock is continuously running at maximum cycle rate.
3. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. For all other inputs must be at either V_{CC} or ground level to ensure full powerdown. Clock must be running at least two cycles and stop at either V_{CC} or ground level.

Timing Characteristics

Table 3. Read Cycle

Over all Recommended Operating Conditions. Test conditions assume input transition times of < 2.4 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3 V (see Figure 9), and output loading for specified IOL and IOH + 30 pF (see Figure 8A).

Symbol	Parameter	Min	Max	Unit
tKHKH	Read Cycle Time	20	—	ns
tKHQV	Clock Access Time	—	10	ns
tKHQX	Output Active from Clock High	1.5	—	ns
tKHQZ	Clock High to Q High Z ($\overline{OE}$ = VIH) [See Figure 8B.]	—	6	ns
tKLKH	Clock Low Pulse Width	7	—	ns
tKHKL	Clock High Pulse Width	7	—	ns
tAVKH	Setup Time for AD	3	—	ns
tEVKH	Setup Time for $\overline{CE}$	3	—	ns
tOVKH	Setup Time for $\overline{OE}$	3	—	ns
tWVKH	Setup Time for $\overline{WE}$	3	—	ns
tKHAX	Hold Time for AD	3	—	ns
tKHEX	Hold Time for $\overline{CE}$	1	—	ns
tKHOX	Hold Time for $\overline{OE}$	1	—	ns
tKHWX	Hold Time for $\overline{WE}$	1	—	ns

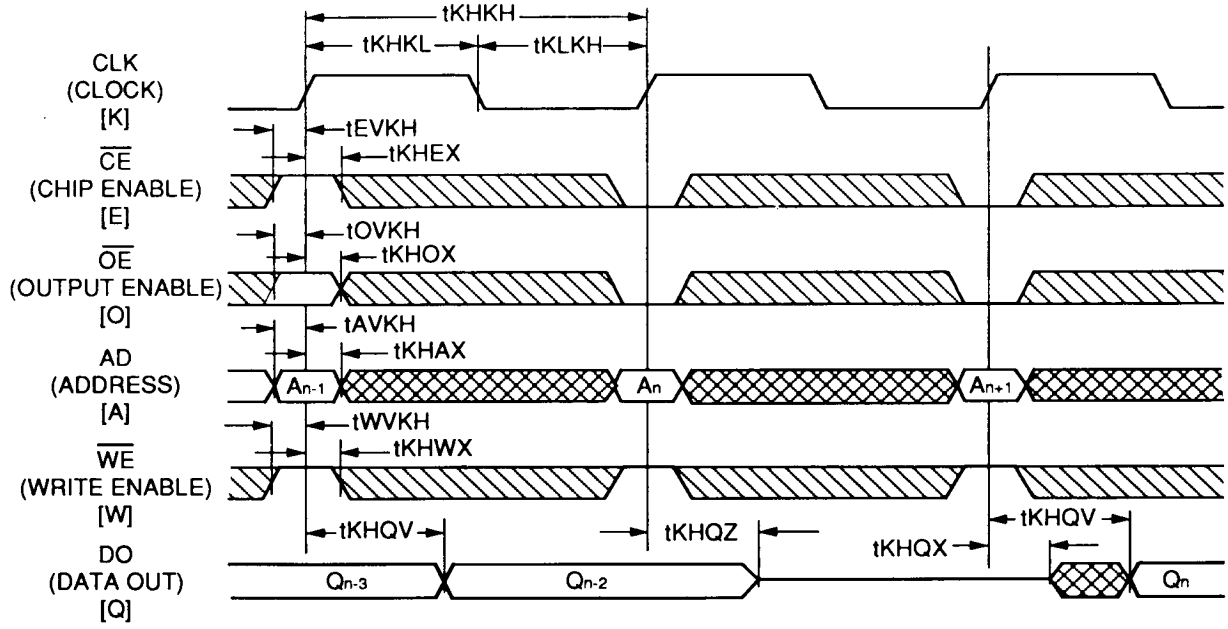
Table 4. Write Cycle

Over all Recommended Operating Conditions. Test conditions assume input transition times of < 2.4 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3 V (see Figure 9), and output loading for specified IOL and IOH + 30 pF (see Figure 8A).

Symbol	Parameter	Min	Max	Unit
tKHKH	Write Cycle Time	20	—	ns
tKHQZ	Clock High to Q High Z ($\overline{OE}$ = VIH) [See Figure 8B.]	—	6	ns
tKLKH	Clock Low Pulse Width	7	—	ns
tKHKL	Clock High Pulse Width	7	—	ns
tAVKH	Setup Time for AD	3	—	ns
tEVKH	Setup Time for $\overline{CE}$	3	—	ns
tOVKH	Setup Time for $\overline{OE}$	3	—	ns
tWVKH	Setup Time for $\overline{WE}$	3	—	ns
tKHAX	Hold Times for AD	1	—	ns
tKHEX	Hold Time for $\overline{CE}$	1	—	ns
tKHOX	Hold Time for $\overline{OE}$	1	—	ns
tKHWX	Hold Time for $\overline{WE}$	1	—	ns

Timing Characteristics (continued)

Timing Diagrams



Notes:
When the $\overline{CE}$ is high, regardless of the $\overline{OE}$ level, the outputs 3-state.
The outputs Qn-3 and Qn-2 are from two previous cycles where $\overline{WE}$ is high, and $\overline{CE}$ and $\overline{OE}$ are low.

Figure 3. Read Cycle 1

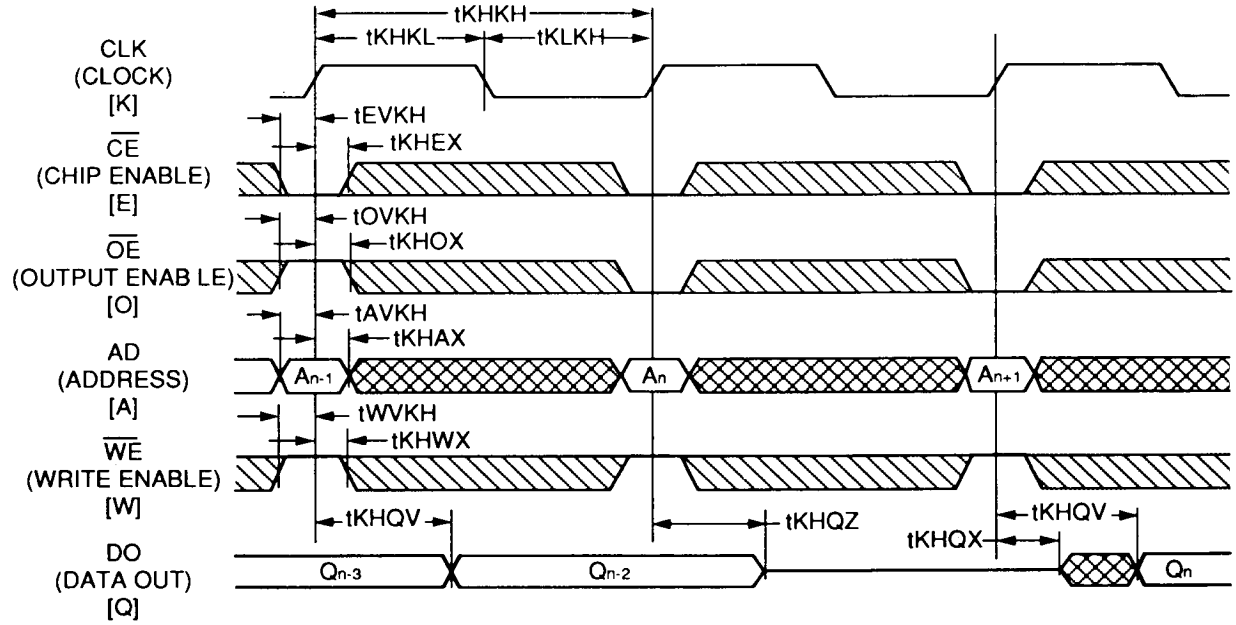


Figure 4. Read Cycle 2

Timing Characteristics (continued)

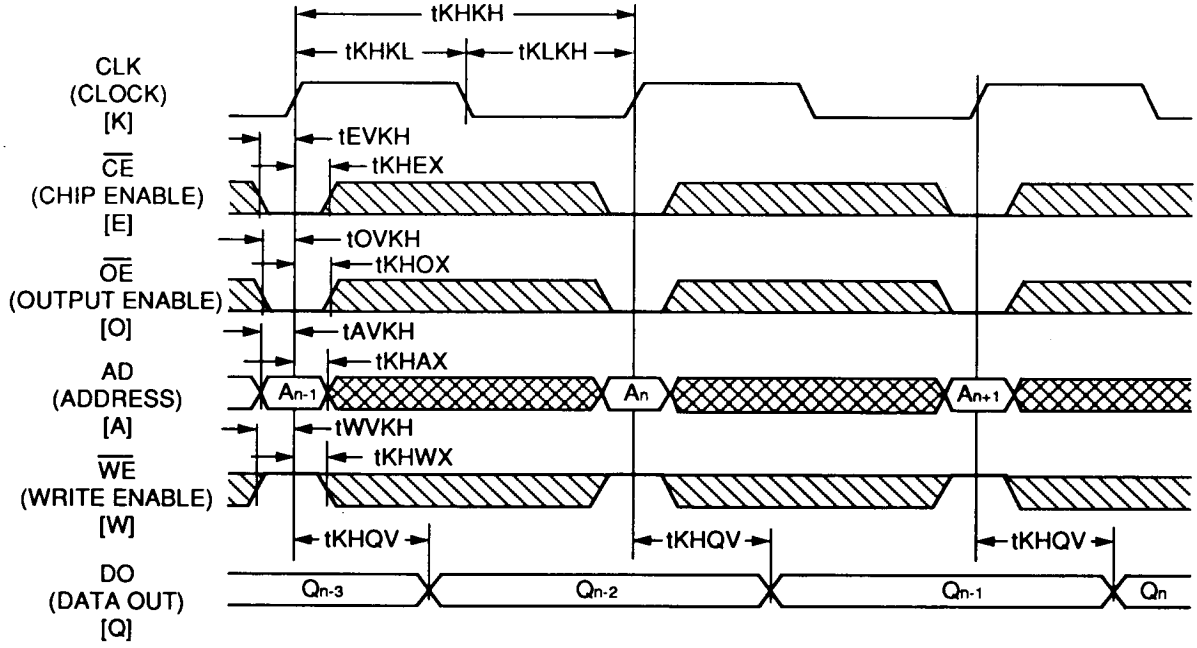
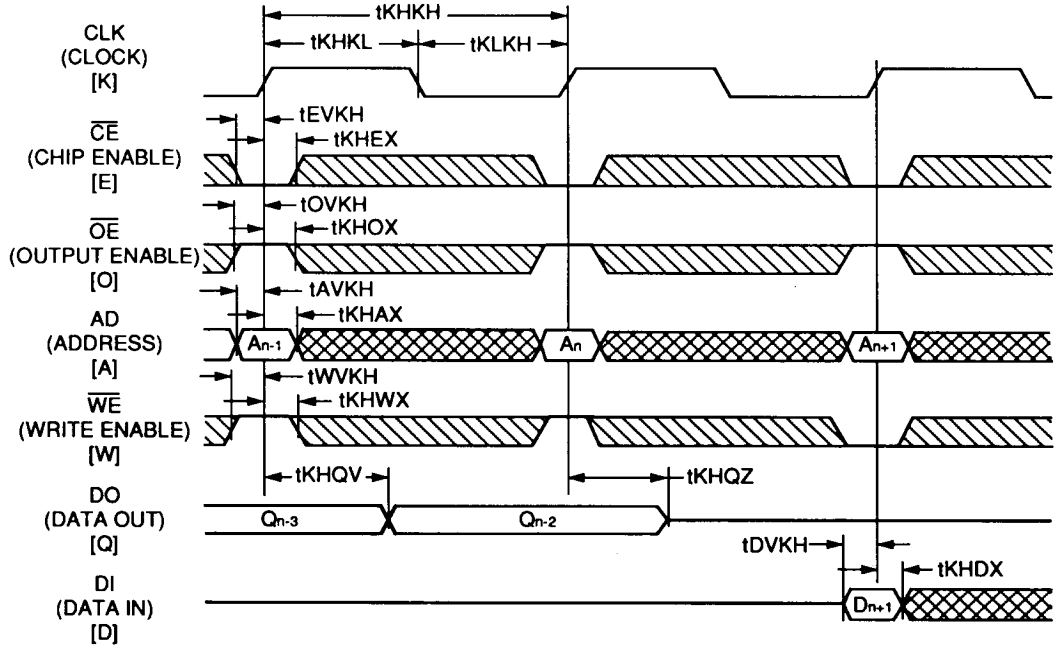


Figure 5. Read Cycle 3



Notes:
Since the device has common I/O, the data out must be 3-stated before the data in can be applied. It is recommended that the data in is applied in the next cycle. $\overline{OE}$ must be latched in high in the previous cycle.
The outputs Qn-3 and Qn-2 are from two previous cycles where $\overline{WE}$ is high, $\overline{CE}$ and $\overline{OE}$ are low.

Figure 6. Write Cycle

Timing Characteristics (continued)

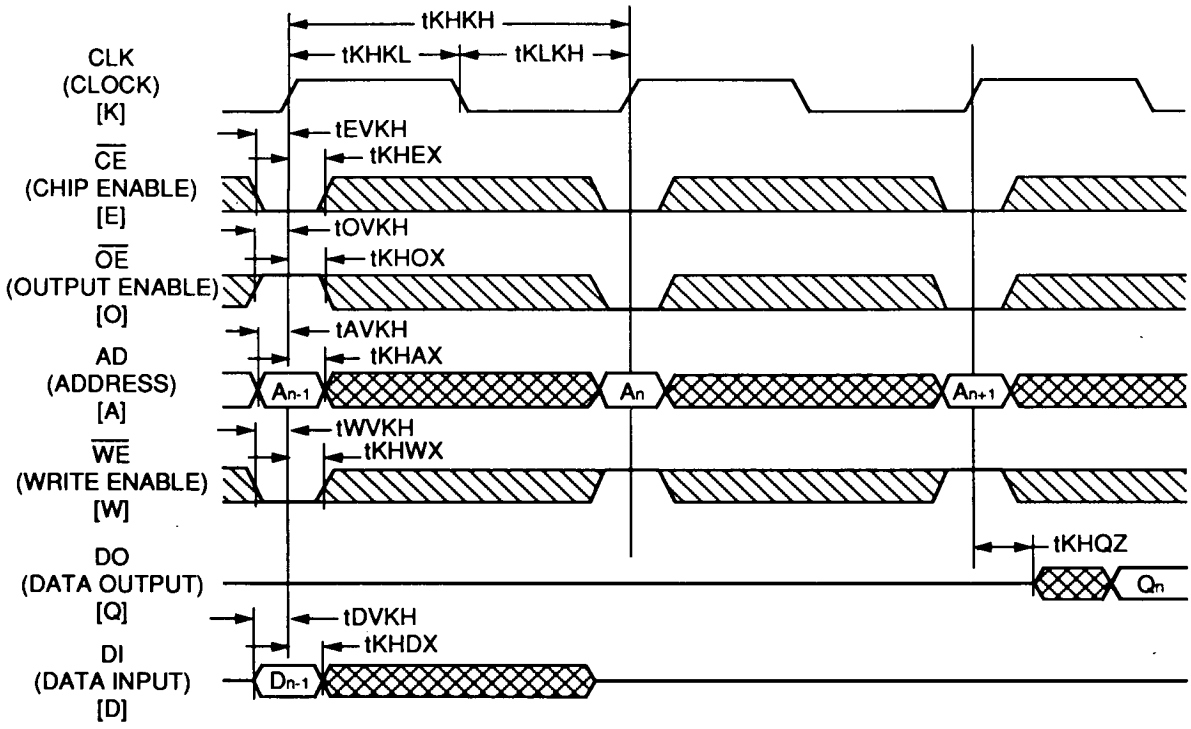


Figure 7. Write/Read Cycle

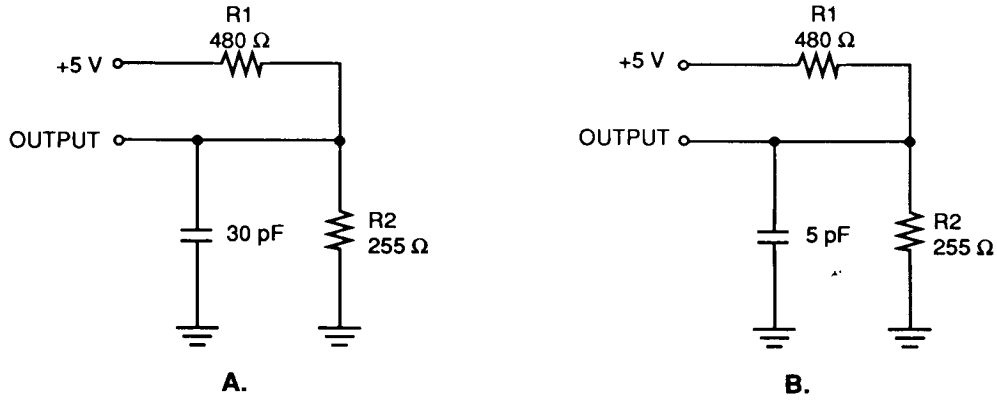


Figure 8. Test Loads

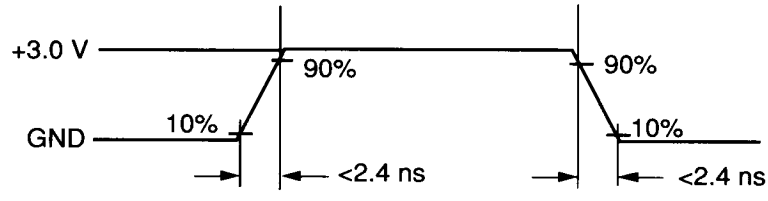
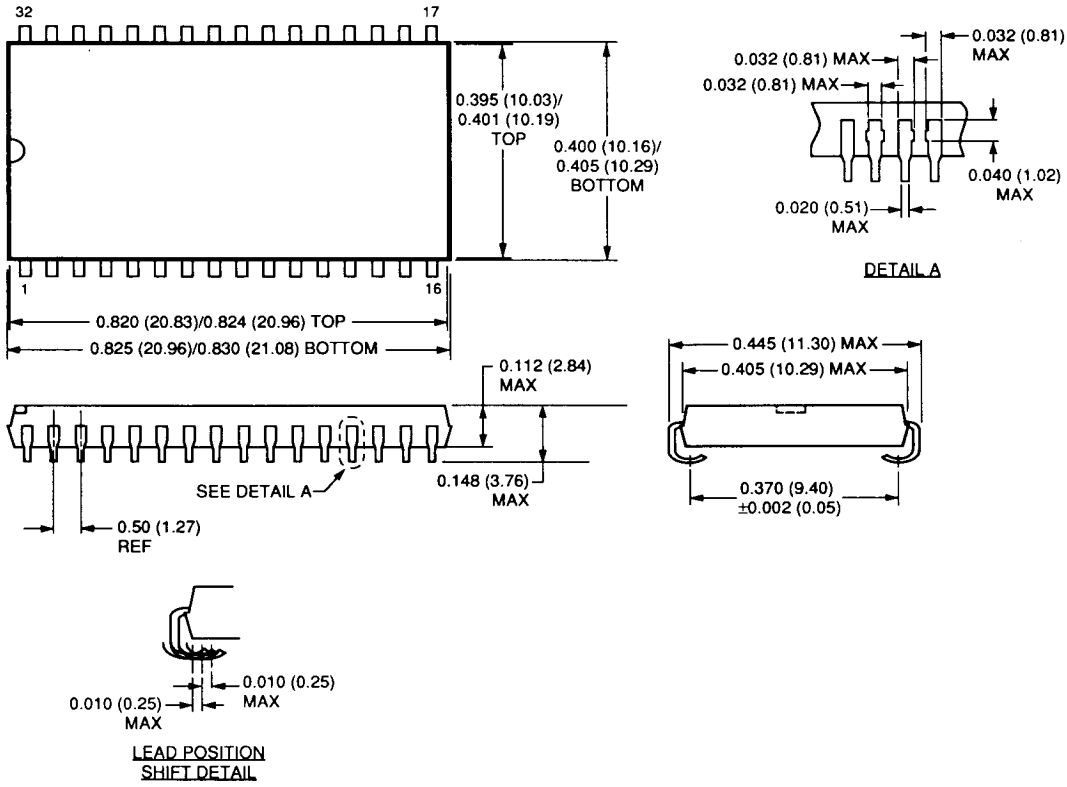


Figure 9. Transition Times

Outline Diagram

32-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).



Ordering Information

Device Code	Package	Temperature
ATT7C340	32-Pin, Plastic SOJ	0 °C to 70 °C

For additional information, contact your AT&T Account Manager or the following:
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