21145 Phoneline/Ethernet LAN Controller

Preliminary Datasheet

Product Features

HomePNA Features

- Compliant with the *Home Phoneline Networking Alliance* (HomePNA*) Specification effort.
- Integrates a HomePNA PHY for 1 Mb/s Ethernet-like home networking on telephone lines.
- Provides automatic support for dual HomePNA data transfer rates and dual transmission power levels.
- Supports autodetection between 10BASE-T, HomePNA and MII/SYM ports.
- Generates an interrupt upon HomePNA PHY interrupt.
- Provides a software interface to the HomePNA PHY internal registers.

Power Management and Power Saving Features

- Fully compliant with the *Network Device Class Power Management Specification*, Revision 1.0, and the *Communication Device Class Power Management Specification*, under the OnNow Architecture for Microsoft's *PC97 Design Guide, PC 98 Hardware Design Guide, and PC 99 Hardware Design Guide*.
- Supports all wake-up events defined in the *Network Device Class Power Management Specification*, Revision 1.0 and the *Communication Device Class Power management Specification.*
- Fully compliant with the *Advanced Configuration and Power Interface* (ACPI) *Specification*, Revision 1.0
- Fully compliant with the *PCI Bus Power Management Interface Specification*, Revision 1.0.

PCI and CardBus Features

- Supports PCI and CardBus interfaces for network and modem access.
- Supports CardBus cstschg pin and Status Changed registers.
- Supports storage of CardBus card information structure (CIS) in the serial ROM or the expansion ROM.

Host Interface Features

- Includes a powerful onchip direct memory access (DMA) with programmable burst size, providing low CPU utilization.
- Supports interrupt mitigation on transmit and receive.
- Contains large independent receive and transmit FIFOs.

Network Side Features

- Supports three network ports: 10BASE-T (10 Mb/s), HomePNA (1 Mb/s), and MII/SYM (10/100 Mb/s).
- Supports autodetection between 10BASE-T, HomePNA, and MII/SYM ports.
- Supports full-duplex operation on both MII/SYM and 10BASE-T ports.
- Provides internal and external loopback capability on all network ports.
- Supports IEEE 802.3 and ANSI 8802-3 Ethernet standards.

Other Features

- Provides MicroWire* interface for serial ROM (1 K and 4 K EEPROM).
- Incorporates a modem interface that connects to a wide range of modem chipsets available in the marketplace.

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1.0 Introduction

This manual contains detailed electrical and mechanical specifications for the 21145 Phoneline/ Ethernet LAN Controller.

1.1 Manual Organization

This manual contains the following.

- Section 1.0, “Introduction”, provides a general description of the 21145 and an overview of the hardware components.
- Section 2.0 “Pinout and Signal Descriptions”, provides the physical layout of the 21145 and describes each of the input and output signals.
- Section 3.0 “Electrical and Environmental Specifications”, describes the 21145’s electrical and environmental specifications.
- Section 4.0 “Mechanical Specifications”, includes the 21145 144-pin and 176-pin package marking and mechanical specifications.

1.2 General Description

The 21145 is an Ethernet/HomePNA LAN controller for both 100 Mb/s and 10 Mb/s data rates, that integrates a HomePNA PHY for 1 Mb/s data rate home networking on telephone lines. The 21145 provides a direct interface to the Peripheral Component Interconnect (PCI) local bus or to the CardBus. The 21145 interfaces to the host processor by using onchip command and status registers (CSRs) and a shared host memory area, set up mainly during initialization. This minimizes processor involvement in the 21145 operation during normal reception and transmission.

The 21145 also incorporates a modem interface, and can operate with a wide range of modem chipsets available in the marketplace.

The 21145 is optimized for low power PCI/CardBus based systems and supports a power-management mechanism based upon the OnNow architecture for Microsoft’s *PC 97 Hardware Design Guide, PC 98 Hardware Design Guide, and PC 99 Hardware Design Guide*.

Large FIFOs allow the 21145 to efficiently operate in systems with longer latency periods. Bus traffic is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without a repeated fetch from the host memory. The 21145 provides an upgradable expansion ROM interface.

The 21145 provides these network interfaces:

- 10BASE-T 10 Mb/s port
- HomePNA port
- A media-independent/symbol interface (MII/SYM) 10/100 Mb/s port

The 10BASE-T port provides a direct Ethernet connection to the twisted-pair (TP) interface. The HomePNA port provides a direct interface to a telephone line at a rate of 1 Mb/s.

The MII/SYM port supports two operational modes:

- MII mode—A full implementation of the MII standard
- SYM mode—Symbol interface to an external 100 Mb/s front-end decoder (ENDEC). In this mode the 21145 uses an onchip physical coding sublayer (PCS) and a scrambler/descrambler circuit to enable a low-cost 100BASE-T implementation.

The 21145 is capable of functioning in a full-duplex environment for the MII/SYM and 10BASE-T ports.

1.3 21145 Block Diagram

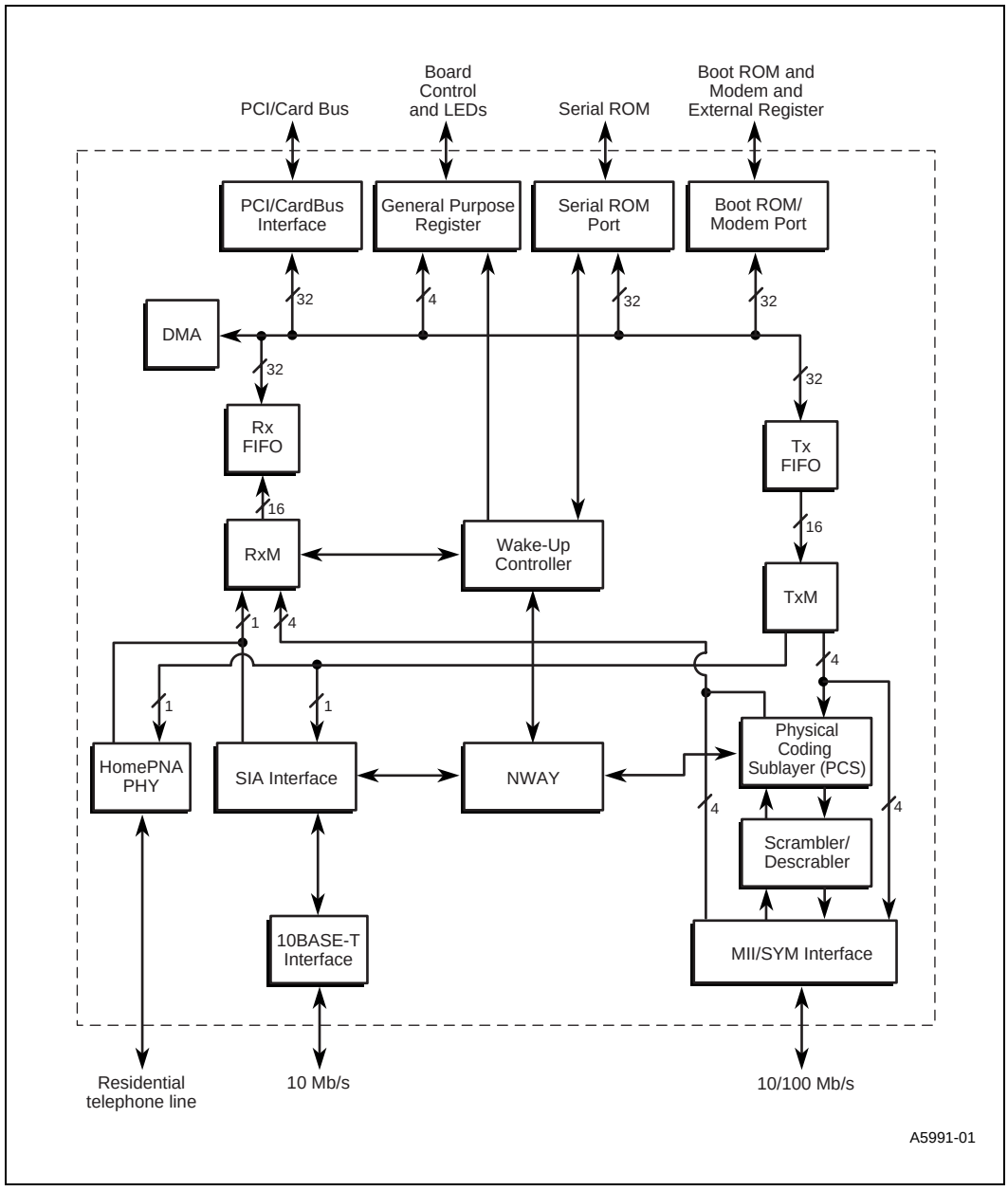
The following list describes the 21145 hardware components, and Figure 1 shows a block diagram of the 21145:

- PCI/CardBus interface—Includes all interface functions to the PCI and CardBus bus. Handles all interconnect control signals; and executes DMA and I/O transactions.
- Boot ROM/Modem port—Provides an interface to perform read and write operations to ISA compliant modem chipsets and to the boot ROM; supports accesses to bytes or longwords (32-bit) to the boot ROM. Provides the ability to connect an external 8-bit register to the boot ROM port.
- Serial ROM port—Provides a direct interface to a MicroWire ROM for storage of the Ethernet address and system parameters.
- General-purpose register—Enables software use for input or output functions and LEDs.
- DMA—Contains independent receive and transmit controllers; handles data transfers between CPU memory and onchip memory.
- FIFOs—Contains independent FIFOs for receive and transmit. Supports automatic packet deletion on receive (runt packets or after a collision) and packet retransmission after a collision on transmit.
- RxM—Handles all CSMA/CD[1] receive operations, and transfers the network data from the ENDEC to the receive FIFO.
- TxM—Handles all CSMA/CD MAC[2] transmit operations, and transfers data from transmit FIFO to the ENDEC for transmission.
- SIA interface—Performs 10 Mb/s physical layer network operations; implements the HomePNA and 10BASE-T functions, including the Manchester encoder and decoder functions.
- NWAY—Implements the IEEE 802.3 Auto-Negotiation algorithm.
- Physical coding sublayer—Implements the encoding and decoding sublayer of the 100BASE-TX (CAT5) specification, including the squelch feature.
- HomePNA PHY—Implements the HomePNA telephone network interface.
- Scrambler/descrambler—Implements the twisted-pair physical layer medium dependent (TP-PMD) scrambler/descrambler scheme for 100BASE-TX.

1. Carrier-sense multiple access with collision detection.
2. Media access control.

- Three network interfaces—A HomePNA interface, a 10BASE-T interface, and an MII/SYM interface provide a full MII signal interface and direct interface to the 100 Mb/s ENDEC for CAT5.
- Wake-up-controller—Enables power-management control compliant with the ACPI.

Figure 1. 21145 Block Diagram



2.0 Pinout and Signal Descriptions

This section describes the 21145 pinouts and signals.

2.1 21145 Pinout

The 21145 is offered as a 176-pin LQFP or a 144-pin LQFP. Figure 2 and Figure 3 show the 176-pin and 144-pin device pinouts respectively.

Figure 2. 21145 176-pin Pinout Diagram (Top View)

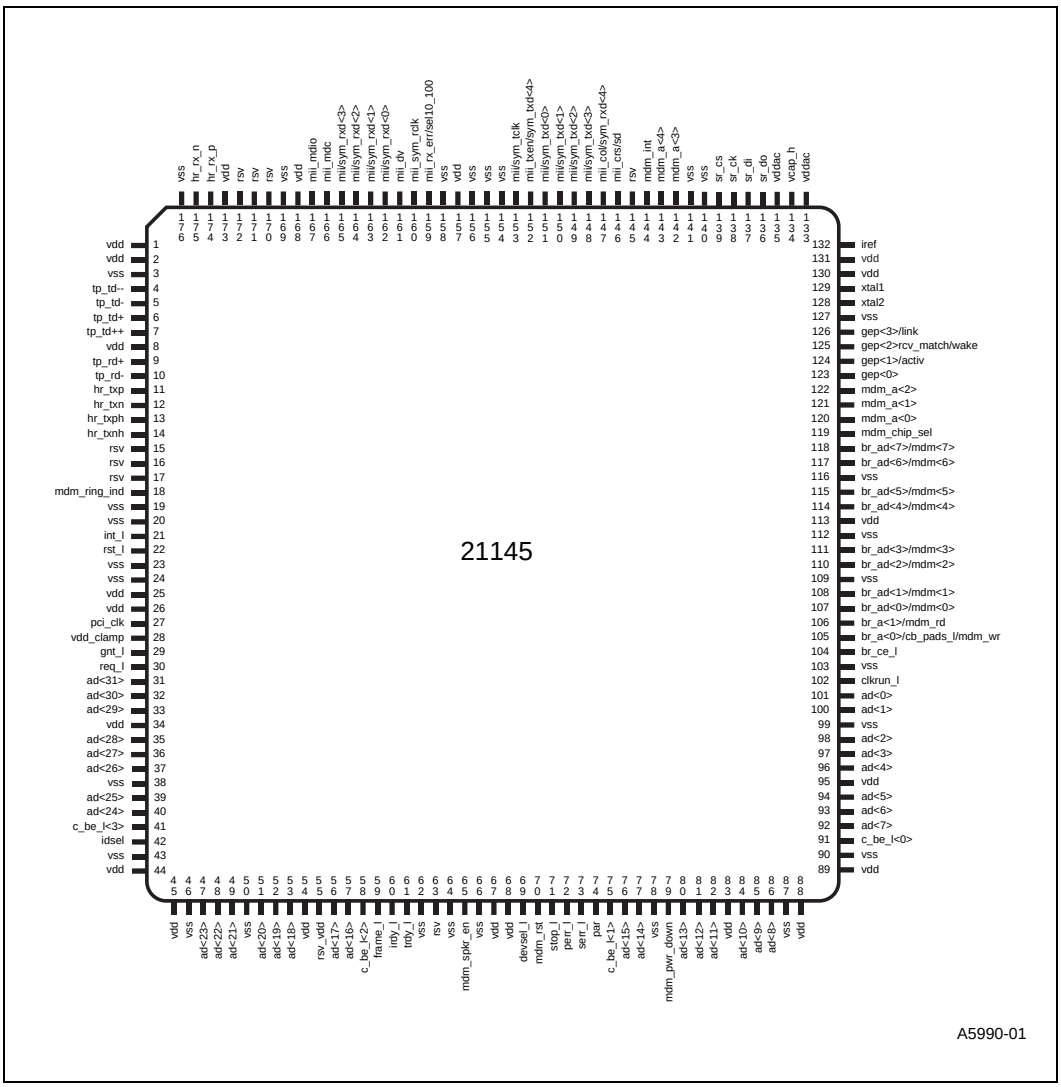
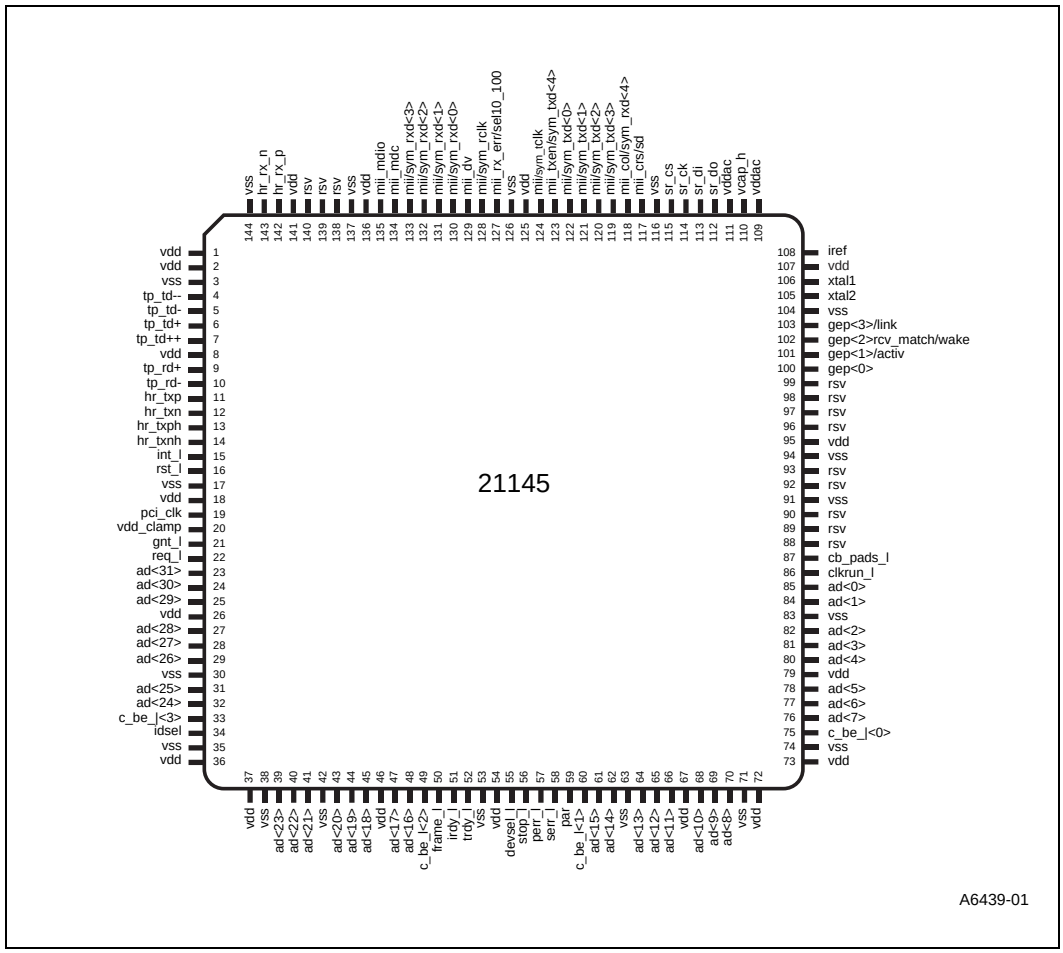


Figure 3. 21145 144-pin Pinout Diagram (Top View)



2.2 Signal Descriptions

The following terms describe the 21145 pinout used in Table 1:

- Address phase
  Address and appropriate bus commands are driven during this cycle.
- Data phase
  Data and the appropriate byte enable codes are driven during this cycle.
- _l
  All pin names with the **_l** suffix are active low.

The following abbreviations are used in Table 1:

O = Output
I/O = Input/output
O/D = Open drain

P = Power

Pins labeled rsv are reserved for future use and must be left unconnected.

The following signals have an internal pull-up:

sr_do

mii/sym_tclk

Signal sr_cs has an internal pull-down.

Table 1 provides a functional description of each of the 21145 signals. These signals are listed alphabetically.

Table 1. Functional Description of 21145 Signals (Sheet 1 of 8)

Signal	Type	Pin Number, 176-pin	Pin Number, 144-pin	Description
ad<31:0>	I/O	31, 32, 33, 35, 36, 37, 39, 40, 47, 48, 49, 51, 52, 53, 56, 57, 76, 77, 80, 81, 82, 84, 85, 86, 92, 93, 94, 96, 97, 98, 100, 101	23, 24, 25, 27, 28, 29, 31, 32, 39, 40, 41, 43, 44, 45, 47, 48, 61, 62, 64, 65, 66, 68, 69, 70, 76, 77, 78, 80, 81, 82, 84, 85	32-bit PCI address and data lines. Address and data bits are multiplexed on the same pins. During the first clock cycle of a transaction, the address bits contain a physical address (32 bits). During subsequent clock cycles, these same lines contain 32 bits of data. A 21145 bus transaction consists of an address phase followed by one or more data phases. The 21145 supports both read and write bursts (in master operation mode only). Little and big endian byte ordering can be used.
br_a<0>/cb_pads_l/ mdm_wr (on 176 pins) br_a<0>/cb_pads_l (on 144 pins)	I/O	105	87	**For the 176-pin 21145 only**: During operation, when accessing the modem chipset (mdm_chip_sel is asserted), this pin is used as the modem write line and is active low. When the modem is not accessed (mdm_chip_sel is deasserted), this pin is used as the expansion ROM address line bit 0. In a 256KB configuration, this pin also carries in two consecutive address cycles, expansion ROM address bits 16 and 17. **For both the 144-pin and 176-pin 21145**: During reset, this pin also determines the type of signals to use for the PCI/CardBus output pins, either PCI or CardBus. By default, this pin selects PCI signaling. To select CardBus signaling, this pin must be connected to a pull-down resistor.
br_a<1>/mdm_rd	O	106	NA	**For the 176-pin 21145 only**: During operation, when accessing the modem chipset (mdm_chip_sel is asserted), this pin is used as the modem read line and is active low. When the modem is not accessed (mdm_chip_sel is deasserted), this pin is used as the expansion ROM address line bit 1. This pin also latches the expansion ROM address and control lines by the two external latches.

Table 1. Functional Description of 21145 Signals (Sheet 2 of 8)

Signal	Type	Pin Number, 176-pin	Pin Number, 144-pin	Description
br_ad<7:0>/ <mdm<7:0>	I/O	107, 108, 110, 111, 114, 115, 117, 118	NA	**For the 176-pin 21145 only**: During operation, when accessing the modem chipset (mdm_chip_sel is asserted), these pins are used as the modem data lines bits 7 through 0. When the modem is not accessed (mdm_chip_sel is deasserted), these pins are used as the expansion ROM address and data lines.
br_ce_l	O	104	NA	Expansion ROM or external register chip enable.
c_be_l<3:0>	I/O	41, 58, 75, 91	33, 49, 60, 75	Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins. During the address phase of the transaction, these 4 bits provide the bus command. During the data phase, these 4 bits provide the byte enable. The byte enable determines which byte lines carry valid data. For example, bit 0 applies to byte 0, and bit 3 applies to byte 3.
clkrun_l	I/O O/D	102	86	PCI/CardBus clock run indication. The host system asserts this signal to indicate normal operation of the clock. The host system deasserts clkrun_l when the clock is going to be stopped or slowed down to a nonoperational frequency. If the clock is needed by the 21145, the 21145 asserts clkrun_l, requesting normal clock operation to be maintained or restored. Otherwise, the 21145 allows the system to stop the clock.
devsel_l	I/O	69	55	Device select is asserted by the target of the current bus access. When the 21145 is the initiator of the current bus access, it expects the target to assert devsel_l within 5 bus cycles, confirming the access. If the target does not assert devsel_l within the required bus cycles, the 21145 aborts the cycle. To meet the timing requirements, the 21145 asserts this signal in a medium speed (within 2 bus cycles).
frame_l	I/O	59	50	The frame_l signal is driven by the bus master to indicate the beginning and duration of an access. The frame_l signal asserts to indicate the beginning of a bus transaction. While frame_l is asserted, data transfers continue. The frame_l signal deasserts to indicate that the next data phase is the final data phase transaction.
gep<0>	I/O	123	100	This pin can be configured by software to be a general-purpose pin that performs either input or output functions. This general-purpose pin can provide an interrupt when functioning as an input.
gep<1>/activ	I/O	124	101	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. This general-purpose pin can provide an interrupt when functioning as an input. • A status pin that provides an LED that indicates either receive or transmit activity.

Table 1. Functional Description of 21145 Signals (Sheet 3 of 8)

Signal	Type	Pin Number, 176-pin	Pin Number, 144-pin	Description
gep<2>/rcv_match/ wake	I/O	125	102	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. • A status pin that provides an LED that indicates a receive packet has passed address recognition. This pin can also be controlled by PME_Enable bit (Func0_HwOptions<3>) in the serial ROM to be a wake-up event pin that can be connected to pin pme# of the PCI connector or pin cstschg of the CardBus connector. When this pin is in a wake function, bit MiscHwOptions<1> in the serial ROM determines the polarity.
gep<3>/link	I/O	126	103	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. • A status pin that provides an LED to indicate (according to the MiscHWOptions<0> field in the Serial ROM): — Network link integrity state for 10BASE-T or 100BASE-TX. — Both network activity and network link integrity state. • An input link status pin for OnNow support. When used with an MII PHY device, this pin should be connected to the MII PHY link indication pin (the 21145 interprets a high logic level on this pin as link-pass). This pin should not be left unconnected if it is used as an input in the D1, D2, or D3 power states.
gnt_l	I	29	21	Bus grant asserts to indicate to the 21145 that access to the bus is granted.
hr_rx_n	I	175	143	HomePNA negative differential receive input from the phone line.
hr_rx_p	I	174	142	HomePNA positive differential receive input from the phone line.
hr_txn	O	12	12	HomePNA negative differential transmit output to phone line.
hr_txnh	O	14	14	HomePNA high power negative differential transmit output to phone line.
hr_txp	O	11	11	HomePNA positive differential transmit output to phone line.
hr_txph	O	13	13	HomePNA high power positive differential transmit output to phone line.
idsel	I	42	34	Initialization device select asserts to indicate that the host is issuing a configuration cycle to the 21145.

Table 1. Functional Description of 21145 Signals (Sheet 4 of 8)

Signal	Type	Pin Number, 176-pin	Pin Number, 144-pin	Description
int_l	O/D	21	15	Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. Interrupt request deasserts by writing a 1 into the appropriate CSR5 bit. If more than one interrupt bit is asserted in CSR5 and the host does not clear all input bits, the 21145 deasserts int_l for one cycle to support edge-triggered systems.
iref	I	132	108	Current reference input for the analog phase-locked loop logic.
irdy_l	I/O	60	51	Initiator ready indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of the clock when both irdy_l and target ready trdy_l are asserted. Wait cycles are inserted until both irdy_l and trdy_l are asserted together. When the 21145 is the bus master, it asserts irdy_l during write operations to indicate that valid data is present on the 32-bit ad lines. During read operations, the 21145 asserts irdy_l to indicate that it is ready to accept data.
mdm_a<4:0>	O	120, 121, 122, 142, 143	NA	Modem address lines. Address lines that are not needed in order to access the modem should be left unconnected. For example, if the modem chipset has only 8 registers, mdm_a<4:3> should be left unconnected.
mdm_chip_sel	O	119	NA	Modem chip select. This pin is active low.
mdm_int	I	144	NA	Modem interrupt line. When asserted, the 21145 asserts the int_l pin. This pin is active high. It must be connected to a pull-down resistor.
mdm_pwr_down	O	79	NA	Modem power down. This pin is asserted when the modem function is in D3 power state. It can be used by the modem chipset power control. The polarity of this pin is determined by the Func1_HwOptions<5> bit in the serial ROM.
mdm_ring_ind	I	18	NA	Modem ring indicator. The assertion of this pin affects the assertion of the wake pin. The polarity of this pin is determined by the Func1_HwOptions<4> bit in the serial ROM. This pin must not be left floating.
mdm_rst	O	70	NA	Modem reset. This pin is asserted for 15 µs from the end of the 21145's power-up reset pulse, and on moving from the D3 to the D0 power state.
mdm_spkr_en	O	65	NA	Modem speaker enable. This pin reflects the Audio enable bits of the modem function Status Changed registers. If the Func1_HwOptions<7> bit in the serial ROM is set, the value of the FEMR<5> is driven on the MDM_SPKR_EN pin. If the Func1_HwOptions<7> is cleared, the value of FEMR<6> is driven on the MDM_SPKR_EN pin.

Table 1. Functional Description of 21145 Signals (Sheet 5 of 8)

Signal	Type	Pin Number, 176-pin	Pin Number, 144-pin	Description
mii_clsn/sym_rxd<4>	I	147	118	In MII mode (CSR6<18>=1, CSR6<23>=0), this pin functions as the collision detect. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin. In SYM mode (CSR6<18>=1, CSR6<23>=1), this pin functions as receive data. This line along with the four receive lines (sym_rxd<3:0>) provides five parallel data lines in symbol form. This data is controlled by an external physical layer medium-dependent (PMD) device and should be synchronized to the sym_rclk signal.
mii_crs/sd	I	146	117	In MII mode this pin functions as the carrier sense and is asserted by the PHY when the media is active. In SYM mode this pin functions as the signal detect indication. It is controlled by an external PMD device. If no PHY device is connected to the MII/SYM port, the mii_crs/sd pin should be tied to Vss in order to make the link-integrity test function properly.
mii_dv	I	161	129	Data valid is asserted by an external PHY when receive data is present on the mii_rxd lines and is deasserted at the end of the packet. This signal should be synchronized with the mii_rclk signal.
mii_mdc	O	166	134	MII management data clock is sourced by the 21145 to the MII PHY device as a timing reference for the transfer of information on the mii_mdio signal.
mii_mdio	I/O	167	135	MII management data input/output transfers control information and status between the PHY and the 21145. This signal should be tied to an external pullup resistor if an MII PHY is connected, and to an external pulldown resistor otherwise.
mii/sym_rclk	I	160	128	Supports either the 25-MHz or 2.5-MHz receive clock. This clock is recovered by the PHY.
mii_rx_err/sel10_100	I/O	159	127	When used with an MII PHY device (CSR6<18>=1, CSR6<23>=0), this pin functions as receive error input. It is asserted when a data decoding error is detected by an external PHY device. This signal is synchronized to mii_rclk and can be asserted for a minimum of one receive clock. When asserted during a packet reception, it sets the cyclic redundancy check (CRC) error bit in the receive descriptor (RDES0). When used with a SYM PHY device (CSR6<23>=1), this pin functions as select 10/100 output. The signal sel10_100 equals 1 when the 21145 is in 100-Mb/s SYM mode (CSR6<18>=1) and equals 0 when the 21145 is in 10BASE-T mode (CSR6<18>=0).
mii/sym_rxd<3:0>	I	162, 163, 164, 165	130,131, 132,133,	Four parallel receive data lines. This data is driven by an external PHY that attached the media and should be synchronized with the mii_rclk signal.
mii/sym_tclk	I	153	124	Supports the 25-MHz or 2.5-MHz transmit clock supplied by the external PMD device. This clock should always be active.

Table 1. Functional Description of 21145 Signals (Sheet 6 of 8)

Signal	Type	Pin Number, 176-pin	Pin Number, 144-pin	Description
mii/sym_txd<3:0>	O	148, 149, 150, 151	119, 120, 121, 122	Four parallel transmit data lines. This data is synchronized to the assertion of the mii_tclk signal and is latched by the external PHY on the rising edge of the mii_tclk signal.
mii_txen/sym_txd<4>	O	152	123	In MII mode, this pin functions as transmit enable. It indicates that a transmission is active on the MII port to an external PHY device. In SYM mode, this pin functions as transmit data. This line along with the four data transmit lines (sym_txd<3:0>) provides five parallel data lines in symbol form. The data is synchronized to the rising edge of the sym_tclk signal.
par	I/O	74	59	Parity is calculated by the 21145 as an even parity bit for the 32-bit ad and 4-bit c_be_l lines. During address and data phases, parity is calculated on all the ad and c_be_l lines whether or not any of these lines carry meaningful information.
pci_clk	I	27	19	The clock provides the timing for the 21145 related PCI bus transactions. All the bus signals are sampled on the rising edge of pci_clk. The supported clock frequency range is 20 MHz to 33 MHz.
perr_l	I/O	72	57	Parity error asserts when a data parity error is detected. When the 21145 is the bus master and a parity error is detected, the 21145 asserts both CSR5 bit 13 (fatal bus error) and CFCS bit 24 (data parity report). Next, it completes the current data burst transaction, then stops operation. After the host clears the system error via CSR5<13>, the 21145 continues its operation. The 21145 asserts perr_l when a data parity error is detected in either a master-read or a slave-write operation.
req_l	O	30	22	Bus request is asserted by the 21145 to indicate to the bus arbiter that it wants to use the bus.
rst_l	I	22	16	Resets the 21145 to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all PCI output pins are put into tristate and all PCI O/D signals are floated.
rsv	—	15, 16, 17, 63, 145, 170, 171, 172	88, 89, 90, 92, 93, 96, 97, 98, 99, 138, 139, 140	Reserved. These pins should remain unconnected.
rsv_vdd	I	55	NA	Must be connected to Vdd for proper operation.
serr_l	O/D	73	58	If an address parity error is detected and CFCS bit 8 (serr_l enable) is enabled, 21145 asserts both serr_l (system error) and CFCS bit 30 (signal system error). When an address parity error is detected, system error asserts two clocks after the failing address.
sr_ck	O	138	114	Serial ROM clock signal. This pin provides a serial clock output for the serial ROM.
sr_cs	O	139	115	Serial ROM chip-select signal. This pin provides a chip select for the serial ROM.

Table 1. Functional Description of 21145 Signals (Sheet 7 of 8)

Signal	Type	Pin Number, 176-pin	Pin Number, 144-pin	Description
sr_di	O	137	113	Serial ROM data-in signal. This pin serially shifts the write data from the 21145 to the serial ROM device.
sr_do	I	136	112	Serial ROM data-out signal. This pin serially shifts the read data from the serial ROM device to the 21145.
stop_l	I/O	71	56	Stop indicator indicates that the current target is requesting the bus master to stop the current transaction. The 21145 responds to the assertion of stop_l when it is the bus master, either to disconnect, retry, or abort.
tp_rd–	I	10	10	Twisted-pair negative differential receive data from the twisted-pair lines.
tp_rd+	I	9	9	Twisted-pair positive differential receive data from the twisted-pair lines.
tp_td– tp_td– –	O O	5 4	5 4	Twisted-pair negative differential transmit data. The positive and negative differential transmit data outputs are combined resistively outside the 21145 with equalization to compensate for intersymbol interference on the twisted-pair medium.
tp_td+ tp_td+ +	O O	6 7	6 7	Twisted-pair positive differential transmit data. The positive and negative differential transmit data outputs are combined resistively outside the 21145 with equalization to compensate for intersymbol interference on the twisted-pair medium.
trdy_l	I/O	61	52	Target ready indicates the target agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both trdy_l and irdy_l are asserted. Wait cycles are inserted until both irdy_l and trdy_l are asserted together. When the 21145 is the bus master, target ready is asserted by the bus slave on the read operation, which indicates that valid data is present on the ad lines. During a write cycle, it indicates that the target is prepared to accept data.
vcap_h	I	134	110	Capacitor input for analog phase-locked loop logic.
vdd	P	1, 2, 8, 25, 26, 34, 44, 45, 54, 67, 68, 83, 88, 89, 95, 113, 130, 131, 157, 168, 173	1, 2, 8, 18, 26, 36, 37, 46, 54, 67, 72, 73, 79, 95, 107, 125, 136, 141	3.3-V supply input. These pins should be connected to the auxiliary power, if such power exists. Otherwise, these pins should be connected to the main power.
vddac	P	133, 135	109,111	Supplies +3.3-V input for analog phase-locked loop logic. These pins should each be decoupled with a separate 0.1 µf capacitor to ground. The capacitors should be located as close to the package pins as possible.
vdd_clamp	P	28	20	Supplies +5-V or +3.3-V reference for clamp logic. This pin is also used to determine the lack of main power when the auxiliary power is on. It should be connected to the main power. This pin determines whether 5 V or 3.3 V signalling is used on the PCI bus.

Table 1. Functional Description of 21145 Signals (Sheet 8 of 8)

Signal	Type	Pin Number, 176-pin	Pin Number, 144-pin	Description
vss	P	3, 19, 20, 23, 24, 38, 43, 46, 50, 62, 64, 66, 78, 87, 90, 99, 103, 109, 112, 116, 127, 140, 141, 154, 155, 156, 158, 169, 176	3, 17, 30, 35, 38, 42, 53, 63, 71, 74, 83, 91, 94, 104, 116, 126, 137, 144	Ground pins.
xtal1	I	129	106	20-MHz crystal input, or crystal oscillator input. This input should always be active.
xtal2	O	128	105	Crystal feedback output pin used for crystal connections only. If this pin is unused, then it should be unconnected.

2.3 Pin Tables

This section contains four types of pin tables:

- Table 2 lists the input pins.
- Table 3 lists the output pins.
- Table 4 lists the input/output pins.
- Table 5 lists the open drain pins.

Table 2. Input Pins (Sheet 1 of 2)

Signal	Active Level
hr_rx_n	Analog
hr_rx_p	Analog
gnt_l	Low
idsel	High
iref	—
mdm_int	High
mdm_ring_ind	Dependent on Func1_HWOptions<4> in the Serial ROM.
mii_clsn/sym_rxd<4>	High for mii_clsn, NA for sym_rxd<4>.
mii_crs/sd	High
mii_dv	High
mii/sym_rclk	—
mii/sym_rxd<3:0>	—
mii/sym_tclk	—
pci_clk	—

Table 2. Input Pins (Sheet 2 of 2)

Signal	Active Level
rst_l	Low
rsv_vdd	—
sr_do	—
tp_rd–	—
tp_rd+	—
vcap_h	—
xtal1	—

Table 3. Output Pins

Signal	Active Level
br_ce_l	Low
hr_txn	—
hr_txnh	—
hr_txp	—
hr_txph	—
mdm_a<4:0>	—
mdm_chip_sel	Low
mdm_pwr_down	Dependent on Func1_HWOptions<5> in the Serial ROM.
mdm_spkr_en	High
mii_mdc	—
mii/sym_txd<3:0>	—
mii_txen/sym_txd<4>	High for mii_txen, low for sym_txd<4>.
req_l	Low
sr_ck	—
sr_cs	High
sr_di	—
tp_td–	—
tp_td– –	—
tp_td+	—
tp_td+ +	—
xtal2	—

Table 4. Input/Output Pins

Signal	Active Level
ad<31:0>	—
br_a<0>/cb_pads_l	High for br_a<0>, low for cb_pads_l.
br_ad<7:0>	—
clkrun_l	Low
c_be_l<3:0>	Low
devsel_l	Low
frame_l	Low
gep<0>	—
gep<1>/activ	NA for gep<1>, high for activ.
gep<2>/rcv_match/wake	NA for gep<2>, high for rcv_match, controlled by bit MiscHwOptions<1> (PME_STSCHG) in the serial ROM for wake. Tristate when not used as wake.
gep<3>/link	NA for gep<3>, high for link.
irdy_l	Low
mii_mdio	—
mii_rx_err/sel10_100	High for mii_rx_err, NA for sel10_100.
par	High
perr_l	Low
stop_l	Low
trdy_l	Low

Table 5. Open Drain Pins

Signal	Active Level
clkrun_l	Low
int_l	Low
serr_l	Low
wake	Controlled by bit MiscHwOptions<1> (PME_STSCHG) in the serial ROM.

2.4 Signal Grouping by Function

Table 6 lists the signals according to their interface function.

Table 6. Signal Functions (Sheet 1 of 2)

Interface	Function	Signals
PCI/CardBus	Address and data	ad<31:0>, par
	Arbitration	gnt_l, req_l
	Bus command and byte enable	c_be_l<3:0>
	Device select	devsel_l, idsel
	Error reporting	perr_l, serr_l
	Interrupt	int_l
	System	pci_clk, rst_l
	Control signals	frame_l, stop_l, irdy_l, trdy_l
	Power-management status	wake
	Clock status	clkrun_l
	Pad select	cb_pads_l
Modem Connections (176-pin 21145 only)	Address lines	mdm_a<4:0>
	Data lines	mdm<7:0>
	Chip select	mdm_chip_sel
	Read line	mdm_rd
	Write line	mdm_wr
	Interrupt	mdm_int
	Power down	mdm_pwr_down
	Reset	mdm_rst
	Ring indicator	mdm_ring_ind
	Speaker enable	mdm_spkr_en
MII/SYM network port	Transmit data lines	mii/sym_txd<3:0>
	Receive data lines	mii/sym_rxd<3:0>
	Transmit, receive clocks	mii/sym_tclk, mii/sym_rclk
	Transmit enable	mii_txen
	Collision detect	mii_clsn
	MII error reporting	mii_rx_err
	Data control	mii_dv, mii_crs
	MII management data clock	mii_mdc
	MII management data input/output	mii_mdio
	Signal detection	sd
	SYM mode data lines	sym_rxd<4>, sym_txd<4>
	SYM mode 10/100 select	sel10_100
Serial ROM port	Serial ROM	sr_ck, sr_cs, sr_di, sr_do
Expansion port (176-pin 21145 only)	ROM interface	br_a<1:0>, br_ad<7:0>

Table 6. Signal Functions (Sheet 2 of 2)

Interface	Function	Signals
Power	3.3-V or 5.0-V supply input	vdd_clamp
	3.3-V supply input	vdd, vddac
	Ground	vss
General-purpose port and LEDs	General-purpose pins	gep<3:0>
	LED indicators	activ, rcv_match, link
Network connection	Analog phase-locked loop logic	iref, vcap_h
	Crystal oscillator	xtal1, xtal2
	Twisted-pair transmit and receive data	tp_rd–, tp_rd+, tp_td–, tp_td– –, tp_td+, tp_td+ +
HomePNA port	Connect to phone line	hr_txp, hr_txn, hr_txph, hr_txnh, hr_rx_p, hr_rx_n

3.0 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications for the 21145.

Caution: Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21145. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21145.

3.1 Voltage Limit Ratings

Table 7 lists the voltage limit ratings.

Table 7. Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	3.0 V	3.6 V
vdd_clamp (5 V)	4.75 V	5.25 V
vdd_clamp (3.3 V)[1]	3 V	3.6 V
ESD protection voltage[2]	—	2000 V

NOTE:
1. In the 3.3 V signaling environment, vdd_clamp must not be greater than vdd + 0.3 V.
2. Using the HBM (Human Body Modulation) model.

3.2 Temperature Limit Ratings

Table 8 lists the temperature limit ratings.

Table 8. Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	–55°C	+125°C
Operating temperature	0°C	+70°C

3.3 Oscillator Characteristics

When driving the 21145's integrated oscillator circuitry from an external clock source, an external clock having the following characteristics must be used to ensure proper operation of the 21145:

- Clock frequency: 20 MHz ±0.01% (100 ppm, TTL, or CMOS)
- Rise/fall time: < 4 ns
- Duty cycle: 40%–60%

Table 9 lists the specifications for the crystal oscillator.

Table 9. Crystal Oscillator Specification

Category	Value
Frequency	20 MHz
Tolerance	±0.01% at 25°C (100 ppm)
Stability	±0.005% at 0°C to 70°C (100 ppm)

3.4 Power Specifications

This section describes the power specifications for all versions of the 21145 device.

3.4.1 21145 Power Specifications

The values in Table 10 are based on a PCI or CardBus clock frequency of 25 MHz, VDD at 3.6 V, Ta at 0°C, and a network data rate of 100 Mb/s.

Table 10. 21145 Power Specifications (25 MHz)

Condition	Idd (mA)
D0 in Normal Mode, full network activity	267
D0 in Snooze Mode, 50% network activity	274
D1 in Snooze Mode, 50% network activity	206
D2 in Snooze Mode, 50% network activity	200
D3 in Snooze Mode, no network activity[1]	185
After power-up[2,3]	200

1. PCI/CardBus clock stopped.
2. Using the CardBus pads.
3. After power-up, the 21145 initializes to Sleep Mode.

The values in Table 11 are typical values based on a PCI or CardBus clock frequency of 33 MHz, VDD at 3.3 V, room temperature, and a network data rate of 1 Mb/s in the HomePNA port.

Table 11. 21145 Power Specifications (33 MHz)

Condition	Idd (mA)
D0 in Normal Mode, full network activity	190
D0 in Snooze Mode, 50% network activity	185
D1 in Snooze Mode, 50% network activity	150
D2 in Snooze Mode, 50% network activity	150
D3 in Snooze Mode, no network activity[1]	135

1. PCI/CardBus clock stopped.

3.5 PCI Bus and CardBus Electrical Parameters

This section describes the PCI Bus and CardBus characteristics for the 21145.

3.5.1 PCI and CardBus I/O Voltage Specifications

The 21145 meets the I/O voltage specifications listed in Table 12 and Table 13.

Table 12. I/O Voltage Specifications for 5 V Levels

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input high voltage	—	2 V	vdd_clamp + 0.5 V
V_{il}	Input low voltage	—	–0.5 V	0.8 V
I_i[1]	Input leakage current	0.5 V<V_{in}<2.7 V	—	±10 µA
V_{oh}	Output high voltage	I_{out}=–2 mA	2.4 V	—
V_{ol}[2]	Output low voltage	I_{out}=3 mA, 6 mA	—	0.55 V
Cap	Pin capacitance	—	5 pF	8 pF

NOTES:
1. Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up resistors (including frame_l, trdy_l, irdy_l, devsel_l, stop_l, serr_l, and perr_l) must have 6 mA.

Table 13. I/O Voltage Specifications for 3.3 V Levels

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input high voltage	—	0.475*vdd_clamp	vdd_clamp + 0.5 V
V_{il}	Input low voltage	—	–0.5 V	0.325*vdd_clamp
I_i[1]	Input leakage current	0.0 V<V_{in}<vdd_clamp	—	±70 µA
V_{oh}	Output high voltage	I_{out}=–500 µA	0.9*vdd_clamp	—
V_{ol}	Output low voltage	I_{out}=1500 µA	—	0.1*vdd_clamp
Cap	Pin capacitance	—	5 pF	8 pF

NOTES:
1. Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

3.5.2 System Bus Reset

System bus (PCI or CardBus) reset (rst_l) is an asynchronous signal that must be active for at least 10 system bus (PCI or CardBus) clock (pci_clk) cycles. Table 14 lists the reset signal limits.

Table 14. Reset Timing Parameters

Symbol	Parameter	Minimum	Maximum	Condition
T_{rst}	rst_l pulse width	100 µs	Not applicable	pci_clk active

3.5.3 PCI and CardBus Clock Specifications

The clock frequency range[1] for PCI and CardBus is between 20 MHz and 33 MHz. Figure 4 shows the PCI and CardBus clock specification timing characteristics and the required measurement points for both the 5 V and 3.3 V signaling environments. Table 15 lists the frequency-derived clock specifications.

1. The PCI and CardBus clock frequency is from dc to 33 MHz; network operational with the PCI or CardBus clock from 20 MHz to 33 MHz.

Figure 4. PCI and CardBus Clock Specification Timing Diagram

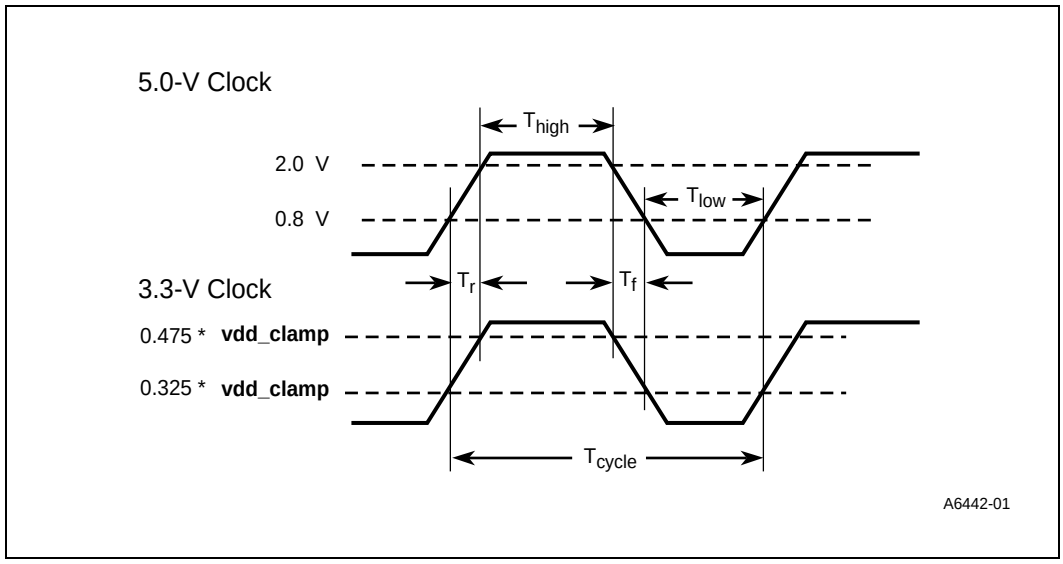


Table 15. PCI and CardBus Clock Timing Specifications

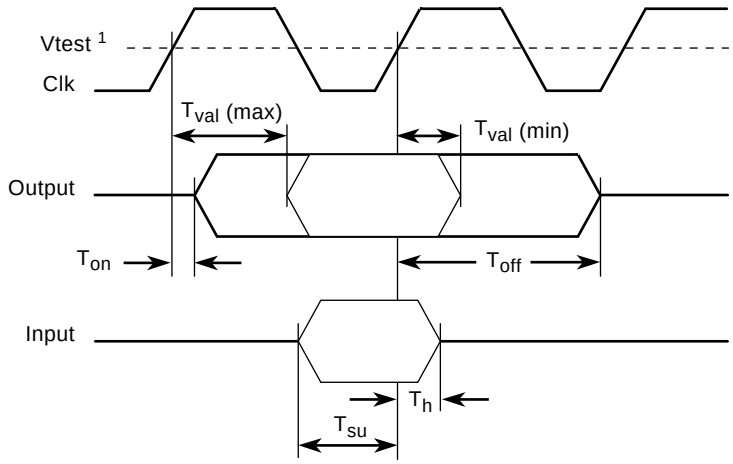
Symbol	Parameter	Minimum	Maximum
T_{cycle}	Cycle time	30 ns	50 ns
T_{high}	pci_clk high time	11 ns	-
T_{low}	pci_clk low time	11 ns	-
T_r/T_f[1]	pci_clk slew rate	1 V/ns	4 V/ns

NOTE:
1. Rise and fall times are specified in terms of the edge rate measured in V/ns.

3.5.4 Other PCI and CardBus Signals

Figure 5 shows the timing diagram characteristics for other PCI and CardBus signals and Table 16 lists their timing specifications. This timing is identical to the timing for the general-purpose register signals.

Figure 5. Timing Diagram for Other PCI and CardBus Signals



[1] Vtest is 1.5 V in a 5.0-V signaling environment and is 0.4 * **vdd_clamp** in a 3.3-V signaling environment.

A6443-01

Table 16. Other PCI and CardBus Signals' Timing Specifications

Symbol	Parameter	Minimum	Typical	Maximum
T_{val}[1]	clk-to-signal valid delay[2]	2 ns		11 ns
T_{val}[1]	clk-to-signal valid delay[3]	2 ns		18 ns
T_{on}	Float-to-active delay from clk		2 ns	—
T_{off}	Active-to-float delay from clk	—	28 ns	
T_{su}	Input signal valid setup time before clk	7 ns		—
T_h	Input signal hold time from clk	0 ns		—

NOTES:
1. Load for this measurement is as specified in *PCI Local Bus Specification,* Revision 2.0 and *PCI Local Bus Specification*, Revision 2.1.
2. Valid delays for PCI, selected by default when pin cb_pad_l is not pulled down externally.
3. Valid delays for CardBus, selected when pin cb_pad_l is pulled down externally.

3.6 HomePNA Specifications

3.6.1 HomePNA Transmit Timing Parameters (25 °C)

Table 17 describes the HomePNA transmit timing parameters.

Table 17. HomePNA Transmit Timing Parameters

Parameters	Symbol	Typical	Units	Notes
Transmit drivers Tr/Tf	hr_txn/p	2	ns	10% to 90% into 100 ohm differential
Transmit drivers Tr/Tf	hr_txph/nh	2	ns	10% to 90% into 100 ohm differential
Transmit drivers width	hr_txn/p	133	ns	—
Transmit drivers width	hr_txph/nh	133	ns	—

3.6.2 HomePNA Transmit Specifications

Table 18 gives the HomePNA transmit pads DC specifications.

Table 18. Transmit pad DC specifications

Symbol	Parameter	Condition	Minimum	Maximum	Units
I_{oh}	Output high current	0.9 Vcc	12.5	30	mA
I_{ol}	Output low current	0.1 Vcc	26	58	mA

3.6.3 HomePNA Receive Specifications

The receiver detects differential input signals between hr_rx_p and hr_rx_n that meet the waveform mask of Figure 6. The mask shows the acceptable limits of the response to a single isolated pulse that meets the HomePNA PHY transmit waveform requirements.

The parameters for Figure 6 are defined as follows:

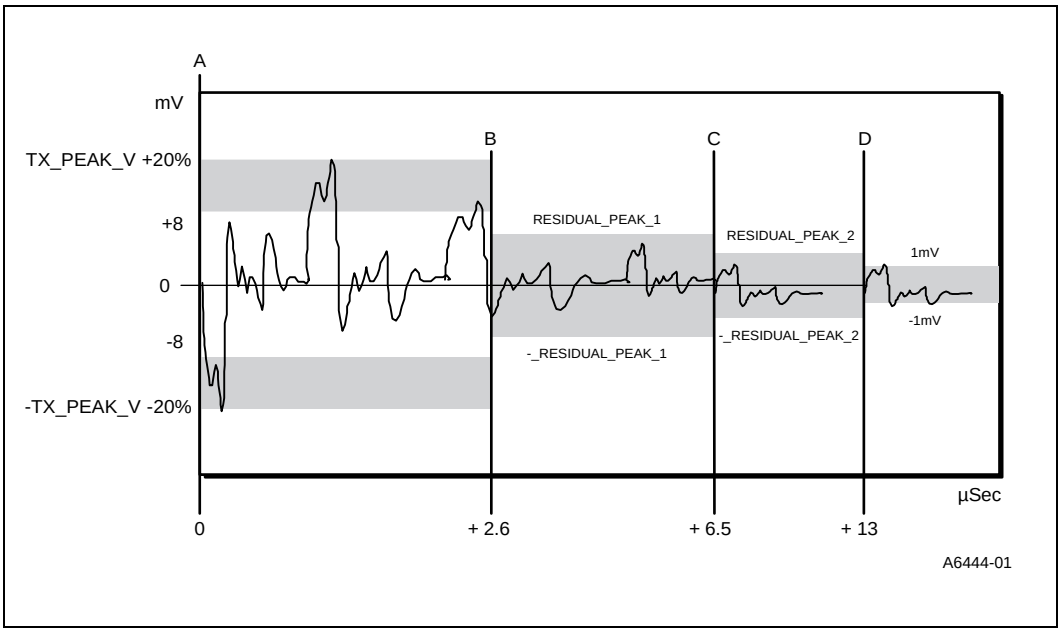
RESIDUAL_PEAK_1 = ENVELOPE_PEAK /10

RESIDUAL_PEAK_2 = ENVELOPE_PEAK /20

ENVELOPE_PEAK is defined as the peak level of the waveform arriving during interval A_B in the figure. A representative waveform that meets the mask is shown. The near DC bias is not shown and must include up to +/- 200 V to accommodate POTS signaling. The signal must form at least one peak in the shaded portion of the figure bounded between lines A and B.

Timing in the figure is referenced to the point when the signal first crosses the 5 mV threshold.

Figure 6. Receiver data symbol signal mask



3.6.4 HomePNA Receive AC Electrical Characteristics

Table 19 describes the receive AC electrical characteristics.

Table 19. HomePNA Receive AC Electrical Characteristics

Parameters	Symbol	Typical	Units	Notes
Input AC frequency	hr_rx_n/hr_rx_p	7.5	MHz	—
Input AC voltage	hr_rx_n/hr_rx_p	0.01 – 1.4	V	Differential peak

3.7 Twisted-Pair DC Specifications

Table 20 lists the DC specifications for the twisted-pair parts of the SIA.

Table 20. Twisted-Pair DC Specifications

Symbol	Definition	Condition	Minimum	Typical[1]	Maximum	Unit
V_{toh}	Output high voltage (tp_td± and tp_td±±)	I_{oh} = –25 mA	2.5		—	V
V_{tol}	Output low voltage (tp_td± and tp_td±±)	I_{ol} = 25 mA	—		0.5	V
$V_{tsq}+$	Differential positive squelch threshold (tp_rd±)	—		300—520		mV
$V_{tsq}–$	Differential negative squelch threshold (tp_rd±)	—		–520 — –300		mV
V_{tdif}	Differential input voltage range (tp_rd±)	—		–3.1 — 3.1		V

1. At 3.3 V.

3.8 Serial Interface Attachment Specifications

This section describes the dc specifications and timing limits of the SIA unit.

3.8.1 Internal SIA Mode 10BASE-T Interface Timing—Transmit

Figure 7 shows the internal SIA transmit timing characteristics for the 10BASE-T interface, and Table 21 lists the internal SIA transmit limits.

Figure 7. Internal SIA Mode 10BASE-T Interface Timing Diagram—Transmit

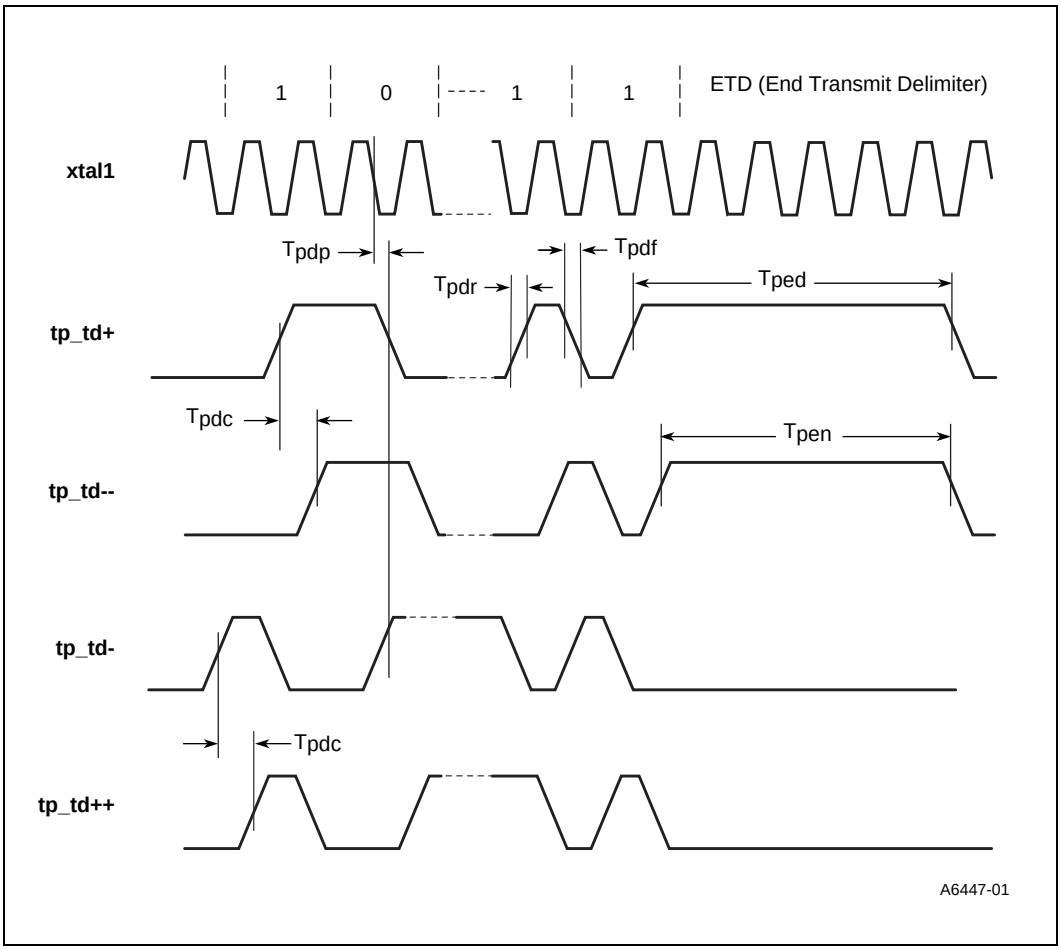


Table 21. Internal SIA Mode 10BASE-T Interface Timing Specifications—Transmit

Symbol	Definition	Minimum	Maximum	Unit
T_{pdp}	tp_td+, tp_td– propagation delay from xtal1 fall	—	30	ns
T_{pdr}	tp_td+, tp_td++, tp_td–, tp_td– – rise time	—	8	ns
T_{pdf}	tp_td+, tp_td++, tp_td–, tp_td– – fall time	—	8	ns
T_{pdm}	tp_td+, tp_td++, tp_td–, tp_td– – rise and fall time mismatch (not shown)	—	1	ns
T_{pdc}	tp_td+ to tp_td– – and tp_td– to tp_td++ delay	46	54	ns
T_{ped}	tp_td± end transmit delimiter length	295	355	ns
T_{pen}	tp_td++/– – end transmit delimiter length	245	305	ns

3.8.2 Internal SIA Mode 10BASE-T Interface Timing—Receive

Figure 8 shows the internal SIA receive timing characteristics for the 10BASE-T interface, and Table 22 lists the internal SIA receive limits for the 10BASE-T interface.

Figure 8. Internal SIA Mode 10BASE-T Interface Timing Diagram—Receive

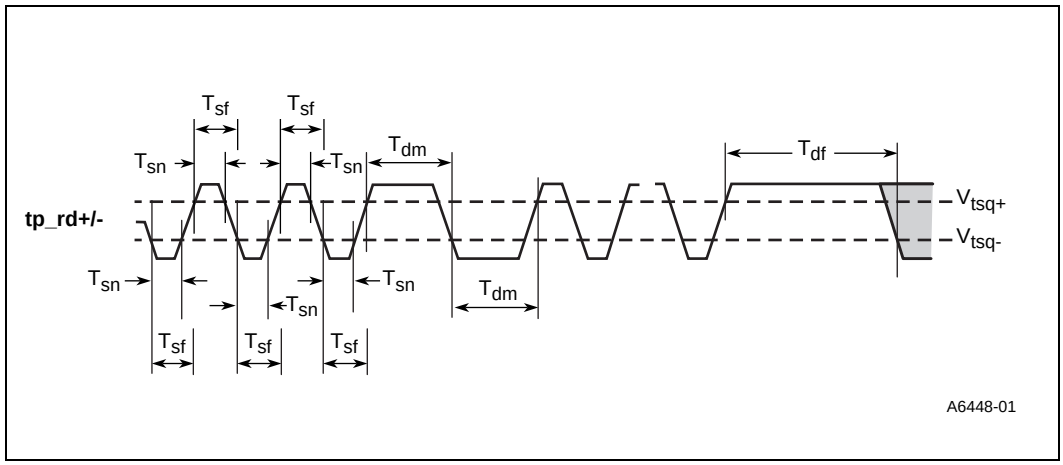


Table 22. Internal SIA Mode 10BASE-T Interface Timing Specifications—Receive

Symbol	Definition	Minimum	Maximum	Unit
T_{sn}	tp_rd± start of frame pulse width during smart squelch operation	15	20	ns
T_{sf}	tp_rd± maximum delay between opposite squelch crossings not to turn smart squelch off	140	150	ns
T_{dm}	tp_rd± delay between opposite squelch crossings not recognized as end of packet	—	140	ns
T_{df}	tp_rd± delay from last squelch crossing recognized as end of packet	150	—	ns

3.8.3 Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse

Figure 9 shows the internal SIA idle link pulse timing characteristics for the 10BASE-T interface, and Table 23 lists the internal SIA idle link pulse limits for the 10BASE-T interface.

Figure 9. Internal SIA Mode 10BASE-T Interface Timing Diagram—Idle Link Pulse

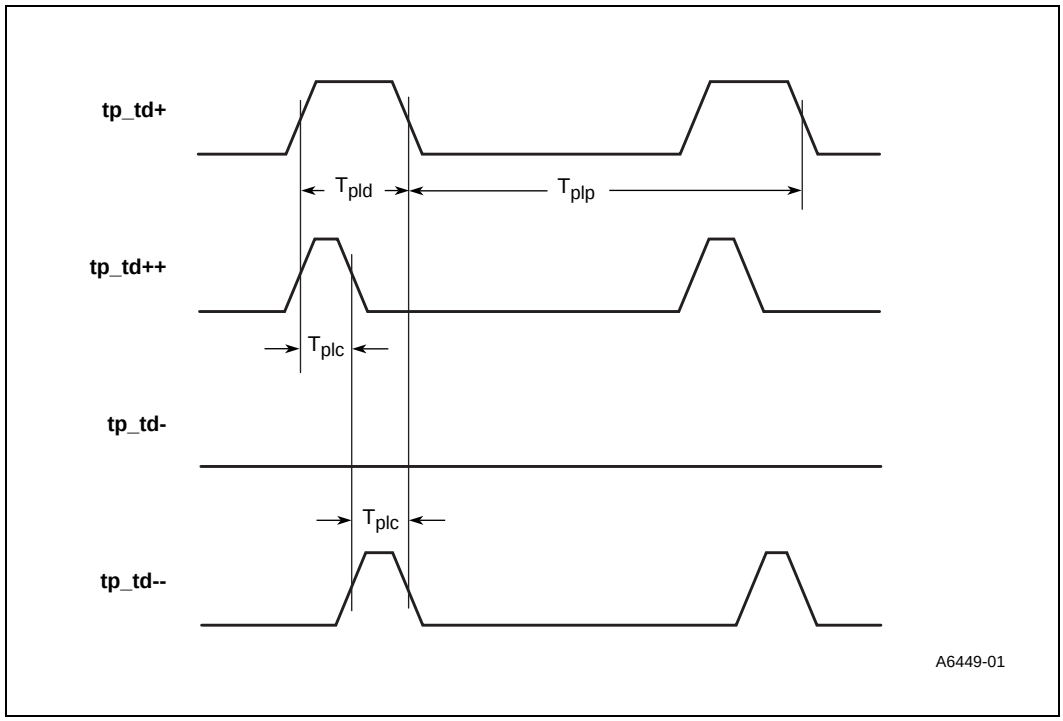


Table 23. Internal SIA Mode 10BASE-T Interface Timing Specifications—Idle Link Pulse

Symbol	Definition	Minimum	Maximum	Unit
T_{pld}	tp_td+ idle link pulse width	80	120	ns
T_{plc}	tp_td++ and tp_td– – idle link pulse width	40	60	ns
T_{plp}	Idle link pulse period	8	24	ms

3.9 MII Interface Specifications

Table 24 lists the specifications for the MII interface.

Table 24. MII Interface

Symbol	Definition	Condition	Minimum	Maximum	Unit
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	—	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{in}	Input current	V_{in} = vcc or vss	–10.0	10.0	µA
I_{oz}	Maximum tristate output leakage current	V_{in} = vdd or vss	–10.0	10.0	µA

3.10 MII/SYM Port Timing

This section describes the MII/SYM port timing limits.

3.10.1 MII/SYM 10/100 Mb/s and 10 Mb/s Timing—Transmit

Figure 10 shows the MII/SYM port transmit timing characteristics, and Table 25 lists the MII/SYM port transmit timing limits.

Figure 10. MII/SYM Port Timing Diagram—Transmit

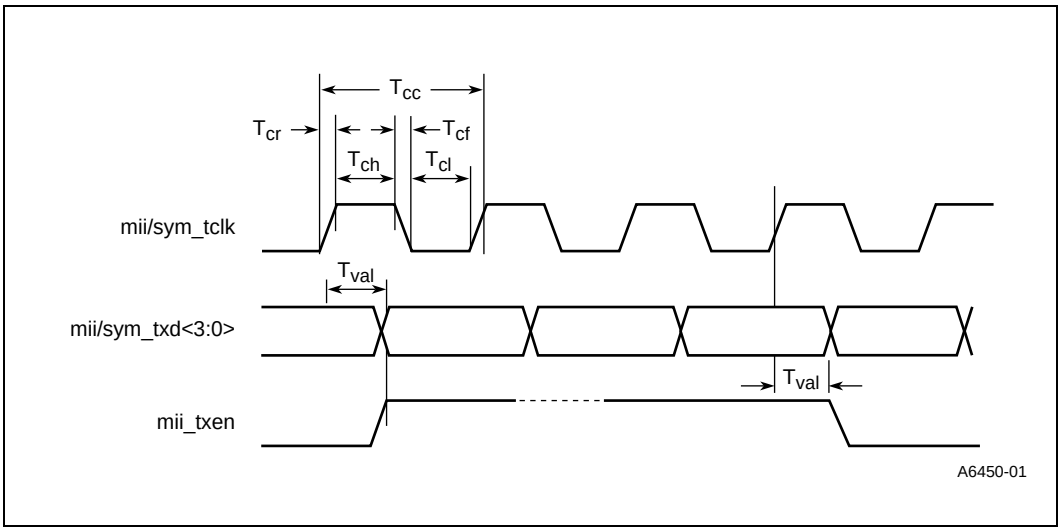


Table 25. MII/SYM Port Timing Limits—Transmit

Symbol	Definition	Minimum	Typical	Maximum	Unit
T_{cc}[1]	mii/sym_tclk cycle	—	40t[2]	—	ns
T_{ch}	mii/sym_tclk high time	14t[2]	—	26t[2]	ns
T_{cl}	mii/sym_tclk low time	14t[2]	—	26t[2]	ns
T_{cr}	mii/sym_tclk rise time	—	8	—	ns
T_{cf}	mii/sym_tclk fall time	—	8	—	ns
T_{val}	mii_tclk rise to mii_txen valid time or mii/sym_tclk rise to mii/sym_txd valid time	0	—	20	ns

NOTES:
1. ±50 parts per million.
2. t=1 for 100 Mb/s operation; t=10 for 10 Mb/s operation.

3.10.2 MII/SYM 10/100 Mb/s Timing—Receive

Figure 11 shows the MII/SYM port receive timing characteristics, and Table 26 lists the MII/SYM port receive timing limits.

Figure 11. MII/SYM Port Timing Diagram—Receive

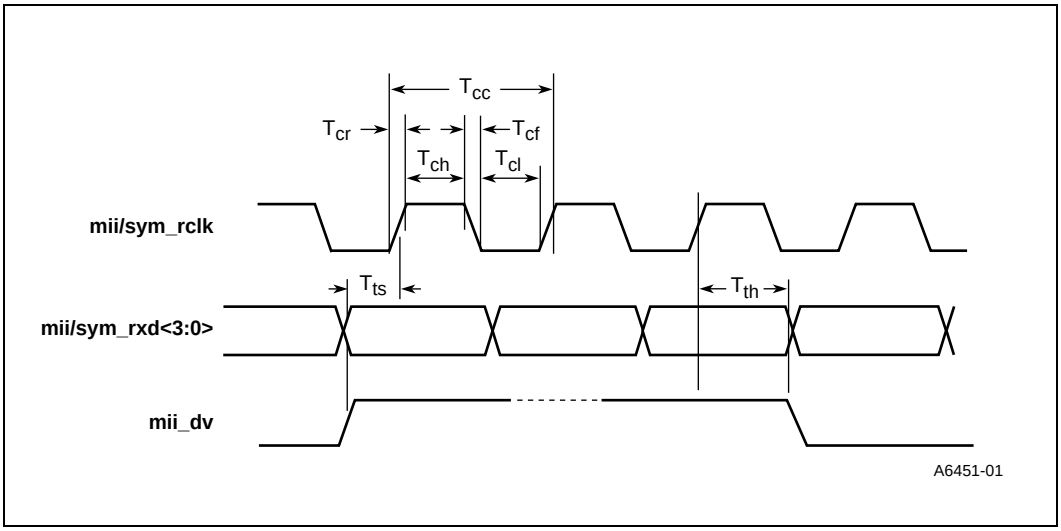


Table 26. MII/SYM Port Timing Limits—Receive (Sheet 1 of 2)

Symbol	Definition	Minimum	Typical	Maximum	Unit
T_{cc}[1]	mii/sym_rclk cycle time	—	40t[2]	—	ns
T_{c}	mii/sym_rclk high time	14t[2]	—	26t[2]	ns
T_{cl}	mii/sym_rclk low time	14t[2]	—	26t[2]	ns
T_{cr}	mii/sym_rclk rise time	—	8	—	ns
T_{cf}	mii/sym_rclk fall time	—	8	—	ns

Table 26. MII/SYM Port Timing Limits—Receive (Sheet 2 of 2)

Symbol	Definition	Minimum	Typical	Maximum	Unit
T_{ts}[3]	mii/sym_rxd setup (both rise and fall transactions) to mii/sym_rclk rise time or mii_dv setup (both rise and fall transactions) to mii_rclk rise time	8	—	—	ns
T_{th}	mii/sym_rxd hold (both rise and fall transactions) after mii/sym_rclk rise time or mii_dv hold (both rise and fall transactions) after mii_rclk rise time	10	—	—	ns

NOTES:
1. ±50 parts per million.
2. t=1 for 100 Mb/s operation; t=10 for 10 Mb/s operation.
3. The receive data (mii/sym_rxd) and data valid (mii_dv) input pins are latched internally on the rising edge of mii/sym_rclk.

3.10.3 SYM 10/100 Mb/s Timing—Signal Detect

Figure 12 shows the SYM port signal detect timing characteristics, and Table 27 lists the SYM port signal detect timing limits.

Figure 12. SYM Port Timing Diagram—Signal Detect

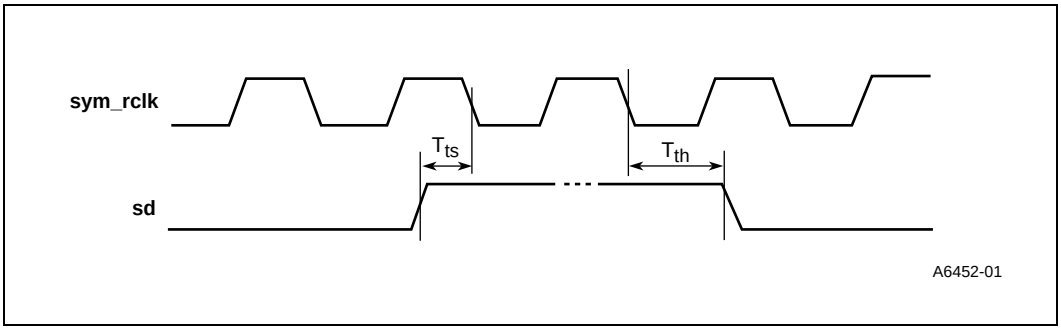


Table 27. SYM Port Timing Limits—Signal Detect

Symbol	Definition	Minimum	Maximum	Units
T_{ts}[1]	sd setup (both rise and fall transactions) to sym_rclk fall time	10	—	ns
T_{th}[1]	sd hold (both rise and fall transactions) after sym_rclk fall time	12	—	ns

NOTE:
1. Input signal detect (sd) is latched internally on the falling edge of sym_rclk.

3.10.4 MII 10/100 Mb/s Timing—Receive Error

Figure 13 shows the MII port receive error timing characteristics, and Table 28 lists the MII port receive error timing limits.

Figure 13. MII Port Timing Diagram—Receive Error

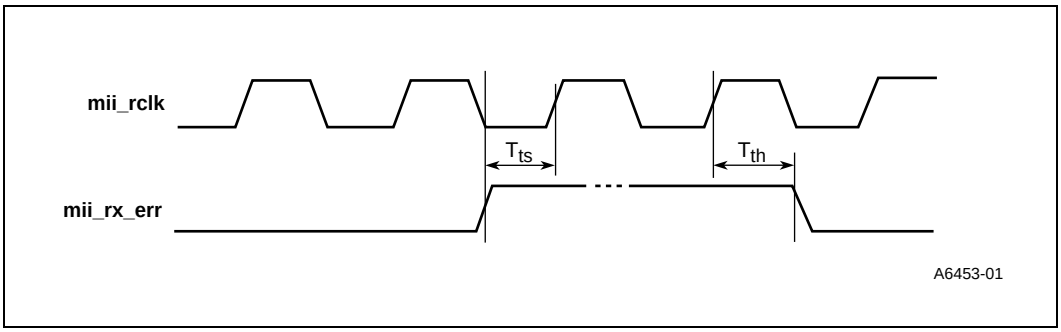


Table 28. MII Port Timing Limits—Receive Error

Symbol	Definition	Minimum	Maximum	Unit
Tts[1]	mii_rx_err setup (both rise and fall transactions) to mii_rclk rise time	10	—	ns
Tth[1]	mii_rx_err hold (both rise and fall transactions) after mii_rclk rise time	10	—	ns

NOTE:
1. Input signal detect (mii_rx_err) is latched internally on the falling edge of mii_rclk.

3.10.5 MII 10/100 Mb/s Timing—Carrier Sense and Collision

Figure 14 shows the MII port carrier sense and collision timing characteristics, and Table 29 lists the MII port carrier sense and collision timing limits.

Figure 14. MII Port Timing Diagram—Carrier Sense and Collision

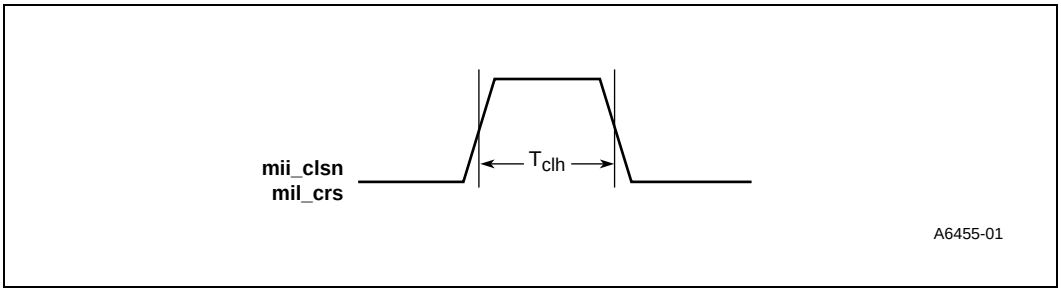


Table 29. MII Port Timing Limits—Carrier Sense and Collision

Symbol	Definition	Minimum	Maximum	Unit
Tclh	mii_crs, mii_clsn high time	80	—	ns

3.11 Expansion ROM and Serial ROM Port DC Specification

Table 30 lists the DC specifications for the expansion ROM and serial ROM ports. These specifications apply in any mode in which the ports are used.

Table 30. Expansion ROM and Serial ROM Port DC Specifications

Symbol	Definition	Condition	Minimum	Maximum	Unit
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	—	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{oz}[1]	Maximum tristate output leakage current	V_{out} = vdd or vss	–10	10	µA

NOTE:
1. For sr_do and br_ce_l, the maximum value is 1.0 µA.

3.12 Expansion ROM Port Timing

This section describes the expansion ROM port timing.

3.12.1 Expansion ROM Read Timing

Figure 15 shows the expansion ROM read timing characteristics, and Table 31 lists the expansion ROM read timing limits.

Figure 15. Expansion ROM Read Timing Diagram

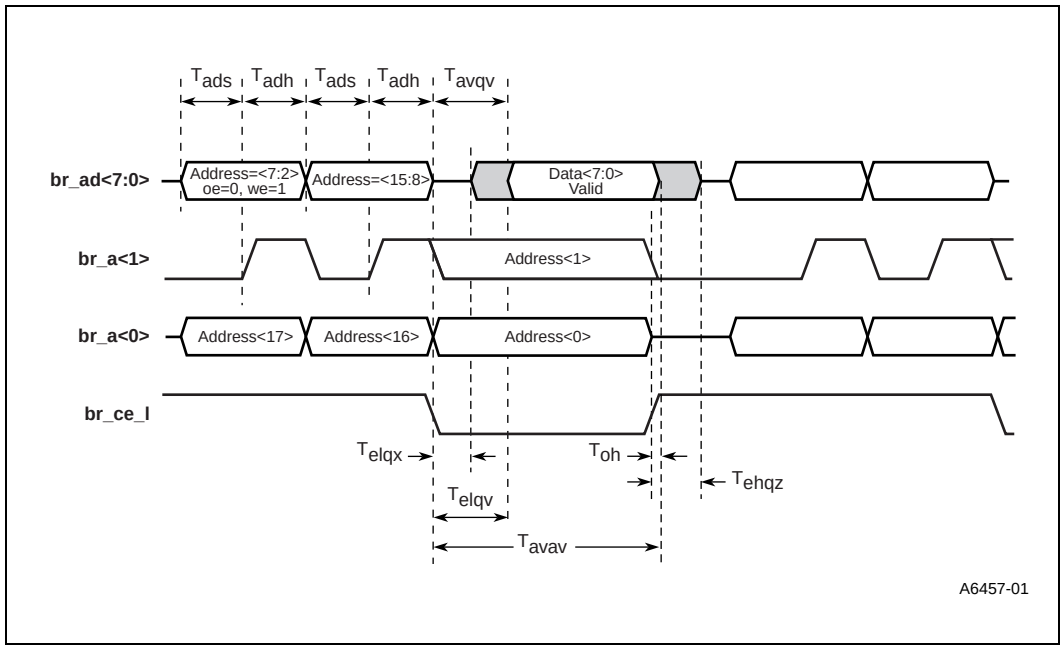


Table 31. Expansion ROM Read Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{avav}	Read cycle time	240	—	ns
T_{avqv}	Address to output delay	—	220	ns
T_{elqv}	br_ce_l to output delay	—	220	ns
T_{elqx}	br_ce_l to output low impedance	0	—	ns
T_{ehqz}	br_ce_l going high to output high impedance	—	2	pci_clk
T_{oh}	Output hold from br_ce_l change	0	—	ns
T_{ads}	Address setup to latch enable high	10	—	ns
T_{adh}	Address hold from latch enable high	10	—	ns

3.12.2 Expansion ROM Write Timing

Figure 16 shows the expansion ROM write timing characteristics, and Table 32 lists the expansion ROM write timing limits.

Figure 16. Expansion ROM Write Timing Diagram

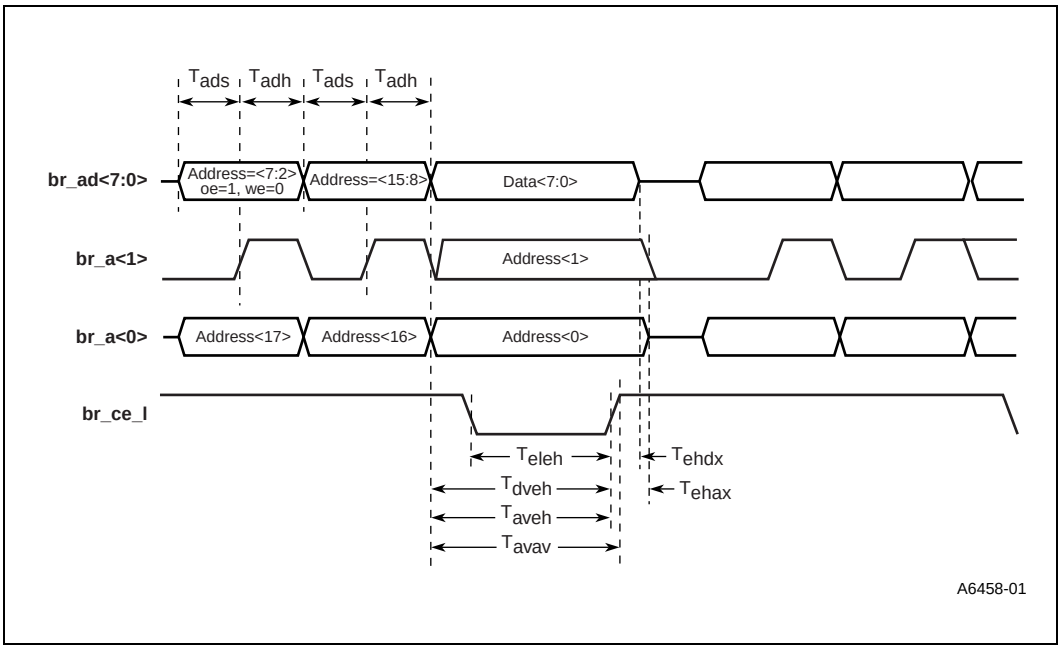


Table 32. Expansion ROM Write Timing Specifications (Sheet 1 of 2)

Symbol[1]	Parameter	Minimum	Unit
T_{avav}	Write cycle time	210	ns
T_{eleh}	br_ce_l pulse width	210	ns
T_{aveh}	Address setup to br_ce_l going high	50	ns
T_{dveh}	Data setup to br_ce_l going high	50	ns

Table 32. Expansion ROM Write Timing Specifications (Sheet 2 of 2)

Symbol[1]	Parameter	Minimum	Unit
T_{ehdx}	Data hold from br_ce_l going high	10	ns
T_{ehax}	Address hold from br_ce_l high	15	ns
T_{ads}	Address setup to latch enable high	10	ns
T_{adh}	Address hold from latch enable high	10	ns

NOTE:
1. There are no maximum specifications.

3.13 Serial ROM Timing Characteristics

Figure 17 shows the Serial ROM timing characteristics, and Table 33 lists the characteristics.

Figure 17. Serial ROM Port Timing Diagram

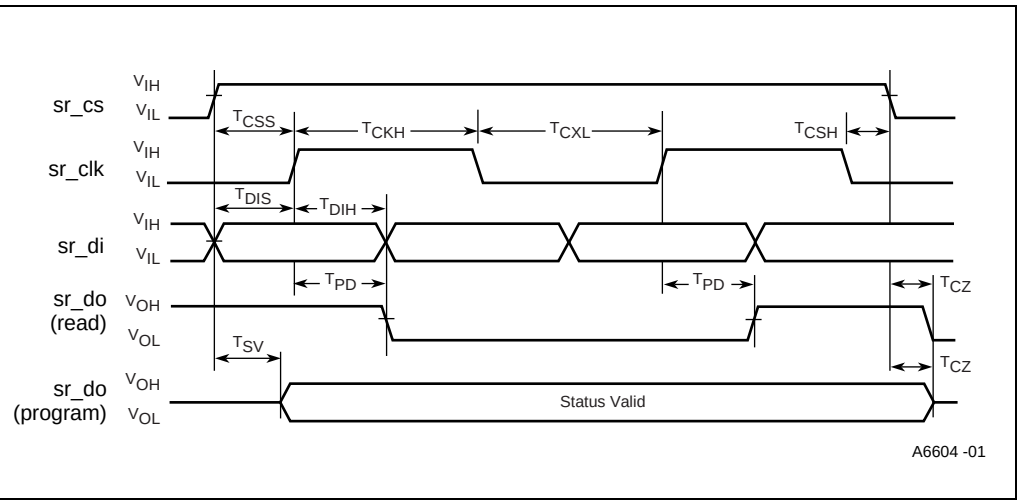


Table 33. Serial ROM Port Timing Characteristics

Symbol	Definition	Minimum	Maximum	Unit
T_{CKH}	Clock high time	350	—	ns
T_{CKL}	Clock low time	350	—	ns
T_{CSS}	Chip select setup time	150	—	ns
T_{CSH}	Chip select hold time	0	—	ns
T_{CSL}	Chip select low time	300	—	ns
T_{DIS}	Data input setup time	150	—	ns
T_{DIH}	Data input hold time	150	—	ns
T_{PD}	Data output delay time	—	550	ns
T_{CZ}	Data output disable time	—	150	ns

3.14 External Register Timing

Figure 18 shows the external register read timing characteristics, and Figure 19 shows the write timing characteristics. Table 34 lists the external register timing specifications for both read and write operations.

Figure 18. External Register Read Timing Diagram

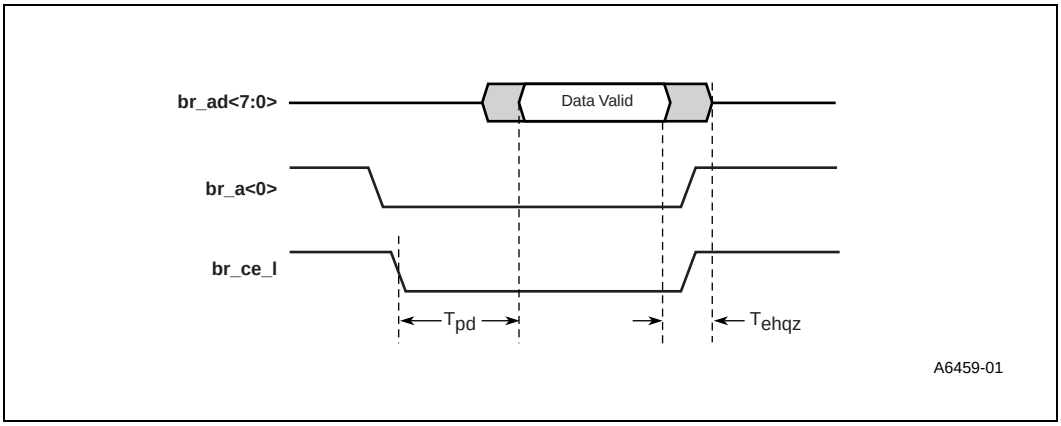


Figure 19. External Register Write Timing Diagram

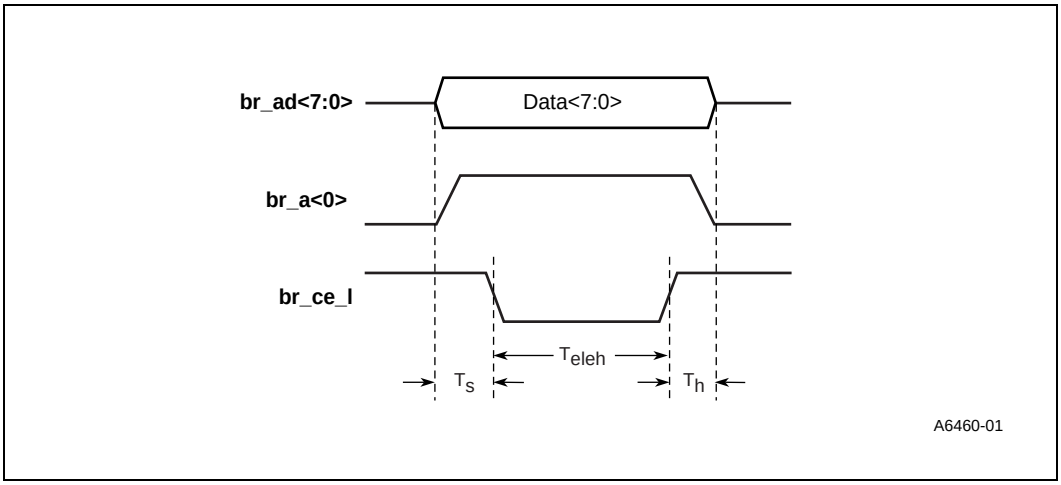


Table 34. External Register Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{eleh}	br_ce_l pulse width	240	—	ns
Read Timing				
T_{pd}	br_ce_l low to br_ad<7:0> valid high	—	20	ns
T_{ehqz}	br_ce_l high to br_ad<7:0> high impedance	—	20	ns
Write Timing				
T_s	Data setup time prior to br_ce_l	10	—	ns
T_h	Data hold after br_ce_l high	10	—	ns

3.15 Modem Electrical Parameters

This section describes the modem write and read characteristics for the 21145. For more information about the modem characteristics for the 21145, see the 2*1145 Phoneline/Ethernet LAN Controller Hardware Reference Manual*.

3.16 Write Access to Modem Chipset

Figure 20 and Table 35 describe a write access to the modem chipset. For more information about the sequence for a write access to the modem chipset, see the 2*1145 Phoneline/Ethernet LAN Controller Hardware Reference Manual*.

Figure 20. Write Access Timing

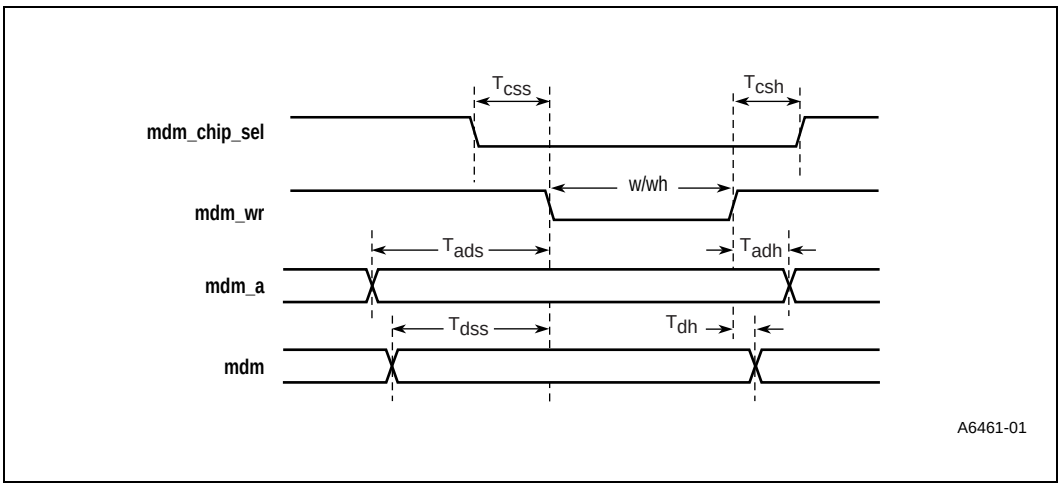


Table 35. Modem Write Access Timing Values

Symbol	Parameter	Minimum	Unit
T_{css}	Chip select set-up	15	ns
T_{ads}	Address set-up	45	ns
T_{adh}	Address hold	45	ns
W/wh	Write pulse width	100	ns
T_{dss}	Data set-up	45	ns
T_{dh}	Data hold	15	ns
T_{csh}	Chip select hold	15	ns

3.16.1 Read Access to Modem Chipset

Figure 21 and Table 36 describe a read access to the modem chipset. For more information about the sequence for a read access to the modem chipset, see the 2*1145 Phoneline/Ethernet LAN Controller Hardware Reference Manual*.

Figure 21. Read Access Timing

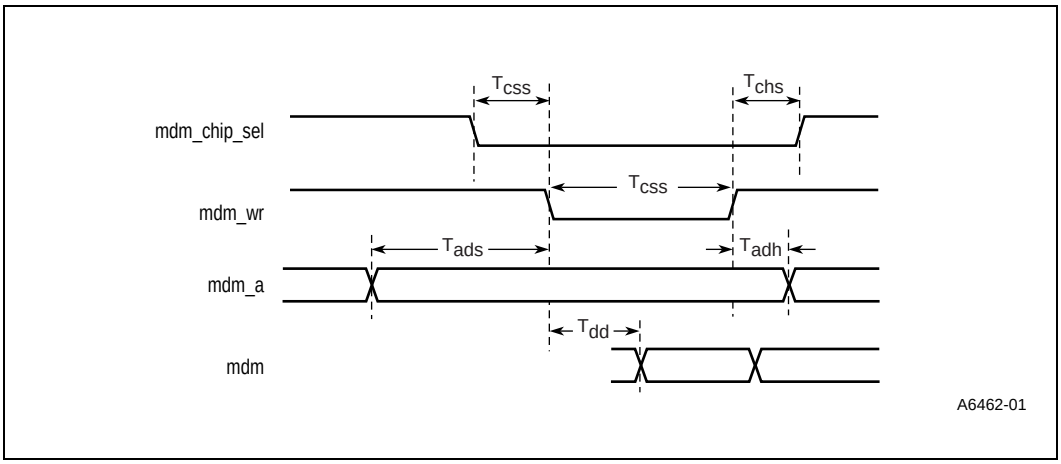


Table 36. Modem Read Access Timing Values

Symbol	Parameter	Minimum	Maximum	Unit
T_{css}	Chip select set-up	15	–	ns
T_{ads}	Address set-up	45	–	ns
T_{adh}	Address hold	45	–	ns
r/wh	Read pulse width	100	–	ns
T_{dd}	Data delay	–	90	ns
T_{dh}	Data hold	0	–	ns
T_{csh}	Chip select hold	15	–	ns

4.0 Mechanical Specifications

The 21145 is contained in a 176-pin TQFP package or a 144-pin TQFP package, as listed in Table 37. Figure 22 shows the package markings. Figure 23 shows the mechanical layout of the 176-pin package, and Figure 24 that of the 144-pin package. All measurements are in mm.

Table 37. 21145 Identifiers

Device Identifier	Stepping	Marketing Part Number	Order Code	Version	Status
DC1116	B0	21145	DE-NH978-AA	176TQFP	Production Parts, 176 pin
DC1116	B0	21145	DE-NH978-TA	144TQFP	Production parts, 144 pin

Figure 22. 21145 Package Marking

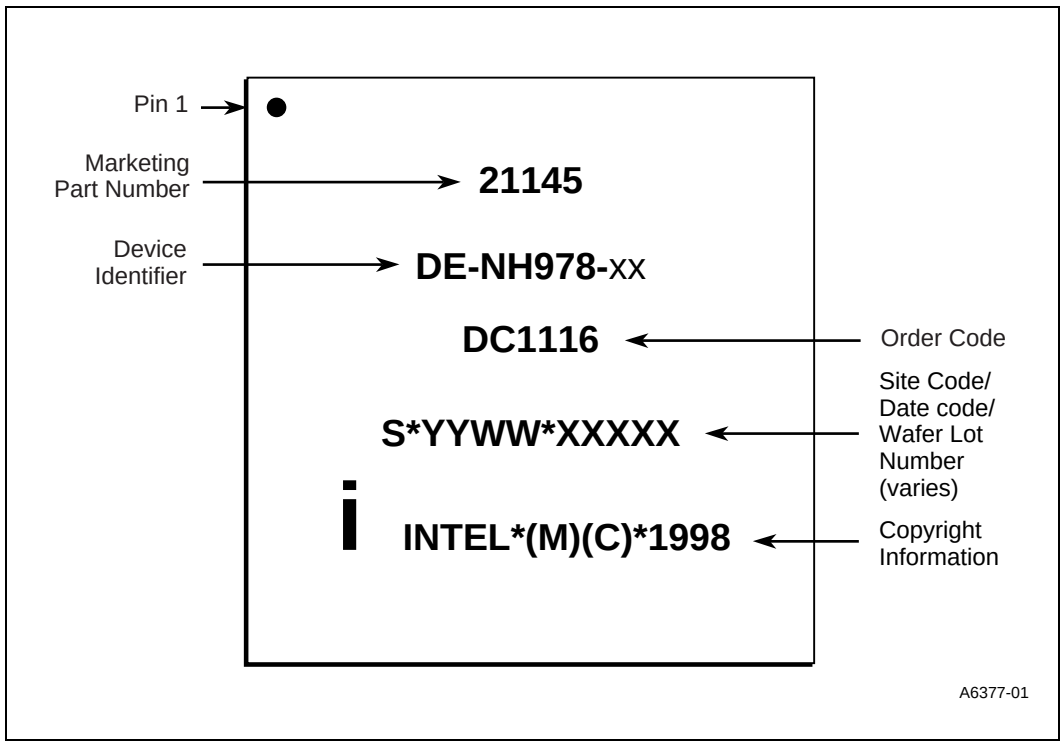


Figure 23. 176-Pin TQFP Package

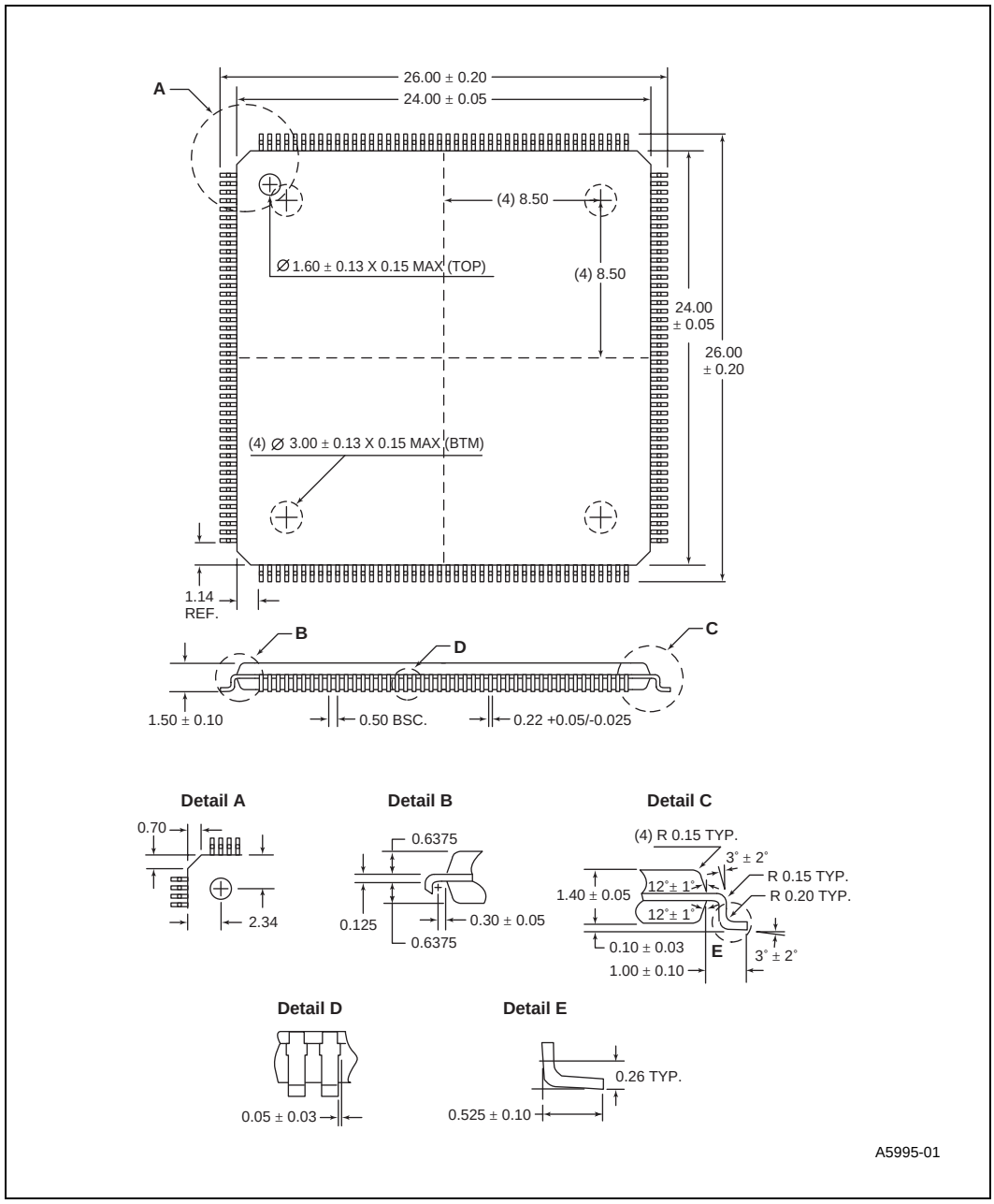


Figure 24. 144-Pin TQFP Package

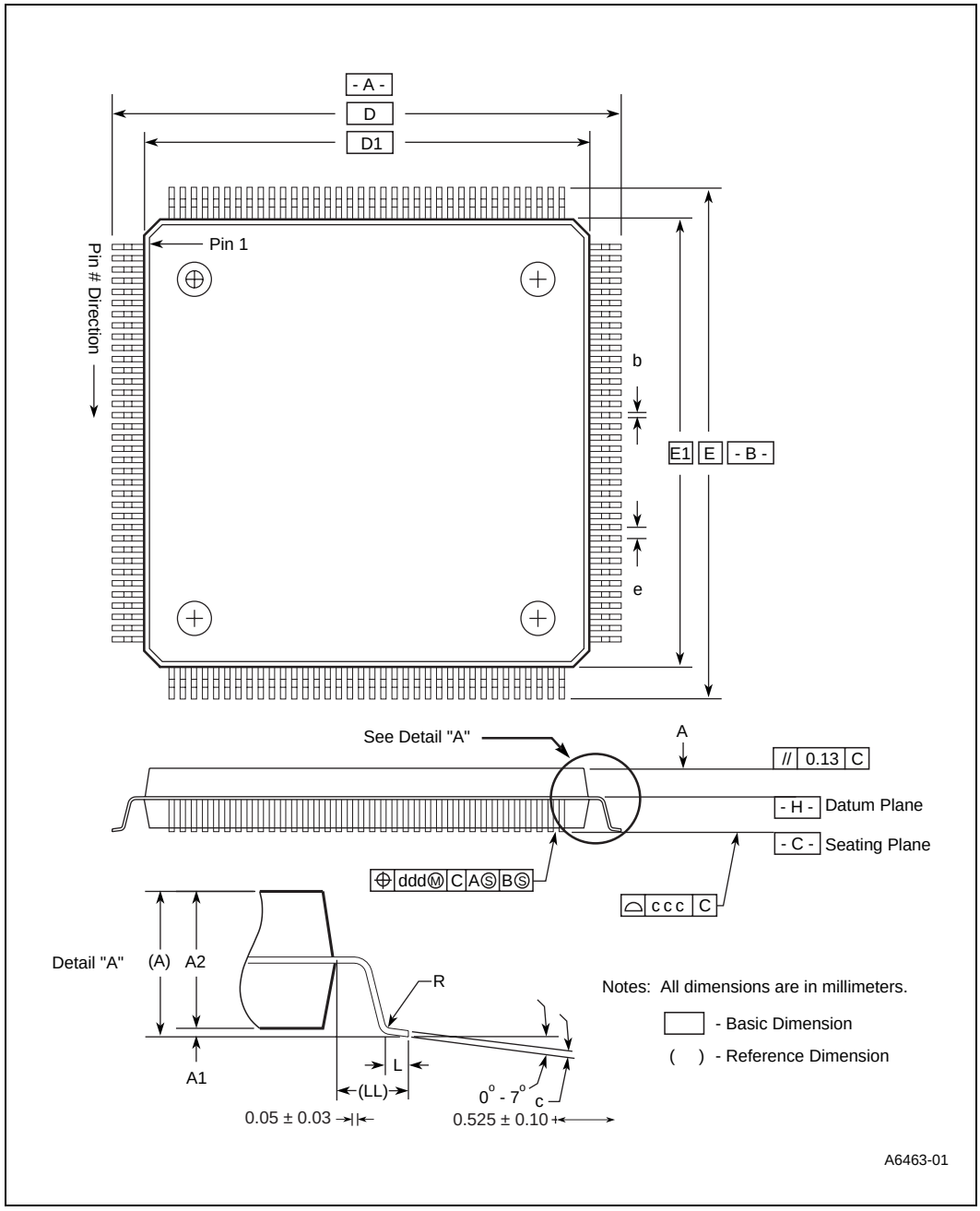


Table 38. 144-Pin LQFP Package Dimensions

Symbol	Dimension	Value (mm)
LL	Lead length	1.00 reference[1]
e	Lead pitch	0.50 BSC[2]
L	Foot length	0.45 minimum to 0.75 maximum
A	Package overall height	1.60 maximum
A1	Package standoff height	0.05 minimum
A2	Package thickness	1.35 minimum to 1.45 maximum
b	Lead width	0.17 minimum to 0.27 maximum
c	Lead thickness	0.09 minimum to 0.20 maximum
ccc	Coplanarity	0.08
ddd	Lead skew	0.08
D	Package overall width	22.00 BSC
D1	Package width	20.00 BSC
E	Package overall length	22.00 BSC
E1	Package length	20.00 BSC
R	Ankle radius	0.08 minimum to 0.20 maximum

1. The value for this measurement is for reference only.
2. ANSI Y14.5M–1982 American National Standard Dimensioning and Tolerancing, Section 1.3.2, defines Basic Dimension (BSC) as: A numerical value used to describe the theoretically exact size, profile, orientation, or location of a feature or datum target. It is the basis from which permissible variations are established by tolerances on other dimensions, in notes, or in feature control frames.

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