LS7266R1 Encoder to Microprocessor Interface Chip

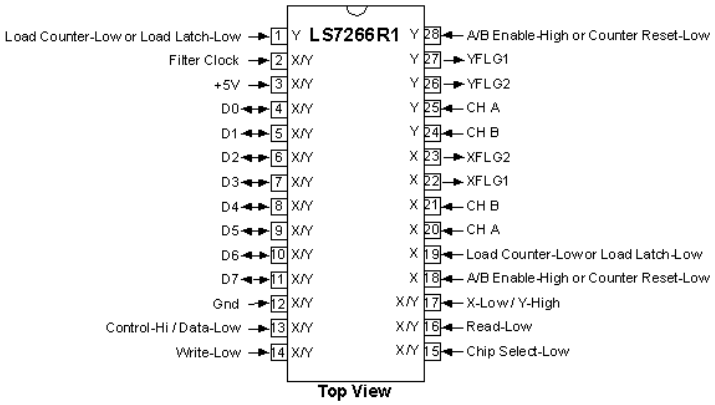
Description:

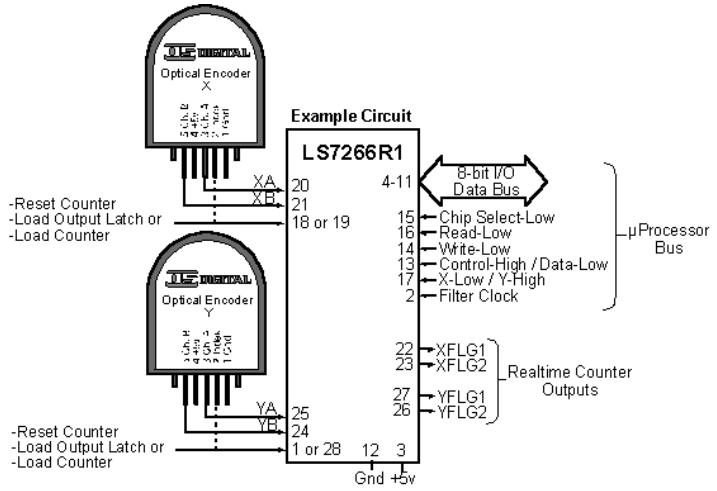
The **LS7266R1** is an LSI monolithic CMOS building block useful in motion control applications. The two 24-bit multimode counters, registers, and logic enables a microprocessor to track the speed, direction, position, and index of one or two optical incremental encoders. In addition to an 8-bit data bus, programmable real-time inputs and outputs are provided for hardware based control functions and status indication.

Note:
US Digital has already designed the IC's on this data sheet into various products. Please see the **PC7266**, **AD5** or **ED2**.

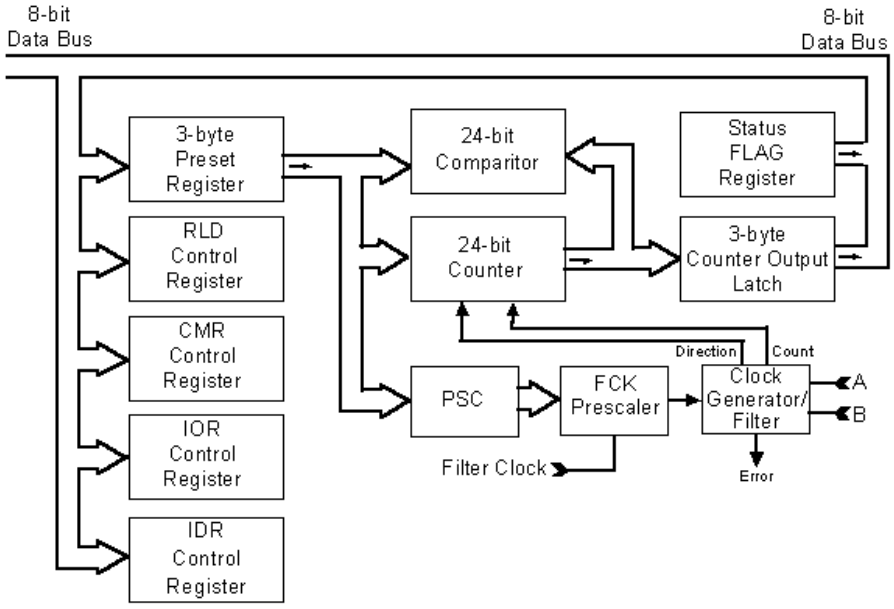
Features:

- X4 or X1 resolution multiplication.
- Two preloadable 24-bit Up/Down counters.
- Choice of two 20-pin packages: SOIC surface mount or DIP (600mil).
- X1 or X2 or X4 resolution multiplier.
- Binary, BCD, Divide-by-N, Range Limit, Non-Recycle & Non-quadrature Modes.
- 2-axis 24-Bit comparators.
- Independent mode programmability for each axis.
- 17 MHz in quadrature mode.
- 4 control registers.
- Readable status flag register.
- Digital filtering of the input quadrature clocks.
- Programmable 8-bit separate filter clock prescalers for each axis.
- Error flags for excess noise.
- 8-Bit tri-state I/O bus.
- Latched counter outputs.
- Input/Output TTL & CMOS compatible.
- 5 volt operation.





Block Diagram of Counter & Registers:



Ordering Information:

DIP Package (600mil):
LS7266R1-DIP

Surface Mount Package:
LS7266R1-SOIC

Price:
$16.55 / 1
$13.25 / 25
$10.60 / 100
$9.00 / 500
$7.65 / 1K

Technical Data, Rev. 11.21.00, November 2000

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Functional Descriptions:

The **LS7266** has two functionally equivalent halves, the X side and the Y side, selected by a dedicated input pin Xnot/Y (pin 17). Each half is a completely independent counting system. Within each counting system there is a data channel and a control channel, selected by a dedicated input addressing pin C/Dnot (pin 13). Reads of the data channel return one byte from the counting system output latch, and writes to the data channel store one byte in a preset latch. The 24-bit counter itself sits in between the preset latch and the output latch, and is not directly addressable. Instead, commands to the control channel of a counting system transfer data from the preset latch into the counter, or from the counter to the output latch. The preset latch and the output latch are also three bytes wide; it takes three successive reads or writes to transfer a full count to or from the data channel. There is a hidden byte pointer BP that controls which byte of the latches is being addressed via the data channel; this byte pointer cannot be directly written, but it can be reset via the control channel. BP auto-increments after every byte transfer to the data channel, and data is read out least-significant byte first.

The control channel has different behavior depending on whether it is being read or written. When read, the control channel always returns six bits of status information from the FLAG register. When writing to the control channel, data is sent to one of four different five-bit-wide control registers: reset/load decoder (RLD), counter mode register (CMR), input/output control register (IOR), and index control register (IDR). Bits D5 and D6 of the data determine which register is addressed; bit D7 is a special bit that forces the write to occur in both the X and Y counting systems when set. There is no provision for reading back the contents of any of the control channel write registers; the host software must keep a local copy of what was sent.

One final wrinkle involves the prescale counter register. To load this register, host software must first write a single byte to the lowest order byte of the preset latch; then the software must invoke a command to transfer data from this latch to the prescaler latch by writing a bit into the RLD register.

X & Y axis Inputs/Outputs:

XA (Pin 20) **XB** (Pin 21) **YA** (pin 25) **YB** (pin 24)	Either quadrature encoded clocks or non-quadrature clocks can be applied to A and B. In quadrature mode, A and B are digitally filtered and decoded for UP/DN clock. In non-quadrature mode, the filter and decoder circuits are bypassed. Also, in non-quadrature mode, A serves as the count input and B as the direction input, with B=1 selecting Up count and B=0 selecting down count mode. The quadrature code will be decoded and used to clock and steer the 24-bit counter. It can be programmed to generate one clock once per quadrature cycle, once per 1/2 cycle or once per 1/4 cycle (X1, X2 or X4 mode). Maximum count frequency is 17 MHz in quadrature mode, and 30 MHz in non-quadrature mode.
XLCNTR/XLOL (pin 19) **YLCNTR/YLOL** (pin 1)	Programmable input to operate either as direct load CNTR or direct load OL or synchronous load CNTR or synchronous load OL. The synchronous load mode is intended for interfacing with the encoder index output in quadrature clock mode. In direct load mode, a logic low level is the active level at this input. In synchronous load mode the active level can be programmed to be either a logic low or a logic high. Both quarter cycle and half cycle index signals are supported by this input in the indexed load mode. The synchronous function must be disabled in non-quadrature count mode.
XRCNTR/XABG (pin 18) **YRCNTR/YABG** (pin 28)	Programmable input to operate either as direct reset CNTR or count enable/disable gate or synchronous reset CNTR. The synchronous reset CNTR mode is intended for interfacing with the encoder index output in quadrature clock mode. The synchronous reset CNTR mode the active level can be programmed to be either a logic low or a logic high. In count enable/disable mode, a logic high at this input enables the counter and a logic low level disables the counter. Both quarter cycle and half cycle index signals are supported by this input in the indexed reset CNTR mode.
XFLG1 (pin 22) **YFLG1** (pin 27)	Programmable output to operate either as CARRY (Active low), or COMPARE (generated when PR = CNTR; Active low), or IDX (FLAG bit 6), or CARRY/BORROW (Active low).
XFLG2 (pin 23) **YFLG2** (pin 26)	Programmable output to operate as either BORROW (Active low), or U/D (FLAG bit 5), or E (FLAG bit 4).

Common Inputs/Outputs:

$\overline{WR}$ (pin 14)	**Write input:** Control/Data bytes are written at the trailing edge of low level pulse applied to this input.
$\overline{RD}$ (pin 16)	**Read input:** A low level applied to this input enables the FLAGs and OLs to be read on the data bus.
$\overline{CS}$ (pin 15)	**Chip select input:** A low level applied to this input enables the chip for Read and Write.
C/$\overline{D}$ (pin 13)	**Control/Data input:** This input selects between a control register or a data register for Read/Write. When low, a data register is selected. When high, a control register is selected.
D0-D7 (pins 4-11)	**Data bus input/output:** The 8-bit three-state data bus is the I/O port through which all data transfers take place between the LS7266 and the host processor.
FCK (pin 2)	**Filter clock input:** The FCK is divided down internally by two 8-bit programmable prescalers, one for each channel.
$\overline{X}$/Y (pin 17)	**X/Y select:** X/Y = 0 selects X-axis and X/Y = 1 selects the Y-axis. X/Y is overridden by D7 = 1 in control write mode(C/D = 1).
VDD (pin 3)	**+5VDC**
VSS (pin 12)	**GND**

Chip Access:

D7	D6	D5	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	X/$\overline{Y}$	$\overline{CS}$	Function
X	X	X	X	X	X	X	1	Disable Chip
0	0	0	1	1	⎍	0	0	Write to XRLD
0	0	0	1	1	⎍	1	0	Write to YRLD
1	0	0	1	1	⎍	X	0	Write to both XRLD and YRLD
0	0	1	1	1	⎍	0	0	Write to XCMR
0	0	1	1	1	⎍	1	0	Write to YCMR
1	0	1	1	1	⎍	X	0	Write to both XCMR and YCMR
0	1	0	1	1	⎍	0	0	Write to XIOR
0	1	0	1	1	⎍	1	0	Write to YIOR
1	1	0	1	1	⎍	X	0	Write to both XIOR and YIOR
0	1	1	1	1	⎍	0	0	Write to XIDR
0	1	1	1	1	⎍	1	0	Write to YIDR
1	1	1	1	1	⎍	X	0	Write to both XIDR and YIDR
X	X	X	0	1	⎍	0	0	Write to X Preset Register, increment Address Counter
X	X	X	0	1	⎍	1	0	Write to Y Preset Register, increment Address Counter
X	X	X	0	⎍	1	0	0	Read X Output Latch, increment Address Counter
X	X	X	0	⎍	1	1	0	Read Y Output Latch, increment Address Counter
X	X	X	1	⎍	1	0	0	Read X FLAG Register
X	X	X	1	⎍	1	1	0	Read Y FLAG Register

Writing to 1 of the 4 Control Registers: Set Control/Data high. Bits 5 and 6 are used as address bits to select one of the 4 registers. Bit 7 allows the data to apply to both X and Y registers and overrides X/Y input. Only bits 0-4 are stored.

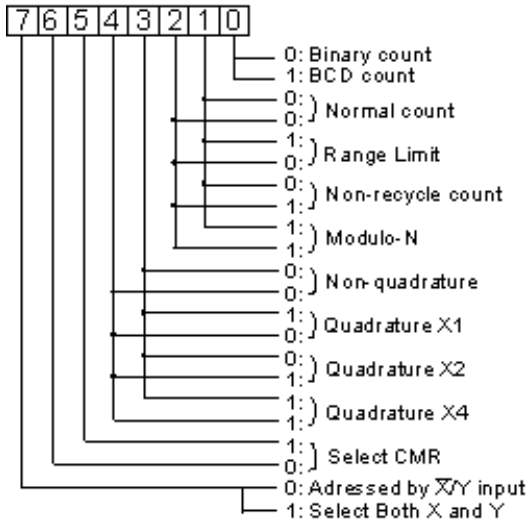
Notes:

1) D7 is the Most significant bit of the data bus.
2) X means "don't care".

Filter Clock Prescalers (XPSC & YPSC):

Each prescaler (PSC) is an 8-bit programmable modulo-N down counter, driven by the filter clock input (FCK). The factor N is loaded into a PSC, from the preset register (PR) byte 0, in the RLD register. This allows the ability to generate independent filter clock frequencies for each channel. Final filter clock frequency = (FCK / (PSC +1)).

Counter Mode Register (CMR):



Output Latch (Read Only, Data):

The 24-bit counter value at any instant can be accessed by transferring its contents to the 24-bit Output Latch. Note that only good stable data will be passed from the counter to the Output Latch even if the counter bits are in the midst of a transition. This chip will internally stretch the latch pulse if necessary until the counter has stabilized. The 3 bytes are then read from the Output Latch (least significant byte 1st). The byte pointer is automatically incremented with each read cycle. You must reset the byte pointer (BP) before making the first read.

Preset Register (Write Only, Data):

The 24-bit preset register is the input port for the 24-bit counter and the filter clock prescaler (PSC). The data is first written into the preset register in 3 write cycles (least significant byte 1st). The byte pointer is automatically incremented with each write cycle. You must reset the byte pointer (BP) before making the first write.

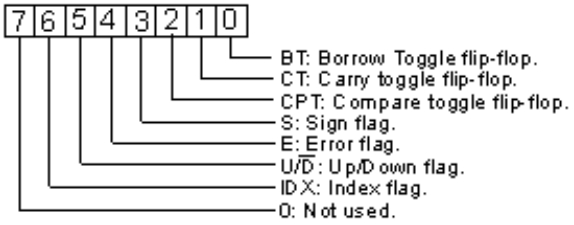
Range Limit: In range limit count mode, an upper and a lower limit is set, mimicking limit switches in the mechanical counterpart. The upper limit is set by the content of the PR and the lower limit is set to be 0. The CNTR freezes as CNTR = PR when counting up and at CNTR = 0 when counting down. At either of these limits, the counting is resumed only when the count direction is reversed.

Non-Recycle: In non-recycle count mode the CNTR is disabled, whenever a count overflow or underflow takes place. The end of cycle is marked by the generation of a Carry (in Up Count) or a borrow (in Down Count). The CNTR is re-enabled when a reset or load operation is performed on the CNTR.

Modulo-N: In modulo-N count mode, a count boundary is set between 0 and the content of the PR. When counting up, at CNTR = PR, the CNTR is reset to 0 and the up count is continued from that point. When counting down, at CNTR = 0, the CNTR is loaded with the content of PR and down count is continued from that point.

The modulo-N is true bidirectional in that the divide-by-N output frequency is generated in both up and down direction of counting for same N and does not require the complement of N in the UP instance. In frequency divider application the modulo-N output frequency can be obtained at either the compare (CY) or the BW output. Modulo-N output frequency fN= (fi/ (N+1)) where fi = Input count frequency and N = PR.

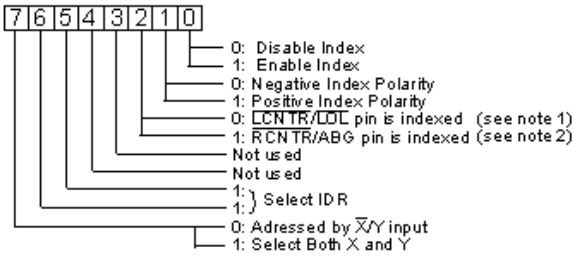
Status FLAG Register (Read only, control):



BT: Toggles every time CNTR underflows
CT: Toggles every time CNTR overflows
CPT: Toggles every time PR = CNTR
S: Reset to 0 when CNTR overflows
E: Set to 1 when excessive noise is present at the count inputs.
U/D̄: Set to 1 when counting up and reset to 0 when counting down.
IDX: Set to 1 when index is valid.

The FLAG registers hold the status information of the CNTRs and can be read out on the data bus when C\D = 1. E = 1 indicates excessive noise at the inputs but not a definite count error. Once set, E can only be reset via the RLD.

Index Control Register (IDR):

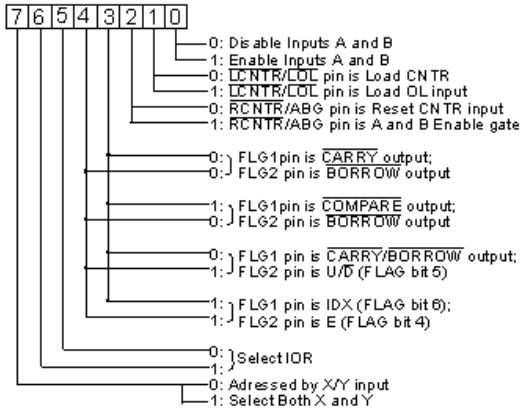


Note 1: LCNTR/LOL input must also be initialized as the Load CNTR or the Load OL input via the IOR register bit 1.

Note 2: RCNTR/ABG input must also be initialized as the reset CNTR input via the IOR register bit 2.

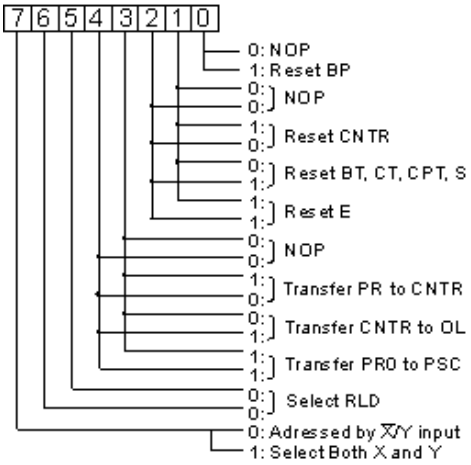
Either the LCNTR/LOL or the RCNTR/ABG inputs can be initialized to operate as an index input. When initialized as such, the index signal from the encoder, applied to one of these inputs performs either the Reset CNTR or the Load CNTR or the Load OL operation synchronously with the quadrature clocks. Note that only one of these inputs can be selected as the Index at a time and hence only one type of indexing function can be performed in any given setup. The index function must be disabled in non-quadrature count mode.

Input/Output Control Register (IOR):



Control functions may be combined. The toggle flip flops are triggered by the trailing edges of the associated Carry, Borrow, or Compare match. Thus there is a 1-clock delay between the input and output of each flip flop. Unless otherwise specified, assume the longest prop delay from any input to any output is <110ns.

Reset & Load Signal Decorders (RLD):



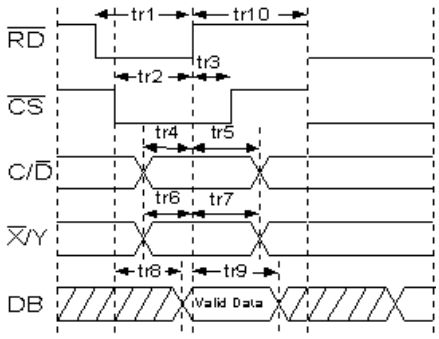
Absolute Maximum Ratings:

Parameter	Min.	Max.	Units
Voltage at any input	-.5	VCC+.5	Volts
Supply voltage (VCC)	-	7	Volts
Operating temperature	-25	80	℃
Storage temperature	-65	150	℃

DC Electrical Characteristics:

Parameter	Min.	Max.	Units	Notes
Supply voltage	4.5	5.5	Volts	
Supply current		800	µA	all clocks off
Input logic low		0.8	Volts	
Input logic high	2.0		Volts	
Output low voltage	0.5		Volts	IOutSink=5mA
Output high voltage	VCC-.5		Volts	IOutSource=1mA
Input leakage current		30	nA	
Output source current	1		mA	V_O = VCC-.5V
Output sink current	5		mA	V_O = 0.5V
Data bus leakage		60	nA	data bus off current

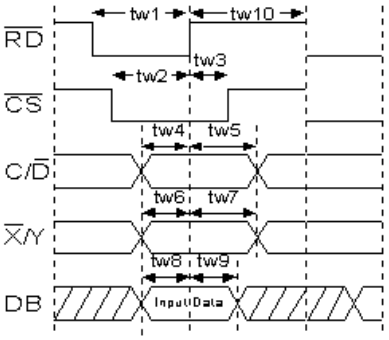
Read Cycle:



Read Cycle Timing: The data bus will become valid 50ns after asserting both Read and Chip Select. Release starts when either Read or Chip Select is terminated.

Parameter	Symbol	Min	Max	Unit
RD Pulse Width	tr1	50	-	ns
CS Setup Time	tr2	50	-	ns
CS Hold Time	tr3	0	-	ns
C/D Setup Time	tr4	50	-	ns
C/D Hold Time	tr5	0	-	ns
X/Y Setup Time	tr6	50	-	ns
X/Y Hold Time	tr7	0	-	ns
Data Bus Access Time	tr8	50	-	ns
Data Bus Release Time	tr9	-	25	ns
Back to Back Read Delay	tr10	60	-	ns

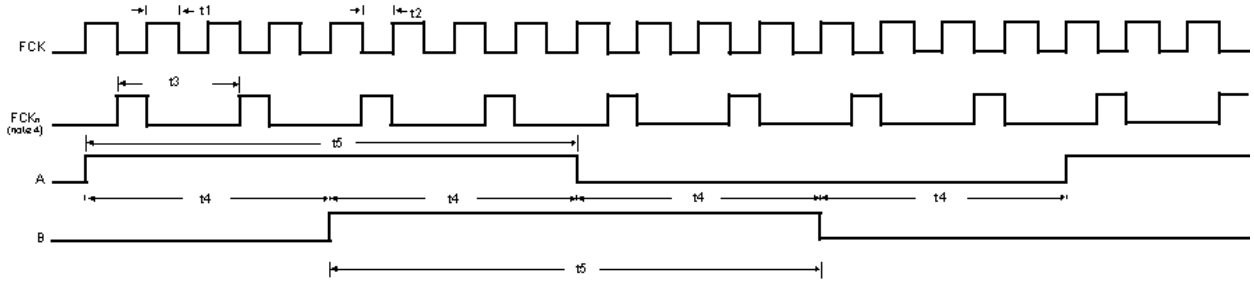
Write Cycle:



Write Cycle Timing: Allow at least 30ns setup time after asserting both Write and Chip Select for valid input data.

Parameter	Symbol	Min	Max	Unit
WR Pulse Width	tw1	30	-	ns
CS Setup Time	tw2	30	-	ns
CS Hold Time	tw3	0	-	ns
C/D Setup Time	tw4	30	-	ns
C/D Hold Time	tw5	0	-	ns
X/Y Setup Time	tw6	30	-	ns
X/Y Hold Time	tw7	0	-	ns
Data Bus Setup Time	tw8	30	-	ns
Data Bus Hold Time	tw9	0	-	ns
Back to Back Write Delay	tw10	60	-	ns

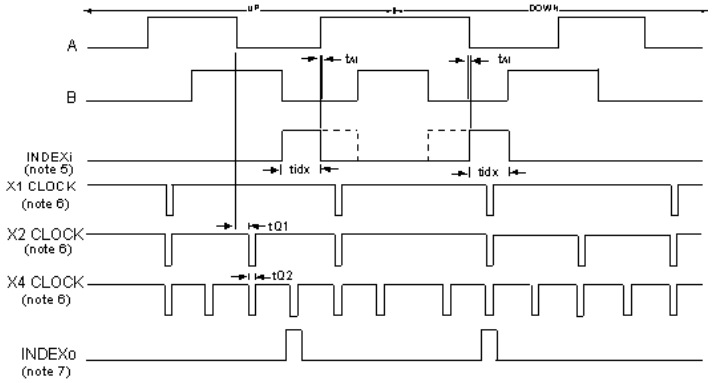
Filter Clock FCK & Quadrature Clocks A & B:



Note 4: FCKn is the final modulo-n internal filter clock, arbitrarily shown here as modulo-1.

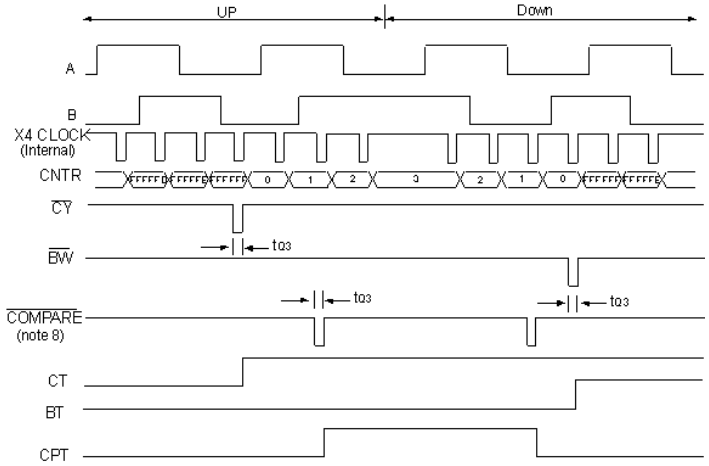
Parameter	Symbol	Min	Max	Unit	Remarks
FCK high pulse width	t1	14	-	ns	-
FCK low pulse width	t2	14	-	ns	-
FCK frequency	fFCK	-	35	MHz	-
Mod-n filter Clock (FCKn) period	t3	28	-	ns	t3 = (n+1)(t1+t2), where N = PSC = 0 to FF(Hex)
FCKn frequency	fFCKn	-	35	MHz	-
Quadrature separation	t4	57	-	ns	-
Quadrature clock pulse width	t5	115	-	ns	-
Quadrature clock frequency	fQA, fQB	-	4.3	MHz	fQA = fQB = 1/8t3

Quadrature Clock A, B & Index Input:



Note 5 : Shown here is positive index with solid line depicting 1/4 cycle index and dotted line depicting 1/2 cycle index. Either $\overline{\text{LCNTR}}$/$\overline{\text{LOL}}$ or $\overline{\text{RCNTR}}$/ABG input can be used as the INDEX input.
Note 6 : X1, X2 and X4 clocks are the final internal Up/Down count clocks derived from filtered and decoded Quadrature Clock inputs, A and B.
Note 7 : INDEX0 is the synchronized internal "load OL" or "reset CNTR" signal based on $\overline{\text{LCNTR}}$/$\overline{\text{LOL}}$ or $\overline{\text{RCNTR}}$/ABG input being selected as the INDEX input, respectively.

Carry, Borrow, Compare:



Note 8 : COMPARE is generated when PR = CNTR. In this timing diagram it is arbitrarily assumed that PR = 1.

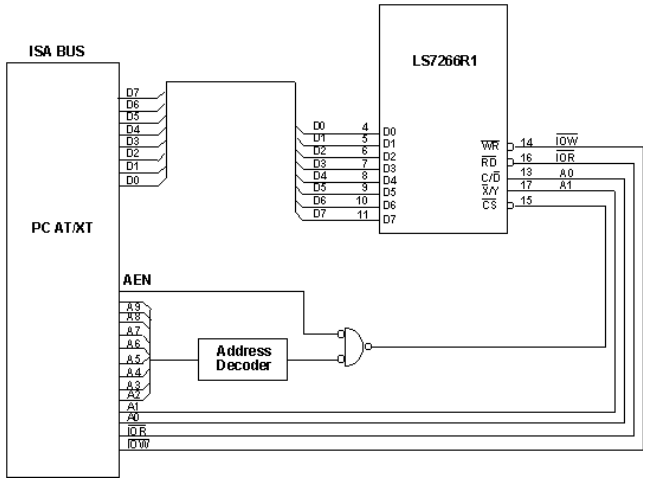
Quadrature Clock A, B & Index Input Specifications:

Parameter	Symbol	Min	Max	Unit	Remarks
Quadrature Clock to Count Delay	tQ1	5t3	6t3	-	-
X1/X2/X4 Count Clock Pulse Width	tQ2	28	-	ns	tQ2=t3
Index Input Pulse Width	tidx	85	-	ns	tidx >= 3t3
Index Skew from A	tAi	-	28	ns	tAi <= t3

Carry, Borrow, Compare Specifications:

Parameter	Symbol	Min	Max	Unit	Remarks
Carry/Borrow/Compare/Output Width	tQ3	28	-	ns	tQ3 = t3

LS7266R1 Interface Example A:



LS7266R1 Interface Example B: