COS/MOS INTEGRATED CIRCUIT

4508 B

HCC/HCF 4508B

DUAL 4-BIT LATCH

- TWO INDIPENDENT 4-BIT LATCHES
- INDIVIDUAL MASTER RESET FOR EACH 4-BIT-LATCH
- 3-STATE OUTPUTS WITH HIGH-IMPEDANCE STATE FOR BUS LINE APPLICATION
- MEDIUM-SPEED OPERATION: $t_{PHL} = t_{PLH} = 70$ ns (TYP.) AT $V_{DD} = 10V$ AND $C_L = 50$ pF
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4508B** (extended temperature range) and the **HCF 4508B** (intermediate temperature range) are monolithic integrated circuits available in 24–lead dual in–line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4508B** dual 4–bit latch contains two identical 4–bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high–impedance state for bus line applications by a high level on the DISABLE input.

ABSOLUTE MAXIMUM RATINGS

V_{DD} *	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

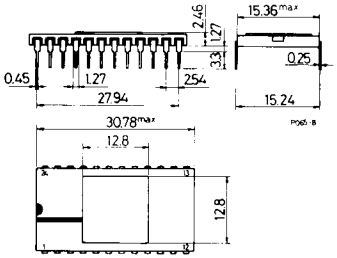
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

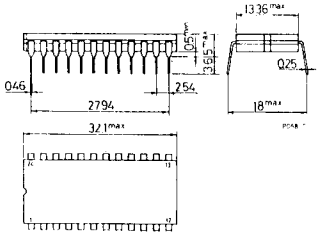
HCC 4508 BD for dual in–line ceramic package
HCC 4508 BF for dual in–line ceramic frit seal package
HCC 4508 BK for ceramic flat package
HCF 4508 BF for dual in–line ceramic frit seal package
HCF 4508 BE for dual in–line plastic package

MECHANICAL DATA (dimensions in mm)

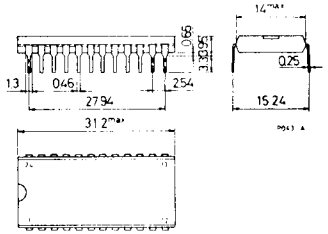
Dual in-line ceramic package for HCC 4508 BD



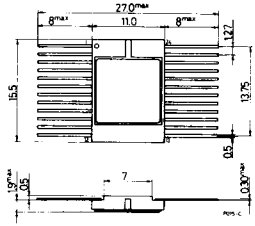
Dual in-line ceramic frit seal package for HCC/HCF 4508 BF



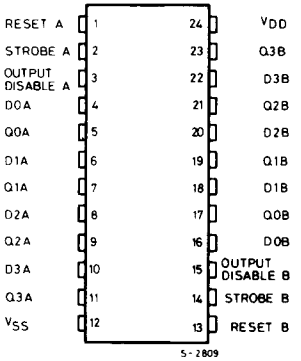
Dual in-line plastic package for HCF 4508 BE



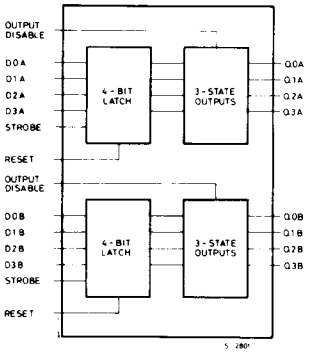
Ceramic flat package for HCC 4508 BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

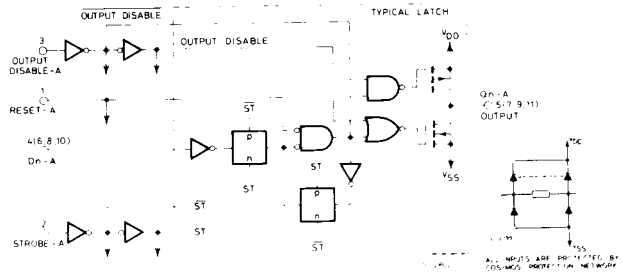


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAM (A Section)

1 of 4 identical latches with common output disable, reset and strobe



TRUTH TABLE

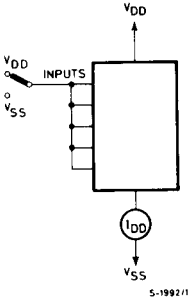
RESET	DISAB	STROBE	D INPUT	Q INPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	Latched
1	0	X	X	0
X	1	X	X	Z

1 = High level
0 = Low level

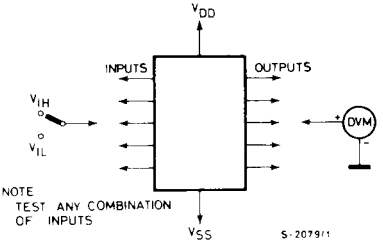
X = Dont' care
Z = High impedance

TEST CIRCUITS

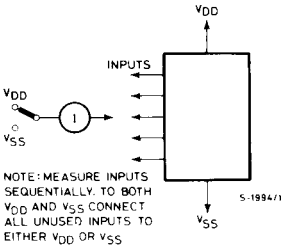
Quiescent device current test circuit



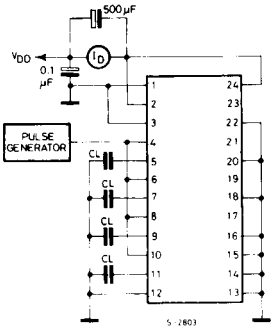
Input voltage test circuit



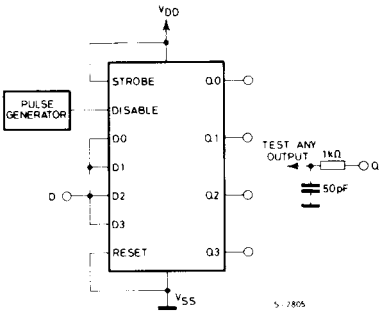
Input current test circuit



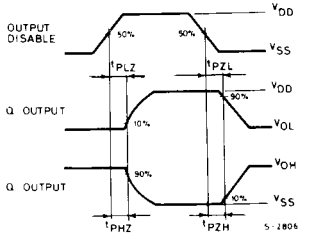
Power dissipation test circuit



Output disable



Waveform



CHAR.	TEST. AT D	VOLT. AT Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

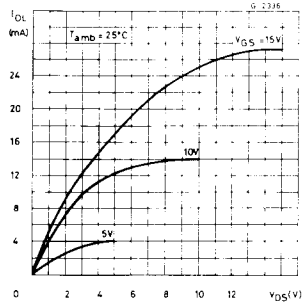
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		± 1	
I_O	3-state output	HCC types	0/18			18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		HCF types	0/15			15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

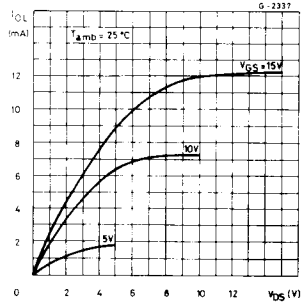
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, unless otherwise specified)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{THL}, t_{TLH} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	
$t_{W(R)}$ Reset pulse width		5	200	100		ns
		10	140	70		
		15	100	50		
$t_{W(st)}$ Strobe pulse width		5	140	70		ns
		10	80	40		
		15	70	35		
t_{setup} Setup time		5	50	25		ns
		10	30	15		
		15	20	10		
t_H Hold time		5	0	0		ns
		10	0	0		
		15	0	0		
t_{PHL}, t_{PLH} Propagation delay times:	Strobe to data out	5		130	260	ns
		10		70	140	
		15		50	100	
	Data in to data out	5		105	210	ns
		10		60	120	
		15		45	90	
	Reset to data out	5		90	180	ns
		10		50	100	
		15		40	80	
t_{PHZ} 3-state propagation delay times: output high to high impedance		5		90	180	ns
		10		50	100	
		15		35	70	
t_{PZH} High impedance to output high		5		90	180	ns
		10		50	100	
		15		35	70	
t_{PLZ} Output low to high impedance		5		90	180	ns
		10		50	100	
		15		35	70	
t_{PZL} High impedance to output low		5		90	180	ns
		10		50	100	
		15		35	70	

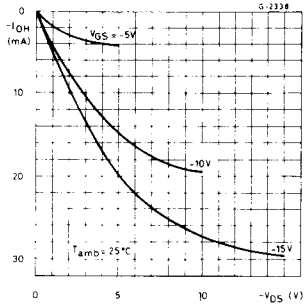
Typical output low (sink) current characteristics



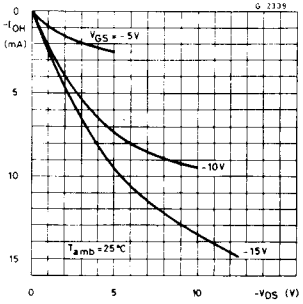
Minimum output low (sink) current characteristics



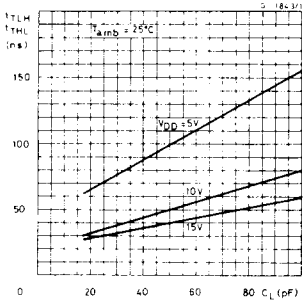
Typical output high (source) current characteristics



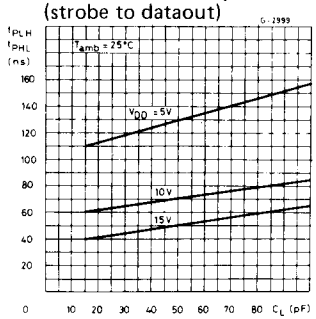
Minimum output high (source) current characteristics



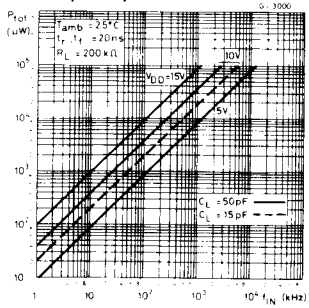
Typical transition time vs. load capacitance



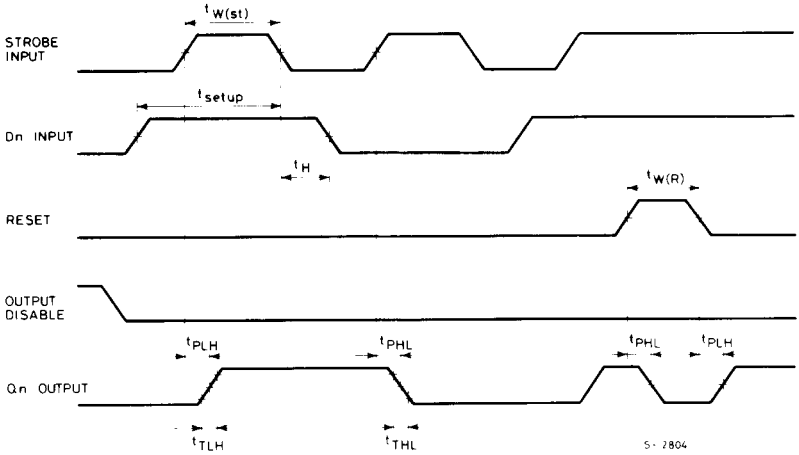
Typical propagation delay time vs. load capacitance (strobe to dataout)



Typical power dissipation vs. frequency

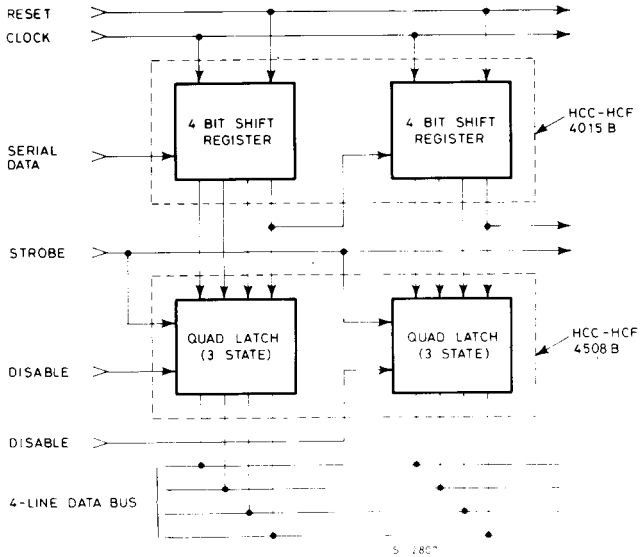


TEST WAVEFORM



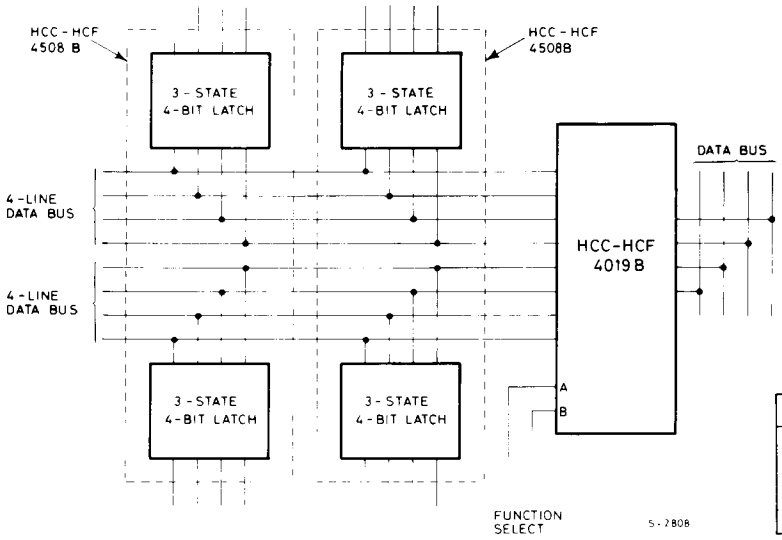
TYPICAL APPLICATIONS

A) Fig. 15 - Bus register

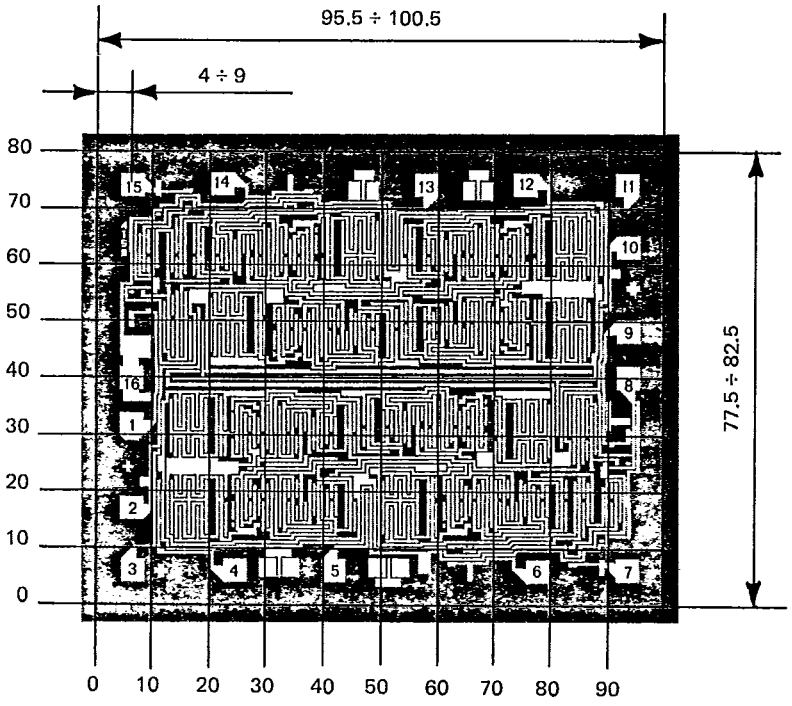


TYPICAL APPLICATIONS (continued)

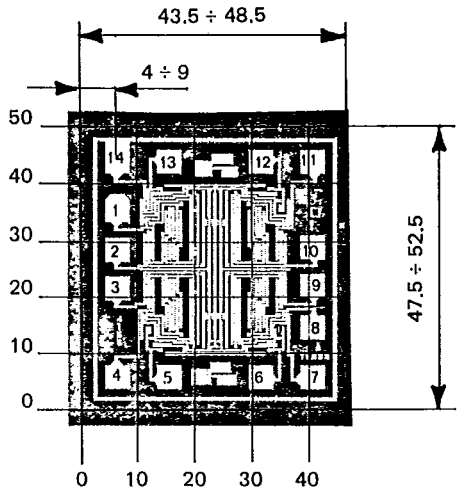
B) Fig. 16 - Dual multiplexed bus register with function select



A	B	FUNCTION
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	$A_1 + B_1$


95.5 ÷ 100.5
4 ÷ 9
77.5 ÷ 82.5
80
70
60
50
40
30
20
10
0
0 10 20 30 40 50 60 70 80 90
15 14 13 12 11 10 9 8 16 1 2 3 4 5 6 7

4015B


43.5 ÷ 48.5
4 ÷ 9
47.5 ÷ 52.5
50
40
30
20
10
0
0 10 20 30 40
14 13 12 11 1 2 3 10 9 8 4 5 6 7

4016B