CIRRUS LOGIC®

CL-MD34XX

Data Book

FEATURES

- **Complete PC telephony solution**
  - Up to 33.6-kbps data rates
  - Highly integrated three- or four-chip set
  - Controller-based robust platform
  - Exceeds Microsoft® PC 95 requirements
  - Full-duplex, echo-cancelled digital speakerphone
  - ITU-V.70 DSVD (digital simultaneous voice and data) upgrade option
  - ITU-V.80 videoconferencing
  - International telephony support
- **Data modulation**
  - ITU-T V.34 (33,600 to 2400 bps) symmetric and asymmetric operation
  - ITU-T V.32 bis, V.23, V.22 bis, V.21
  - Bell® 212A and 103
- **Fax modulation**
  - ITU-T V.17, V.29 to 14,400 bps
- **Voice telephony**
  - Full-duplex, echo-cancelled digital speakerphone
  - Radish® VoiceView™ upgrade option
  - Telephone emulation for headset applications
  - Microsoft® Windows® TAPI-compliant
  - ITU-V.70 DSVD upgrade option
  - ITU-V.80 for videophone
- **Voice coder**
  - Voice compression: ADPCM, linear, and CL1
  - 4800, 7200, 8000, 9600, and 11025 samples per second

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V.34+ FastPath™ 33.6-kbps Data/Fax/Voice Chipset Family

OVERVIEW

The V.34+ FastPath™ chipset family is an ideal solution for today's PC telephony applications, and it is a robust platform that will support future communication standards. With a complete complement of industry-standard features for data, fax, and voice applications, the V.34+ family satisfies internal, standalone, and PC Card applications, plus advanced features such as 33.6-kbps modulation speeds and DSVD.

Integrated, Open Architecture

The FastPath platform owes its capabilities to the sophisticated architecture of its controller and DSP (digital signal processor). Each component's highly integrated design minimizes part count and board area. The single-platform design means that no additional circuitry is needed for features including DSVD, speakerphone, PC Card, serial inter-

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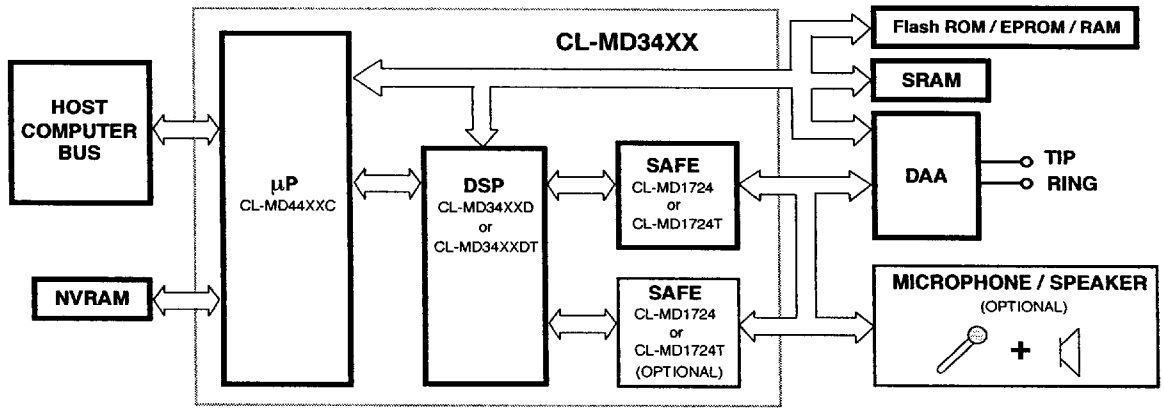
System Block Diagram



Version 1.1

February 1997

FEATURES (cont.)

- **Data link layer protocols**
  - Error correction: ITU V.42 and MNP® 2–4
  - Data compression: ITU V.42 bis and MNP® 5
- **DTE integrated interface alternatives**
  - Serial RS-232/V.24 interface
  - ISA bus direct or plug-and-play
  - PCMCIA bus interface
- **Controller functionality**
  - Industry-standard AT command driven
  - Fax Class 1 commands
  - Voice IS-101 commands
- **Minimal-component design**
  - Direct connection to ISA bus
  - Single crystal
  - Passive hybrid
- **Low power requirements**
  - Single +5-V power source; 3.3-V DSP option
  - Automatic sleep and wake-up modes
- **Small package options**
  - Controller and DSP: 128-pin SQFP or VQFP packages
  - SAFE: 44-pin VQFP package

OVERVIEW (cont.)

face, and ISA plug-and-play compatibility. The single platform serves all levels of product, from basic feature sets to full-featured DSVD/speakerphone applications. The V.34+ family exceeds Microsoft® PC 95 specifications for Windows® and legacy applications.

Satisfies Legacy Applications

The FastPath™ platform supports all requirements for PC-based communications, whether for internal, standalone, or PC Card applications. With its robust controller and powerful DSP, the V.34+ supports even the most demanding DOS gaming applications. The CL-MD34XX supports all industry-standard AT commands for data, IS-101 voice, and Class 1 fax.

Comprehensive Telephony Features

Voice telephony is becoming increasingly important in modem-based products. This chipset family offers a complete telephony interface with features such as Caller ID, voice mail, and answering machine capabilities that include call progress detection and tone generation.

For more advanced voice features, the V.34+ platform adds telephone emulation for headset applications and a Radish® VoiceView™ upgrade option for alternate transfers of voice and data over the same connection. The DSVD upgrade option enables data transfer in realtime during a voice conversation, an essential for whiteboard applications and sophisticated customer support. Additionally, the CL-MD34XX's full-duplex, echo-cancelled digital speakerphone offers the latest technology for hands-free computer telephony. The speakerphone operates in all modes, including DSVD. All voice features are fully compliant with Microsoft's Unimodem-V and TAPI standards, and all commands comply with IS-101 voice command standards.

International Telephony Support

V.34+ chipsets support international applications for PC Card, ISA, and serial bus designs. Cirrus Logic's configuration utility modifies the chipset firmware to comply with international standards. Cirrus Logic also provides international DAA design recommendations.

Platform of the Future

The FastPath™ family is a solid base for future innovation. The controller's embedded RISC processor uses a unique caching architecture that enables the use of lower-cost memory chips. The controller code is open for modification in a C code development environment. A Flash memory interface and configuration utility allow downloading of code and customization of features.

The DSP delivers the bandwidth to handle multiple tasks simultaneously and to support specialized functions. Many advanced features are already built in, including a full-duplex, echo-cancelled speakerphone and a DSVD vocoder. Concurrent operation is enabled for even the most advanced features, such as speakerphone operation in DSVD mode. Other built-in features are call progress and tone generation, including DTMF, CNG, and Caller ID. Tones can be tailored to special requirements.

REVISION HISTORY

Version 1.1 February 1997

Following are the major changes made since version 1.0:

Features/Overview

Radish® VoiceView™ is optional.

Added ITU-V.80 for videoconferencing.

Chapter 1

Section 1.1 on page 12: The DSP chip CL-MD3661DT was replaced with the CL-MD3660DT in all CL-MD34XX chipsets.

Chapter 3

Section 3.18 on page 20: A Cirrus Logic firmware downloading utility is now available.

Chapter 4

Section 4.4 on page 23: The NVRAM is never optional.

Section 6.1.1 on page 41: The following pins on the parallel and plug-and play µP (128-pin SQFP) pinout were changed:

- Pin 57: CS3* - An I/O pin, not an output pin
- Pin 59: HOSTSEL1, not HOSTEL1
- Pin 110: Removed INTA1. The INTA1 signal is no longer incorporated in the V.34+ chipsets.
- Pin 111: Removed INTA0. The INTA0 signal is no longer incorporated in the V.34+ chipsets.
- Pin 119: GND, not GGND.

Chapter 6

Section 6.1.2 on page 42: The following pins on the serial µP (128-pin SQFP) were changed:

- Pin 57: CS3* - An I/O pin, not an output pin
- Pin 59: HOSTSEL1, not HOSTEL1
- Pins 61–63, 65: These no-connect pins have no direction.
- Pin 110: Removed INTA1; changed to I/O from in.
- Pin 111: Removed INTA0
- Pin 119: Changed GGND to GND

Section 6.1.3 on page 43: The following pins on the PC Card µP (128-pin VQFP) were changed:

- Pin 53: CS3* - An I/O pin, not an output pin
- Pins 86–89, 91: HA4–7, HA8: These host address pins are all inputs, not I/Os.
- Pin 106: Removed INTA1
- Pin 107: Removed INTA0
- Pin 115: Changed GGND to GND

Section 6.2.1 on page 44: The following pins on the DSP's 128-pin SQFP pinout were changed:

- Pin 125: CLKOUT, not CLKOUT*
- Pin 124: IFTCH, not IFTCH*
- Pin 123: IACK, not IACK*
- Pin 122: DSPCFG, not DSPCFG*

Section 6.2.2 on page 45: The following pins on the DSP's 128-pin VQFP pinout were changed:

- Pin 62: STOP was changed from an output to an input
- Pin 122: CLKOUT, not CLKOUT*
- Pin 121: IFTCH, not IFTCH*
- Pin 120: IACK, not IACK*
- Pin 119: DSPCFG, not DSPCFG*

Chapter 7

Table 7-1 on page 47: HCS*/CACK* are no-connect for parallel and plug-and-play modes with internal address decode.

page 64: Changed connection instructions for CS2*.

page 66: Changed descriptions of EPGMRD*, EPGMWR*, and DSPCFG.

Section 7.1.1.2 on page 51: Changed reserved pin 84 to be connected to V_{cc} through a 47-kΩ resistor.

page 69: Changed descriptions of TXEN1 and TXEN2, TXSTR1* and TXSTR2*, and RXSTR1* and RXSTR2*.

page 64: The CS2* pin can be connected to either V_{CC} or GND through a 10-K or larger resistor, not only a 47-K resistor.

Chapter 8

Figure 8-2 on page 78: Changed t_8 interval.

Table 8-5 on page 79: Changed former t_7 to t_6; eliminated old t_6.

Table 8-6 on page 80: Changed former t_7 to t_6; eliminated old t_6.

Figure 8-12 on page 90: Added note about WAIT*.

Table 8-18 on page 95: Changed description and values for t_2.

Table 8-19 on page 97: Changed values for t_2.

Table 8-21 on page 99: Changed values for t_3.

Chapter 9

Section 9.3 on page 103: new VQFP 44-pin package.

Chapter 10

page 105: Changed the DSP's chip number in the CL-MD3463T chipset to CL-3660DT from CL-3661DT.

Version 1.0 September 1996

Following are the major changes made since version 0.9:

Chapters 6 and 7

Renamed all µP and DSP power and ground pins as simply V_{CC} and GND. Removed individually named pins from the µP and DSP pin descriptions.

Section 7.1.1.3 on page 52: Added power and ground pins for the µP's parallel/plug-and-play and serial interfaces.

Section 7.1.1.5 on page 55: Added power and ground pins for the µP's PC Card (PCMCIA) interface.

Section 7.2.5 on page 69: Added power and ground pins for the DSP's SQFP and VQFP packages.

Version 0.9 August 1996

Following are the major changes made since version 0.8:

Chapter 5

Table 5-5: Changed range for the **+VNH** command.

Table 5-7: Changed the hex code for the '~' response in the DCE → DTE voice character pairs table.

Table 5-14: Added the **-Tn** manufacturing command.

Chapter 6

Section 6.1.2: Changed pin 97, 'XTC', to 'Reserved'.

Chapter 7

Table 7-1: Changed serial values for HCS*/CACK*, COMSEL[0–1], AEN, and HA[0–9].

Section 7.1.1.1: Changed pin connection information for the parallel/plug-and-play pins HCS*/CACK* and TCS*.

Section 7.1.1.2: Changed the pin connection information for the serial pins HOSTSEL1/CS5*, HOSTSEL0/CS4*, reserved pins, and TCS*.

Section 7.1.1.4: Changed the pin connection information for the PC Card (PCMCIA) pins CS5*, CS4*, and TCS*.

Section 7.1.1.2: Changed the description for pin 97, formerly 'XTC', now 'Reserved.'

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APPENDIXES

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LIST OF FIGURES

CONVENTIONS

This section lists conventions used in this data book.

Abbreviations

Symbol	Units of measure
°C	degree Celsius
µF	microfarad
µs	microsecond (1,000 nanoseconds)
Hz	hertz (cycle per second)
K (memory)	kilobit (1,024 bits)
kbits/second	kilobit (1,000 bits) per second
kHz	kilohertz
kΩ	kilohm
Mbyte (memory)	megabyte (1,048,576 bytes)
MHz	megahertz (1,000 kilohertz)
mA	milliampere
ms	millisecond (1,000 microseconds)
ns	nanosecond
pV	picovolt
V	volt
W	watt

Acronyms

Acronym	Definition
AC	alternating current
AT	'Attention' command prefix for Hayes AT® command set (for example, 'ATDT 123')
CMOS	complementary metal-oxide semiconductor
DC	direct current
DAA	data access arrangement
DRAM	dynamic random-access memory
DSVD	digital simultaneous voice and data
EPROM	electrically programmable read-only memory
FIFO	first in/first out
HDLC	high-level data link control
ISA	industry-standard architecture
LSB	least-significant bit
MSB	most-significant bit
NVRAM	non-volatile random-access memory
RAM	random-access memory
ROM	read-only memory
R/W	read/write
SQFP	shrink quad flat pack
SRAM	static random-access memory
TTL	transistor-transistor logic
UART	universal asynchronous receiver transmitter
VQFP	very-tight-pitch quad flat pack

1. AVAILABLE CHIPSETS

Market	Parallel/Serial Host Interface	PC Card Host Interface
Data/fax voice	**CL-MD3450** µP: CL-MD4450C DSP: CL-MD3450D SAFE: CL-MD1724	**CL-MD3451T** µP: CL-MD4451C DSP: CL-MD3451DT SAFE: CL-MD1724T
Data/fax voice, full-duplex speaker-phone	**CL-MD3452** µP: CL-MD4450C DSP: CL-MD3450D SAFE: CL-MD1724 SAFE: CL-MD1724	**CL-MD3453T** µP: CL-MD4451C DSP: CL-MD3451DT SAFE: CL-MD1724T SAFE: CL-MD1724T
Data/fax voice, full-duplex speaker-phone, DSVD	**CL-MD3462T** µP: CL-MD4450C DSP: CL-MD3460DT SAFE: CL-MD1724T SAFE: CL-MD1724T	**CL-MD3463T** µP: CL-MD4451C DSP: CL-MD3460DT SAFE: CL-MD1724T SAFE: CL-MD1724T

Figure 1-1. CL-MD34XX Family Chipset Composition

1.1 Functional Block Diagrams

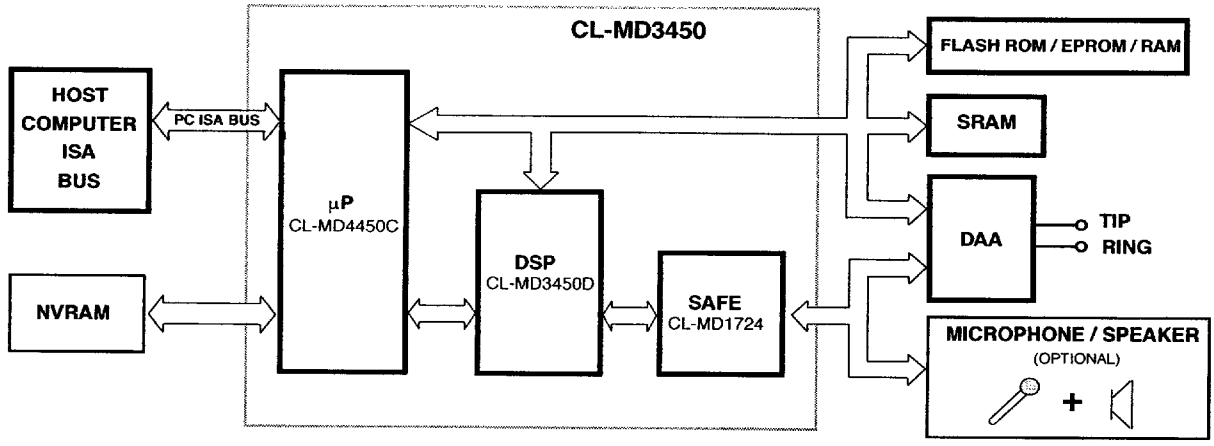

Figure 1-2. CL-MD3450 Functional Block Diagram

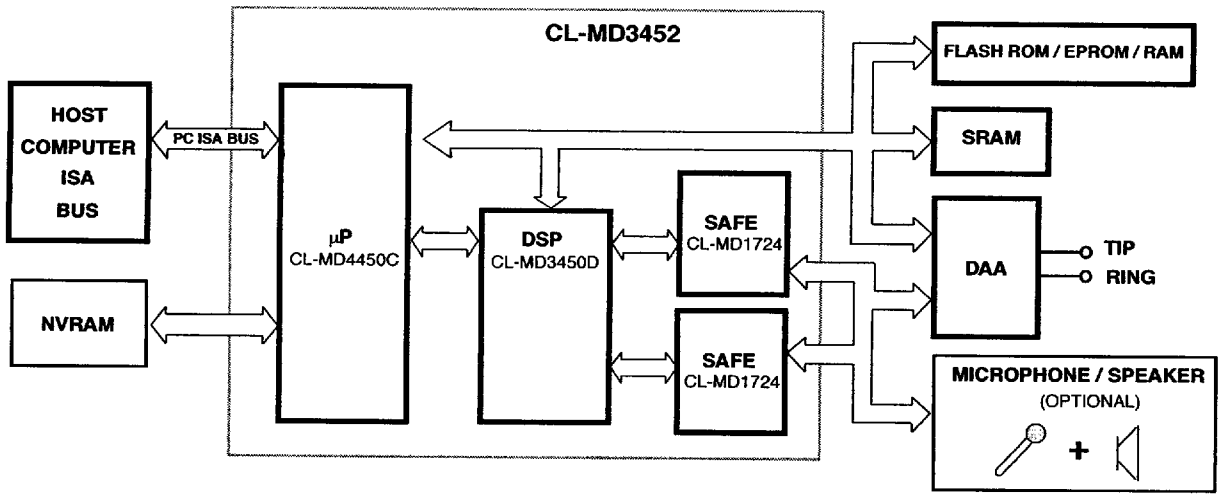

Figure 1-3. CL-MD3452 Functional Block Diagram

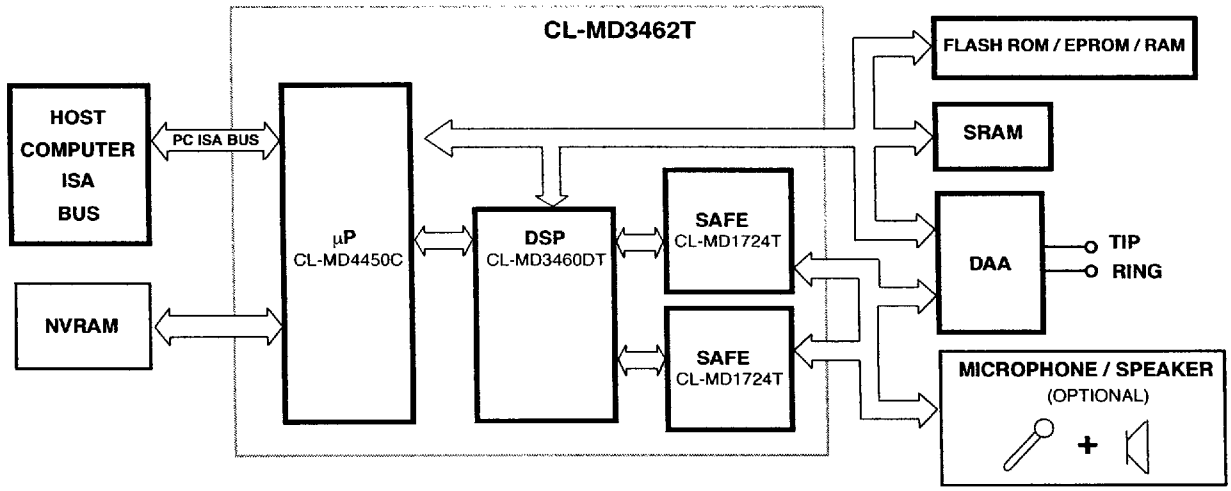

Figure 1-4. CL-MD3462T Functional Block Diagram

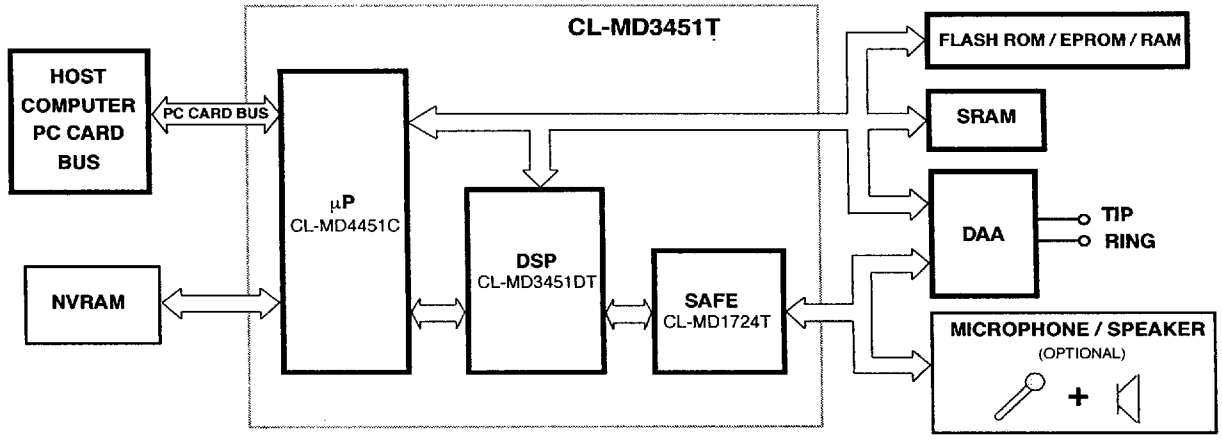

Figure 1-5. CL-MD3451T PC Card Functional Block Diagram

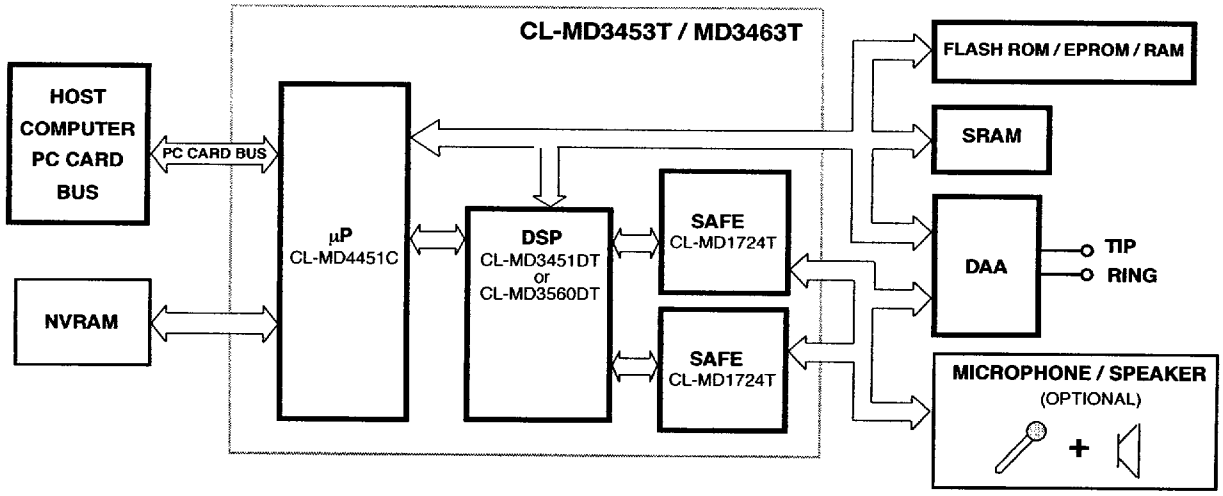

Figure 1-6. CL-MD3453T / MD3463T PC Card Functional Block Diagram

2. CHIPSET DESCRIPTIONS

The V.34+ FastPath™ family is a three- or four-chip solution consisting of a µP (microprocessor), a DSP (digital signal processor), and one or two SAFE (sigma-delta analog front end) devices. These products (also known as smart modems) support a variety of applications and need no additional firmware development. Currently, there are six V.34+ chipset solutions. These are shown in Figure 1-1 on page 11 with their corresponding µP, DSP, and SAFE device part numbers.

2.1 Microprocessor (µP)

Each chipset contains a µP specifically designed for modem applications. The µP implements all AT commands and manages all modem relays and the transmission and reception of data. The µP interfaces with the DTE and DSP. The µP's firmware contains code for all controller functions for Group 3 Fax mode, Data mode (without error correction or data compression), and Voice mode.

2.2 Digital Signal Processor (DSP)

The DSP performs all digital signal processing functions for the chipset, including modulation, echo cancellation, call progress monitoring, voice processing, and compression of voice and video signals.

The DSP offers two power options, depending on the chipset ordered. All PC Card (PCMCIA) chipsets use 3.3-V power. Initial production ISA- and serial-interface chipsets are 5 V only, but the DSP will be converted to a 3.3-V version to take advantage of the latest manufacturing technologies. Therefore, all board designs should include a 3.3-V regulator option (see schematics for details). The 3.3-V DSP not only reduces power consumption, it also enables the concurrent operation of speakerphone and DSVD using a single DSP.

2.3 Sigma-Delta Analog Front End (SAFE) Device

The SAFE device uses sigma-delta techniques to convert analog information from a telephone line to digital information that can be processed by the DSP. In addition to its analog circuitry, the modem's sigma-delta function incorporates unique and proprietary digital-to-analog and analog-to-digital features. These features improve receiver accuracy, which in turn improves performance at low levels of receive signal. Compared to other analog front-end technologies, the sigma-delta implementation better stabilizes the function of the SAFE devices and makes them less sensitive to board layout than other analog front end technologies. Since a significant amount of signal processing is performed by digital rather than analog techniques, sigma-delta analog-to-digital conversion considerably improves signal quality.

For basic Data, Fax, and Voice modes of operation, a single SAFE device is needed. To support DSVD or full-duplex speakerphone with echo cancellation, a second SAFE device is required.

Notes

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3. MODES OF OPERATION

The CL-MD34XX family provides complete modem functions for the following modes: Group 3 Fax, Data, Voice, V.42/MNP 2–4, and V.42 bis/MNP 5 (Microcom Networking Protocol Class 5). Each mode has its own unique AT command set. The data rates and modulation schemes for Data and Fax modes are presented in Table 3-1 on page 18. Additionally, these modem chipsets provide special modes of operation for VoiceView, power management, and loopback testing.

3.1 Data Mode

In the Data mode, the FastPath chipsets operate at up to 33.6 kbps. They implement all data rates and modulation schemes for ITU-T standards V.34, V.32 bis, V.32, V.22 bis, V.22, V.21, Bell 212A, and Bell 103. The V.34+ family implements a standard Data mode AT command set. This is compatible with any communication application software that supports the Hayes® AT command set. The standard AT commands for Data mode are listed in Table 5-1 on page 26.

3.2 V.42/MNP® 2–4 and V.42 bis/MNP® 5 Modes

The FastPath family supports error correction (V.42/MNP 2–4) and data compression (V.42 bis/MNP 5). Error correction ensures error-free data transfer. Data compression substantially increases the modem data throughput over the basic data rate throughput. Depending on the data stream, MNP 5 may provide up to two-to-one compression. Alternately, ITU-T V.42 bis may provide up to four-to-one compression. A description of the AT commands that support error correction and data compression are provided in Table 5-2 on page 31.

3.3 Fax Mode

In Fax mode, the FastPath chipsets operate at up to 14.4 kbps (transmit and receive) and implement all the data rates and modulation schemes for ITU-T standards V.17, V.29, V.27 ter, and V.21 ch2. The chipsets implement a standard Fax mode AT command set compatible with any communication application software that supports EIA/TIA-578 Fax Class 1 standards. The standard AT commands for Fax mode are listed in Table 5-3 and Table 5-4 on page 33.

3.4 Voice Mode

All chipsets support Telephone-Emulation mode, IS-101 voice commands, and record and playback message capabilities. Telephone-Emulation mode allows a handset/microphone-speaker and modem to be used as a complete telephone. In Telephone-Emulation mode, the received data from the SAFE (CL-MD1724 or CL-MD1724T) microphone interface is looped back to the SAFE analog transmit pins. In Voice mode, the message record and playback abilities are accessed by the extended AT command set, shown in Table 5-5 on page 34 through Table 5-7 on page 35.

3.5 Radish® VoiceView™ Mode

The V.34+ family gives the option to upgrade to Radish VoiceView, a widely supported protocol that alternates between voice and data. VoiceView enables data transfer during a regular telephone connection. It can be used in a variety of applications, such as customer service and technical support.

3.6 Digital Simultaneous Voice and Data (DSVD)

Each CL-MD3462 and CL-MD3463 chipset contains an embedded G.729A vocoder that supports digital simultaneous voice and data (DSVD), which allows data to be transferred realtime during a voice conversation. DSVD can be used for interactive applications such as whiteboard conferencing or real-time action games. DSVD is transparent to the application software. Enable DSVD by changing the program modem initialization string to include the DSVD AT command.

Table 3-1. Communication Modes and Data Rates

Application	Mode	Data Rate (kbps)	Modulation	Baud Rate (symbols/sec.)	Carrier Frequency (Hz) (originate/answer)	Constellation Points
Fax	V.17	14.4	TCM	2400	1800	128
		12.0	TCM	2400	1800	64
		9.6	TCM	2400	1800	32
		7.2	TCM	2400	1800	16
	V.29	9.6	QAM	2400	1700	16
		7.2	QAM	2400	1700	8
		4.8	QAM	2400	1700	4
	V.27 ter	4.8	DPSK	1600	1800	8
		2.4	DPSK	1200	1800	4
	V.21	0.3	FSK	300	1650 M/1850 S	1
Data	V.34	33.6	TCM	Variable[a]	Variable[b]	Variable[c]
		31.2	TCM	Variable[a]	Variable[b]	Variable[c]
		28.8	TCM	Variable[a]	Variable[b]	Variable[c]
		26.4	TCM	Variable[a]	Variable[b]	Variable[c]
		24.0	TCM	Variable[a]	Variable[b]	Variable[c]
		21.6	TCM	Variable[a]	Variable[b]	Variable[c]
		19.2	TCM	Variable[a]	Variable[b]	Variable[c]
		16.8	TCM	Variable[a]	Variable[b]	Variable[c]
		14.4	TCM	Variable[a]	Variable[b]	Variable[c]
		12.0	TCM	Variable[a]	Variable[b]	Variable[c]
		9.6	TCM	Variable[a]	Variable[b]	Variable[c]
		7.2	TCM	Variable[a]	Variable[b]	Variable[c]
		4.8	TCM	Variable[a]	Variable[b]	Variable[c]
		2.4	TCM	Variable[a]	Variable[b]	Variable[c]
	V.32 bis	14.4	TCM	2400	1800	128
		12.0	TCM	2400	1800	64
		9.6	TCM	2400	1800	32
		7.2	TCM	2400	1800	16
		4.8	TCM	2400	1800	4
	V.32	9.6	TCM	2400	1800	32
		9.6	QAM	2400	1800	16
		4.8	QAM	2400	1800	4
	V.22 bis	2.4	QAM	600	1200/2400	16
	V.22	1.2	DPSK	600	1200/2400	4
	V.21	0.3	FSK	300	980 M/1650 M 1180 S/1850 S	1
	Bell 212A	1.2	DPSK	600	1200/2400	4
	Bell 103	0.3	FSK	300	1270 M/2225 M 1070 S/2025 S	1

[a] Cirrus Logic supports five of the six baud rates specified by the ITU-T (International Telecommunications Union-Telecommunications): 2400, 2743, 3000, 3200, and 3429 symbols/second. The ITU-T's optional baud rate of 2800 symbols/second is not supported.

[b] The high and low carrier frequencies specified by ITU-T are supported for each baud rate.

[c] Cirrus Logic supports the normal and expanded constellations for each baud and data rate.

3.7 Videoconferencing (V.80) Support

All versions of the CL-MD34XX chipset family support the ITU-V.80 recommendation. This feature ensures compatibility with host-based H.324 videoconferencing application software. The CL-MD34XX family supports both transparent and framed submodes of the V.80 synchronous access mode.

3.8 Full-Duplex Speakerphone

The V.34+ FastPath family supports full-duplex speakerphone with internal adaptive echo cancellation. Phone users can talk simultaneously without the remote user hearing an echo. This speakerphone feature also is supported by DSVD.

3.9 Power Management Modes

The CL-MD34XX family provides both Sleep and Stop modes to reduce power consumption when the modem is inactive. Stop mode turns off all modem power except for the circuitry needed to maintain the host interface signals at the appropriate high-impedance state. To enter Stop mode, the host asserts the µP stop pin. When the stop pin is deasserted, the modem exits Stop mode, performs an internal reset, and enters Power-on mode. After the modem internal reset, the DTE reconfigures the modem.

Power-on mode consists of an Operational mode and a Sleep (or power-down) mode. In Operational mode, the modem chipset is fully powered and is either communicating with the host and/or another modem or is performing internal processing. In Sleep mode, power is turned off to most of the internal circuitry of the µP, DSP, and SAFE. Sleep mode is controlled by S-register **S33**. When enabled, the µP enters Sleep or Power-down mode whenever the modem has been inactive for a user-programmable time delay.

The modem is considered to be in an inactive state when:

1) No internal processing is being performed;
2) No activity occurs between the host and the modem within a specified time period (S–register **S33**);
3) The modem is on-hook.

The modem exits Sleep mode whenever the host writes to the modem or when a ring signal is detected. The modem does not wake up when the host reads the UART registers.

See Section 8.3 on page 75 for the µP's DC electrical characteristics.

3.10 Loopback Test Modes

Testing with local analog loopback, local analog loopback with self-test, remote digital loopback, and remote digital loopback with self-test are provided for testing modem-to-modem and modem-to-DTE communication integrity. These tests are accessed through the **AT&Tn** command and are explained in more detail in the CL-MD34XX Programmer's Guide.

3.11 Transmit Levels

The factory default transmit level is -10 dBm ± 1 dB at Tip and Ring. Data and fax use separate transmission levels. The transmit level can be programmed using the firmware configuration utility.

3.12 Transmit Tone Levels

The modem generates DTMF, answer, call, and guard tones. The specification for each tone is provided in Table 3-2 and Table 3-3 on page 20. DTMF tones are transmitted at –6 dBm for Tone 1 and –4 dBm for Tone 2. The transmit level can be programmed using the firmware configuration utility.

3.13 Receive Level

The receiver can accommodate a receive signal from –9 dBm to –43 dBm. The DCD (data carrier detect) function is activated at –43 dBm and above; it is deactivated at –48 dBm and below.

3.14 Receiver Tracking

The receiver compensates for up to ± 7 Hz of carrier-frequency offset.

3.15 Equalizers

Automatic adaptive and compromise equalizers are provided to compensate for line distortions.

3.16 Call Progress

The modem monitors the detection of call-progress tones during call origination and reports them to the DTE. Call-progress tones include dial, busy, ringback, and answer.

3.17 Caller ID

Caller ID is a service that allows the user to see the caller's telephone number. Caller ID also provides information on call date and time. For more information about this service, refer to Appendix A of the CL-MD34XX Programmer's Guide.

3.18 Firmware Soft Upgrades

CL-MD34XX chipsets that are Flash memory-based can be upgraded via communication software. See the Firmware Downloading Instructions in the CL-MD34XX-XX Applications Book for more information.

3.19 International Support

The FastPath chipsets support international applications. To obtain the settings for a particular country, download new modem specifications from the Cirrus Logic BBS and modify the firmware using the international configuration utility supplied by Cirrus Logic. For information on specific countries, contact your local Cirrus Logic sales office at the address listed on the back cover of this document.

Table 3-2. Transmit Tones

Tone	Value	Application
Calling tone	1100 Hz	Fax originator
	1300 Hz	Data originator
Answer tone	2100 Hz	Data/fax (ITU-T)
	2225 Hz	Data (Bell mode)
Guard tone	1800 Hz	Data/fax (answer mode)
	550 Hz	

Table 3-3. DTMF Tone Pairs

Dial Digit	Tone 1 (Hz)	Tone 2 (Hz)
0	941	1336
1	697	1209
2	697	1336
3	697	1447
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1447
*	941	1209
#	941	1447
A	697	1633
B	770	1633
C	852	1633
D	941	1633

4. HARDWARE INTERFACES

The V.34+ FastPath chipsets support hardware interfaces for the host, Flash memory, expansion bus, NVRAM, DAA, speaker, microphone, and general-purpose I/O functions. The hardware interfaces are demonstrated in Figure 4-1, the CL-MD3450 system block diagram.

4.1 Host Interfaces

Some chipsets can support either a parallel or a serial host interface. The interface type is selected by connecting the µP HOSTSEL0/CS4* and HOSTSEL1/CS5* pins to V_{CC} or ground through a resistor. Other chipsets support PC Card host interfaces.

4.1.1 Serial RS-232 Interface

The serial interface that supports TTL levels is compatible with an RS-232 interface.

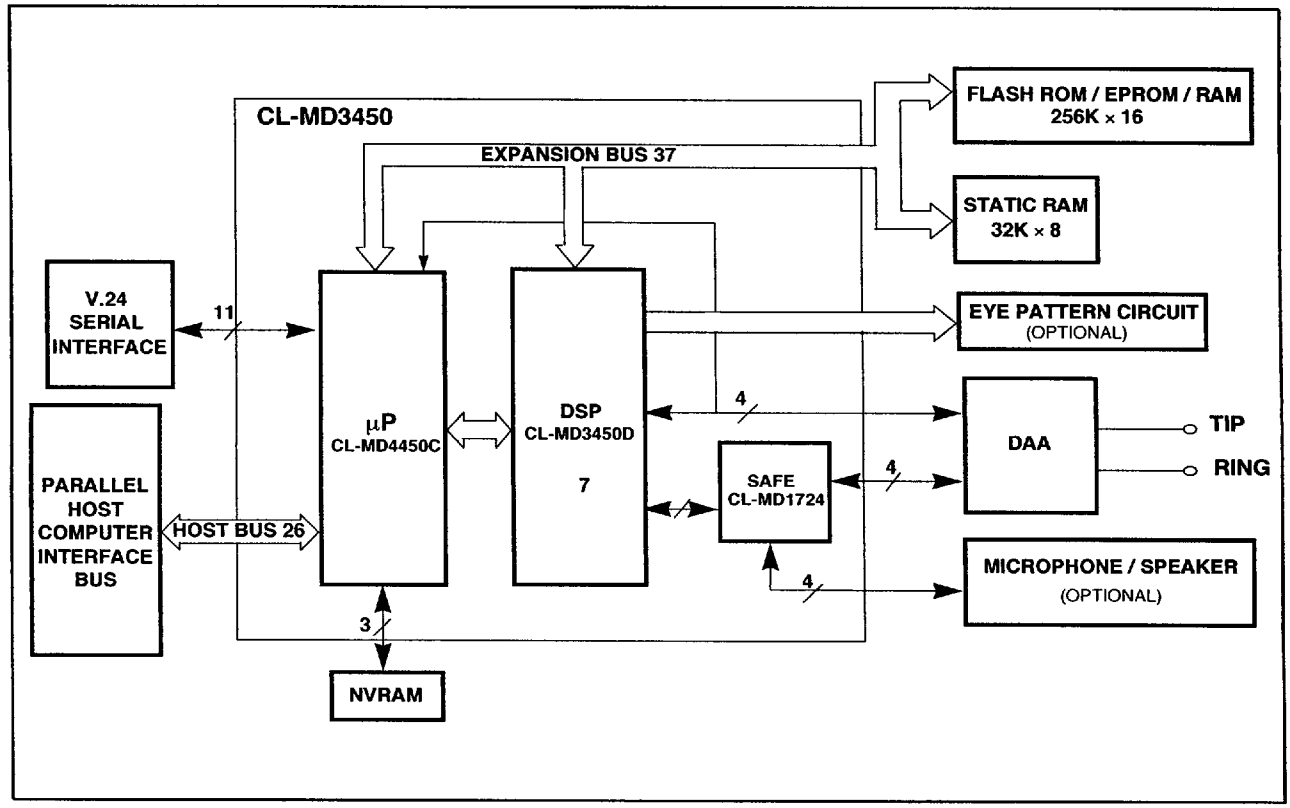


Figure 4-1. Modem System Block Diagram (CL-MD3450)

4.1.2 Parallel Bus Interface

The parallel interface emulates the electrical and register functions of 16C550A and 16C450 UARTs. Upon modem reset, the UART interface defaults to a 16C450 UART. The DTE can then configure the UART to function as a 16C550A UART. Table 4-2 on page 24 shows the UART register bit assignments.

The parallel UART interface can be selected to internally decode the addresses for COM ports 1 through 4 using the COMSEL0 and COMSEL1 settings. For applications not using COM ports 1 through 4, the standard method of selecting the modem with external address decoding also is provided. The type of address decoding is selected by either asserting or deasserting the signal at the µP HOSTSEL0 and HOSTSEL1 hardware pins.

The parallel UART also provides an internal tristate bus interface that eliminates the need for external bus drivers between the host bus and the modem UART. These features eliminate the need for a 74HCT245 and a 74HCT30 device, and they facilitate system designs with lower chip counts, power requirements, and costs.

4.1.3 Plug-and-Play Interface

Additionally, the chipsets support a parallel plug-and-play host interface. The chipset allows an OEM to design one board to support both plug-and-play and non-plug-and-play PC bus applications. The additional plug-and-play pin requirements are described in Section 7.1.1 on page 46 of this document.

4.1.4 PC Card Interface

The CL-MD34XX family integrates a PC Card host interface that allows the modem to be connected directly to a PC Card bus without additional hardware. This host interface also provides a 16C450/16C550 register-compatible UART. Upon modem reset, the UART interface defaults to a 16C450 emulation. The DTE can then configure the UART to function as a 16C550A. Table 4-2 on page 24 shows the UART register bit assignments.

A built-in CIS (card information structure) eliminates the need for an external CIS ROM. The CIS contents are stored in the external µP microcontroller memory (such as Flash ROM or EPROM).

To customize the modem design, the factory default CIS may be overridden by changing the microcontroller firmware CIS contents using the modem's configuration utility program.

4.2 Flash Interface

A Flash interface allows OEMs and end users to quickly and easily download new features as they become available. The FastPath chipsets' Flash interface works with the parallel and PC Card host interfaces and allows the microcontroller firmware code to be downloaded from a PC to the modem Flash ROM or RAM. When firmware is downloaded, it goes through the UART interface, thus eliminating the need for the additional address space and extra hardware required by competing designs.

4.3 Expansion Bus Interface

An expansion bus provides access to external memory and circuitry. The expansion bus is used for the µP microcontroller firmware and SRAM. The µP's firmware bus access time is 70 ns for the µP's Flash ROM, RAM, or EPROM (see Table 4-1). For standard products, this memory device can be 128K x 16 bits or 256K x 8 bits. Additional memory may be required for special applications.

A 32K x 8 bit, 25-ns SRAM is required for all CL-MD34XX-based modems. The SRAM is used to buffer data during data, voice, DSVD, fax, and V.42/MNP modes of operation.

Table 4-1. Expansion Bus Access Times

Memory	Access Times
EPROM Flash 128 K x 16 bits	150 ns
EPROM Flash 256 K x 8 bits	70 ns
SRAM 32 K x 8 bits	25 ns

4.4 NVRAM Interface

A serial interface is provided for a 2 K bit (x 8 configuration) non-volatile RAM (NVRAM). An NVRAM may be used for storing modem configurations and telephone numbers. Plug-and-play designs require NVRAM for the board's serial number information.

4.5 DAA Interface

A DAA (Data Access Arrangement) is the interface between the modem chipset and the telephone network. The DAA interface controls the telephone line off-hook relays, detects ring signals, and transmits and receives analog signals.

4.6 Speaker Interface

The SAFE device internally implements both the volume control and amplifier necessary to drive an external speaker. The output of the internal amplifier can be connected directly to a speaker or to the input of the host speaker amplifier. The internal amplifier is capable of driving a minimum load of 8 Ω up to a maximum load of 100 Ω. The speaker volume is controlled by the **ATLn** command.

4.7 Microphone Interface

The CL-MD1724or CL-MD1724T SAFE device provides a microphone interface that connects a microphone or handset to the modem with a minimum of external parts. This microphone input can then be used for local Voice record mode or for Telephone-Emulation mode.

4.8 General-Purpose I/O Interface

To customize the modem design, the μP provides 24 general-purpose pins that can be used to control or monitor external circuitry.

Some of the general-purpose pins can be configured for specific functions (such as a Caller ID relay, CIDREL*). Pin functions can be selected using the μP firmware's configuration utility program. Some Voice mode functions are enhanced by adding external circuitry for remote hang-up detection, extension phone pickup, or hang-up detection (see Table 5-7, "Voice DTE←DCE Character Pairs", on page 35).

Table 4-2. Parallel Host Interface UART Register Bit Assignments

REGISTER ADDRESS	REGISTER NAME	BIT NUMBER							
		7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register (SCR)							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCDD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	Error in RCVR FIFO (Note 1)	Transmitter Empty (TEMT)	Transmitter Holding Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Loop	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break (SBRK)	Stick Parity (SPAR)	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	FIFO Control Register [Write only] (FCR)	RCVR Trigger (MSB)	RCVR Trigger (LSB)	Reserved	Reserved	Reserved	XMIT FIFO Reset (XFIFOR)	RCVR FIFO Reset (RFIFOR)	FIFO Enable (FIFOE)
2	Interrupt Identity Register [Read only] (IIR)	FIFOs Enabled (See note)	FIFOs Enabled (See note)	0	0	Interrupt ID Bit 2 (See note)	Interrupt ID Bit 1	Interrupt ID Bit 0	'0' if Interrupt pending
1 DLAB=0	Interrupt Enable Register (IER)	0	0	0	0	Modem Status Interrupt Enable (MSIE)	Receiver Line Status Interrupt Enable (RLSIE)	Transmitter Holding Reg. Empty Int. Enable (THREIE)	Received Data Available Int. Enable (RDAIE)
0 DLAB=0	Transmit Holding Register [Write only] (THR)	Transmit Holding Register (THR) [Write only]							
0 DLAB=0	Receiver Buffer Register [Read only] (RBR)	Receiver Buffer Register (RBR) [Read only]							
1 DLAB=1	Divisor Latch (MS) (DLM)	Divisor Latch (MS)							
0 DLAB=1	Divisor Latch (LS) (DLL)	Divisor Latch (LS)							

NOTE: These bits are always '0' in 16C450 mode.

5. AT COMMAND SET

5.1 AT Command Descriptions

The FastPath chipsets' AT command set and S-registers are divided into four categories: Group 3 fax, data, V.42/MNP, and voice. Summaries of all commands are provided in Table 5-1 on page 26 through Table 5-14 on page 40, while Table 5-12 on page 38 provides a summary of all S-registers.

All command lines sent to the modem, except for **A/**, must be preceded by an 'AT' and terminated by the contents of S-register **S3** (typically a carriage return <CR>). AT stands for 'attention' and prompts the modem to receive a command line from the DTE. A <CR> informs the modem that the entire command string has been transmitted and that the modem should begin processing all the commands in the command line. A command line may include one or more AT commands. The commands may be separated by a space, if desired, but no punctuation is needed except for fax and voice commands. In a multiple-command line, fax and voice AT commands must be separated from following commands by a semicolon (;).

Examples:

```
ATS1?<CR>
A/
AT &F &D2 +FCLASS=?<CR>
AT +FCLASS=80; S0=1<CR>
```

The modem provides status information to the DTE in the form of response codes. The supported response codes are listed in Table 5-13 on page 39.

After sending an AT command string to the modem, the DTE must wait for a response code from the modem before sending a new AT command string to the modem.

5.2 AT Escape Sequences

The CL-MD34XX provides two industry-standard escape sequences: the Hayes® Escape Sequence and the Time Independent Escape Sequence (TIES).

Currently, most modems implement the Hayes Escape Sequence; but because licensing may be required, the V.34+ chipsets include TIES as an alternative. TIES is designed to work with existing communication software written for the Hayes Escape Sequence.

TIES/Hayes® Escape Sequences

The Cirrus Logic CL-MD34XX modem chipset is manufactured with TIES (Time Independent Escape Sequence) as the default setting. It is Hayes' position that you must have a valid license from Hayes Micro Computer of Norcross, Georgia, before producing modem systems that use the Hayes Escape Sequence.

Cirrus Logic accepts no responsibility and does not indemnify nor in any way provide protection for patent or possible patent violations to its customers or users of its products.

Table 5-1. Basic Data Modem AT Commands

	Command	Function	Default	Range	Reported by &Vn
**	A/	Repeat last command	none	–	no
	A	Answer	none	–	no
*	Bn	Select ITU-T or Bell	1	0–3	yes
	B0	Selects ITU-T V.22 at 1200 bps and ITU-T V.21 at 300 bps			
	B1	Selects Bell 212A at 1200 bps and Bell 103J at 300 bps			
	B2	Selects ITU-T V.23 only. The originating modem transmits at 75 bps (and receives at 1200 bps); the answering modem receives at 75 bps (and transmits at 1200 bps)			
	B3	Selects ITU-T V.23 only. The originating modem transmits at 1200 bps (and receives at 75 bps); the answering modem receives at 1200 bps (and transmits at 75 bps)			
	Cn	Carrier control option	1	0, 1	no
	C0	Transmit carrier always off			
	C1	Normal transmit carrier			
	D	Dial command	none	–	no
*	En	Command mode echo	1	0, 1	yes
	E0	Disables echo			
	E1	Enables echo			
	Fn	Online echo	1	0, 1	no
	F0	Enables online echo			
	F1	Disables online echo			
	Hn	Switch hook control	0	0, 1	no
	H0	Hangs up the telephone line			
	H1	Picks up the telephone line			
	In	Identification/checksum option	0	0–14, 20–24	no
	I0	Reports product code			
	I1	Reports modem chip firmware version			
	I2	Verifies ROM checksum			
	I3	Reports chipset name			
	I4	Reserved			
	I5	Reserved for modem chip hardware configuration			
	I6	Country code			
	I7	Version of board manufacturer firmware			
	I8	Features of modem firmware			
	I10	Modem board configuration — bits set by board manufacturer			

Table 5-1. Basic Data Modem AT Commands (cont.)

	Command	Function	Default	Range	Reported by &Vn
	I11	Modem board configuration — bits set by board manufacturer			
	I14	SAFE device			
	I20	Cirrus Logic silicon version			
	I21	Cirrus Logic firmware version			
	I22	Cirrus Logic manufacturer name			
	I23	Cirrus Logic product model			
*	Ln	Speaker volume control	2	0–3	yes
	L0	Low speaker volume			
	L1	Low speaker volume			
	L2	Medium speaker volume			
	L3	High speaker volume			
*	Mn	Speaker control	1	0–3	yes
	M0	Speaker always off			
	M1	Speaker on until carrier present			
	M2	Speaker always on			
	M3	Speaker off during dialing; speaker on until carrier present			
*	Nn	Select data rate handshake	1	0, 1	yes
	N0	Handshake only at DTE-to-modem data rate			
	N1	Begins handshake at DTE-to-modem data rate and falls to highest compatible rate			
	On	Go online	0	0, 1	no
	O0	Returns modem to Data mode			
	O1	Retrains equalizer and then returns to Data mode			
*	P	Select pulse dialing	none	–	yes
*	Qn	Result code display control	0	0, 1	yes
	Q0	Enables result codes			
	Q1	Disables result codes			
	Sn	Select an S-register	none	0–37	no
	Sn=x	Write to an S-register	none	n=0–37 x=0–255	no
	Sn?	Read from an S-register	none	0–37	no
*	T	Select tone dialing	none	–	no
*	Vn	Result code form	1	0, 1	yes
	V0	Choose numeric form			
	V1	Choose verbose (text) form			
*	Wn	Response code data rate	0	0–4	yes
	W0	Reports DTE speed response codes			

Table 5-1. Basic Data Modem AT Commands (cont.)

	Command	Function	Default	Range	Reported by &Vn
	W1	Reports DTE speed response codes			
	W2	Reports DCE speed response codes			
	W3	Reports DTE speed response codes and information on error correction and data compression			
	W4	Reports protocol, data compression, and DTE data rate			
*	Xn	Result code type	4	0–4	yes
	X0	Enables result codes 0–4; disables detection of busy and dial tone			
	X1	Enables result codes 0–5, 10, and above; disables busy and dial tone detection			
	X2	Enables result codes 0–6 and 10 and above; disables busy detection and enables dial tone detection			
	X3	Enables result codes 0–5, 7, and 10 and above; enables busy detection and disables dial tone detection			
	X4	Enables result codes 0–7 and 10 and above; enables busy and dial tone detection			
*	Yn	Long space disconnect	0	0, 1	yes
	Y0	Disables long space disconnect			
	Y1	Enables long space disconnect			
	Zn	Recall stored profile	0	0, 1	no
	Z0	Resets modem and recalls user profile 0			
	Z1	Resets modem and recalls user profile 1			
*	&Cn	DCD (data carrier detect) option	1	0, 1	yes
	&C0	Ignores remote modem status; DCD always on			
	&C1	DCD set according to remote modem status			
	&Dn	DTR (data terminal ready) option	2	0–3	yes
	&D0	In Async mode, modem ignores DTR			
	&D1	Modem switches from data mode to command mode when an on-to-off transition of DTR occurs			
	&D2	When DTR switches off, the modem goes on-hook and disables Auto-answer mode; when DTR switches on, auto-answer is enabled			
	&D3	Turning off DTR re-initializes the modem and resets values except UART registers			
	&F	Load factory defaults	none	–	no
*	&Gn	Guard tone option (1200 bps and 2400 bps only)	0	0–2	yes
	&G0	Disables guard tone			

Table 5-1. Basic Data Modem AT Commands (cont.)

	Command	Function	Default	Range	Reported by &Vn
	&G1	Enables 550-Hz guard tone			
	&G2	Enables 1800-Hz guard tone			
*	&Jn	Auxiliary relay control	0	0, 1	yes
	&J0	Auxiliary relay never operated			
	&J1	Activates auxiliary relay when modem is off-hook			
	&Kn	Select serial flow control	3	0, 3, 4	yes
	&K0	Disables flow control			
	&K3	Bidirectional hardware flow control			
	&K4	XON/XOFF software flow control			
*	&M0	Communication mode option — modem supports only Async mode	0	0	no
*	&Pn	Dial pulse ratio	0	0, 1	yes
	&P0	Sets 10-pps pulse dial with 39%/61% make-break			
	&P1	Sets 10-pps pulse dial with 33%/67% make-break			
*	&Q0	Communication mode option — modem supports only Async mode	0	0	yes
*	&Sn	DSR (data set ready) option	0	0, 1	yes
	&S0	DSR is always active			
	&S1	DSR active only during handshaking and when carrier is lost			
	&Tn	Self test commands	0	0–8	no
	&T0	Terminates test in progress			
	&T1	Initiates local analog loopback			
	&T4	Grants RDL request from remote modem			
	&T5	Denies RDL request from remote modem			
	&T6	Initiates remote digital loopback			
	&T7	Starts remote digital loopback with self-test			
	&T8	Initiates local analog loopback with self-test			
*	&Un	Disable Trellis coding	0	0, 1	yes
	&U0	Enables Trellis coding with QAM as fallback			
	&U1	QAM modulation only			
	&Vn	View active and stored profiles	0	0, 1, 3	no
	&V0	View stored profile 0			
	&V1	View stored profile 1			
	&V3	View relay and general-purpose input-output status			
	&Wn	Stored active profile	0	0, 1	no
	&W0	Store in user profile 0			

Table 5-1. Basic Data Modem AT Commands (cont.)

	Command	Function	Default	Range	Reported by &Vn
	&W1	Store in user profile 1			
*	&Yn	Select stored profile on power up	0	0, 1	yes
	&Y0	Recall stored profile 0 on power-up			
	&Y1	Recall stored profile 1 on power-up			
	&Zn=x	Store telephone number (up to 30 digits) to location 'n' (0–3)	none	n = 0–3 x = 0–9 A B C D # * T P R W @ , ! ;	no
*	%En	Auto-retrain control	1	0, 1	yes
	%E0	Disables auto-retrain			
	%E1	Enables auto-retrain			
*	%Gn	Rate renegotiation	0	0, 1	yes
	%G0	Disabled			
	%G1	Enabled			
*	-Cn	Generate data modem calling tone	1	0–2	yes
	-C0	Calling tone disabled			
	-C1	1300-Hz calling tone enabled			
	-C2	V.8 calling tone and 1300-Hz calling tone			
	+GMI?	Identify modem manufacturer	none	–	no
	+GMM?	Identify product model	none	–	no
	+GMR?	Identify product revision	none	–	no
	+MS=m	Modulation selections	V34B, 1, 300, 0	See note [a]	no

[a] See full command description in the CL-MD34XX Programmer's Guide for parameter ranges. For Data mode, the factory default setting is AT+MS=V34B, 1, 300, 0 to connect at 33,600 bps and below.

* Value saved in NVRAM.

** Command not preceded by an 'AT'.

Table 5-2. V.42 / V.42 bis MNP® AT Commands

	Command	Function	Default	Range	Reported by &Vn
*	%An	Set auto-reliable fallback character	13	0–127	yes
*	%Cn	MNP 5 data compression control	1	0, 1	yes
	%C0	No compression			
	%C1	Enables MNP5 data compression			
*	\An	MNP block size	3	0–3	yes
	\A0	Maximum 64 characters			
	\A1	Maximum 128 characters			
	\A2	Maximum 192 characters			
	\A3	Maximum 256 characters			
*	\Bn	Transmit break	none	0–9	no
*	\Cn	Set auto-reliable buffer	0	0–2	yes
	\C0	No data buffering			
	\C1	Four-second buffer until 200 characters in the buffer or detection of a SYN character			
	\C2	No buffering. Connects non-V.42 modems to V.42 modem			
*	\Gn	Set modem port flow control	0	0, 1	yes
	\G0	Disables port flow control			
	\G1	Sets port flow control to XON/XOFF			
*	\Jn	bps rate adjust control	0	0, 1	yes
	\J0	Disables rate adjust			
	\J1	Enables rate adjust			
*	\Kn	Set break control	5	0–5	yes
	In connect state, transmits break to remote (if in Reliable mode):				
	\K0, 2, 4	Enters Command mode, no break sent			
	\K1	Destructive/expedited			
	\K3	Nondestructive/expedited			
	\K5	Nondestructive/nonexpedited			
	In command state, transmits break to remote (if in Reliable mode):				
	\K0, 1	Destructive/expedited			
	\K2, 3	Nondestructive/expedited			
	\K4, 5	Nondestructive/nonexpedited			
	In connect state, receives break at modem port (if in Direct mode):				
	\K0, 2, 4	Immediately sends break and enters command state			
	\K1, 3, 5	Immediately sends the break through			
	In connect state, receives break at modem port and sends to serial port:				
	\K0, 1	Destructive/expedited			
	\K2, 3	Nondestructive/expedited			

Table 5-2. V.42 / V.42 bis MNP® AT Commands (cont.)

	Command	Function	Default	Range	Reported by &Vn
	\K4, 5	Nondestructive/nonexpedited			
*	\Nn	Set operating mode	3	0–4	yes
	\N0, 1	Selects Buffer (Normal) mode with speed buffering			
	\N2	Selects MNP Reliable mode			
	\N3	Selects V.42 Auto-reliable mode			
	\N4	Selects V.42 Reliable mode			
	\O	Originate reliable link	none	–	no
*	\Qn	Set serial port flow control	3	0–3	yes
	\Q0	Disables flow control			
	\Q1	XON/XOFF software flow control			
	\Q2	Unidirectional hardware flow control			
	\Q3	Bidirectional hardware flow control			
*	\T0	Disables inactivity timer	0	0–90	yes
	\U	Accept reliable link	none	–	no
*	\Xn	Set XON/XOFF pass-through	0	0, 1	yes
	\X0	Processes flow control characters			
	\X1	Processes flow control characters and passes to local or remote			
	\Y	Switch to Reliable mode	none	–	no
	\Z	Switch to Normal mode	none	–	no
*	-Jn	Set V.42 detect phase	1	0, 1	yes
	-J0	Disables the V.42 detect phase			
	-J1	Enables the V.42 detect phase			
*	"Hn	V.42 bis compression control	3	0–3	yes
	"H0	Disables V.42 bis			
	"H1	Enables V.42 bis only when transmitting data			
	"H2	Enables V.42 bis only when receiving data			
	"H3	Enables V.42 bis for both transmitting and receiving data			
	"On	V.42 bis string length	32	6–250	yes

* Value saved in NVRAM.

Table 5-3. Fax Identity Commands

Command	Function	Default	Range	Reported by &Vn
+FMDL?	Identifies product model	none	–	no
+FMFR?	Identifies modem manufacturer	none	–	no
+FMI?	Identifies modem manufacturer	none	–	no
+FMM?	Identifies product model	none	–	no
+FMR?	Identifies product version number	none	–	no
+FREV?	Identifies product version number	none	–	no

Table 5-4. Fax Class 1 AT Commands

Command	Function	Default	Range	Reported by &Vn
+FAE=n	Fax/data autorecognition	0	0, 1	no
+FCLASS=1	Mode selection	0	0, 1, 8, 80	yes
+FRH=n	Receive HDLC data	none	3	no
+FRM=n	Receive data	none	24, 48, 72, 73, 74, 96, 97, 98, 121, 122, 145, 146	no
+FRS=n	Wait for silence	none	1–255	no
+FTH=n	Transmit HDLC data	none	3	no
+FTM=n	Transmit data	none	24, 48, 72, 73, 74, 96, 97, 98, 121, 122, 145, 146	no
+FTS=n	Stop transmission and pause	none	0–255	no

Table 5-5. IS-101 Voice AT Commands

Command	Function	Default	Range	Reported by &Vn
+FCLASS=8	Voice mode selection	0	0, 1, 8, 80	yes
+FLO=n	Flow Control Select	1	0–2	no
+VBT=m	Buffer threshold setting	192, 320	192, 320	no
+VCID=n	Caller ID selection	*0	0–2	no
#VCSD=n	Voice command mode silence detection	0	0, 1	no
+VDR=m	Distinctive Ring selection	0,0	0–255, 0–255	no
+VEM=m	Event reporting and masking	'C' BB860980 BFE63883 BB863EE0	–	no
+VGM=n	Speakerphone microphone gain	128	121–131	no
+VGR=n	Receive gain selection	128	121–131	no
+VGS=n	Speakerphone speaker gain	128	121-131	no
+VGT=n	Volume selection	128	121–131	no
+VIP	Initialize parameter	–	–	no
+VIT=n	DTE/DCE inactivity timer	0	0–255	no
+VLS=n	Relay/speaker control	0	0–16	no
+VNH=n	Automatic hang-up control	0	0–2	no
+VRA=n	Ringback-goes-away timer	50	0–50	no
+VRN=n	Ringback-never-appeared timer	10	0–255	no
+VRX	Record mode	none	–	no
+VSD=m	Silence detection (quiet and silence)	128, 50	See note	no
+VSM=m	Compression method selection	140, 8000, 0, 0	See note	no
+VSP=n	Speakerphone on/off control	0	0, 1	no
#VSPS=n	Speakerphone type selection	manufacturer-specified	0, 1	no
+VTD=n	Beep tone duration timer	100	5–255	no
+VTS=m	DTMF and tone generation	none	See note	no
+VTX	Play mode	none	–	no

NOTE: See this command's description in the CL-MD34XX Programmer's Guide for range information.

* The noted parameters, commands, and responses depend on the capability to receive.

Table 5-6. Voice DTE→DCE Character Pairs

Response	Hex Code	Function
<NUL>	00	Do nothing
<DLE>	10	Two contiguous <DLE><DLE> codes indicate a single <DLE> in the data stream
<SUB>	1A	<DLE><DLE> in data stream
<ETX>	03	End transmit data state
/	2F	Start of DTMF tone shielding
~	7F	DTMF transition to off
u	75	Bump up the volume
d	64	Bump down the volume
<ESC>	1B	End receive data state
!	21	Receive data abort
<CAN>	18	Clear transmit buffer of voice data
<FS>	1C	Concatenate transmit data streams
?	3F	Transmit buffer space available query

Table 5-7. Voice DTE←DCE Character Pairs

Response	Hex Code	Function
<DLE>	10	Single <DLE> character in the data stream
<SUB>	1A	<DLE><DLE> in data stream
<ETX>	3	End of Record mode data
X	58	Packet header for 'Complex Event Detection Report'
.	2E	Packet terminator for the 'Complex Event Detection Report'
/	2F	Start of DTMF tone shielding
~	7E	DTMF transition to off
0–9	30–39	DTMF tones 0–9
A–D	41–44	DTMF tones A–D
*	2A	DTMF tone *
#	23	DTMF tone #
o	6F	Receive buffer overrun
c	63	1100-Hz fax calling tone
e	65	1300-Hz data calling tone
h	68	Local phone goes on hook
H	48	Local phone goes off hook
s	73	Presumed hang-up silence time-out
q	71	Presumed end-of-message quiet time-out
l	6C	Loop current interruption
L	4C	Loop current polarity reversal
r	72	Ringback

Table 5-7. Voice DTE←DCE Character Pairs (cont.)

Response	Hex Code	Function
b	62	Busy/reorder/fast busy
d	64	Dial tone detected
u	75	Transmit buffer under-run
p	70	Line voltage increase (extension phone goes on-hook)
P	50	Line voltage decrease (extension phone goes off-hook)
a	61	Fax or data answer tone (2100 Hz)
f	66	Data answer detected (2225 Hz)
R	52	Incoming ring
% ' (,)	25, 26, 27, 28, 29	Manufacturer-specified

Table 5-8. VoiceView™ Commands

Command	Default	Function
+FCLASS=80	0	Mode selection
+FLO=n	1	Flow control select
+FPR	4	Select DTE/DCE Interface Rate —turn on/off autobaud
-SAC	–	Accept Data mode request
-SCD	–	Capabilities data
-SDA	–	Start modem Data mode
-SDS	–	Disable switchhook status monitoring (required if DCE implements switchhook status monitoring and is used with a handset adapter)
-SER?	–	Error status (read only)
-SFX	–	Start Fax data mode
-SIC	–	Reset capabilities to default setting
-SIP	–	Initialize VoiceView parameters
-SQR	–	Capabilities query response control
-SSP	–	VoiceView transmission speed
-SSQ	–	Start capabilities query
-SSR	–	Start sequence response control
-SVV	–	Start VoiceView data mode
+VGM=n	128	Speakerphone microphone gain
+VGS=n	128	Speakerphone speaker gain
+VLS=n	0	Analog source/destination selection
+VSP=n	0	Speakerphone on/off control

Table 5-9. VoiceView™ Response Codes

Response	Function
-SFA	Fax data mode start sequence event (mandatory only if Fax data mode is supported)
-SMD	Modem Data mode start sequence event (mandatory only if modem Data mode is supported)
-SRA	Receive ADSI response event
-SRC:	Receive capabilities information event
-SRQ	Receive capabilities query event
-SSV	VoiceView data mode start sequence event
-STO	Talk-off event

Table 5-10. VoiceView™ <DLE> Character Pairs

Command	Function
<CAN>	Abort data transfer in progress
<EOT>	End of message marker, final message of transaction, no response accepted
<ESC>	End of message marker, DCE shall immediately return to Voice mode
<ETB>	End of message marker, final response requested, after which the transaction terminates
<ETX>	End of message marker, continue transaction, response requested

Table 5-11. Dial Modifiers

Command	Function
0 to 9	Dialing digits
A, B, C, D, *, #	Tone dial characters
P	Pulse dial
R	Reverse Originate mode
S=n	Dial NVRAM telephone number
T	Tone dial
W	Wait for dial tone
,	Pause
!	Flash hook
@	Wait for quiet answer
;	Return to command state
- ( )	Ignored by modem

Table 5-12. S-Registers Summary

	Register	Function	Default	Range	Units	Reported by &Vn
*	S0	No. of rings to auto-answer on	0	0–255	ring	yes
	S1	Ring count	0	0–255	ring	yes
*	S2	Escape character	43	0–127	ASCII	yes
	S3	Carriage return character	13	0–127	ASCII	yes
	S4	Line feed character	10	0–127	ASCII	yes
	S5	Backspace character	8	0–32, 127	ASCII	yes
*	S6	Wait before dialing	2	2–255	second	yes
*	S7	Wait for carrier	60	1–255	second	yes
*	S8	Pause time for dial modifier	2	0–255	second	yes
*	S9	Carrier recovery time	6	1–255	0.1 second	yes
*	S10	Lost carrier hang up delay	14	1–255	0.1 second	yes
*	S11	DTMF dialing speed	70	50–255	ms	yes
*	S12	Guard Time	50	0–255	(0.02 second)	yes
*	S14	Bit-mapped options	170	–	–	no
	S16	Modem test options	0	–	–	no
*	S18	Modem test timer	0	0–255	second	yes
*	S21	Bit-mapped options	48	–	–	no
*	S22	Bit-mapped options	118	–	–	no
*	S23	Bit-mapped options	none	–	–	no
*	S25	Detect DTR change	5	0–255	0.01 second	yes
*	S27	Bit-mapped options	64	–	–	no
*	S30	Disconnect inactivity timer	0	0–255	minute	yes
*	S31	Bit-mapped options	none	–	–	no
*	S33	Sleep mode timer	10	0–90	second	yes
*	S37	Maximum line speed attempted	0	0–19	–	yes

* Value saved in NVRAM.

Table 5-13. DTE-Modem Data Rate Response Codes

Numeric Code	Verbose Code
0	OK
1	CONNECT
2	RING
3	NO CARRIER
4	ERROR
5	CONNECT 1200
6	NO DIAL TONE
7	BUSY
8	NO ANSWER
23	CONNECT 75/1200
22	CONNECT1200/75
10	CONNECT 2400
11	CONNECT 4800
24	CONNECT 7200
12	CONNECT 9600
25	CONNECT 12000
13	CONNECT 14400
59	CONNECT 16800
14	CONNECT 19200
61	CONNECT 21600
62	CONNECT 24000
63	CONNECT 26400
64	CONNECT 28800
28	CONNECT 38400
18	CONNECT 57600
31	CONNECT 115200
33	FAX
35	DATA
45	RINGBACK
See Note	CONNECT (DTE data rate) /(modulation)/(error correction)/(data compression) / TX:(DCE transmit data rate) / RX:(DCE receive data rate)

NOTE: This verbose response code is used to evaluate the modem connection and is enabled by the **W3** AT command. All other 'CONNECT' messages are used for **W0-W2** AT commands.

When the modem is configured for text responses **V1, W3** verbose response codes provide information about the DTE data rate, connection modulation, error correction protocol, data compression, and modem-to-modem data rate. When the modem is configured for **W3** and numeric responses **V0**, the modem responds as if it were set up for **W0**.

Table 5-14. Manufacturing-Only Commands [a]

	Command	Function	Default	Range
	%L	Receive line signal level	none	–
*	*NCnn	Country Select	0	–
	!P=m	Set plug-and-play board serial number	none	0–255, 0–255, 0–255, 0–255
*	S91	Select transmit level	10	0–15
*	S92	DTMF transmit level	10	0–15
	-Tn	Generate continuous DTMF tones	7	6, 7
	#VGP0=n	Read/write to general-purpose pins 0–7	See note	–
	#VGP1=n	Read/write to general-purpose pins 8–15	See note	–
	#VGP2=n	Read/write to general-purpose pins 16–23	See note	–

[a] These commands are meant to be used by the board manufacturer and not in generic applications software for end users.

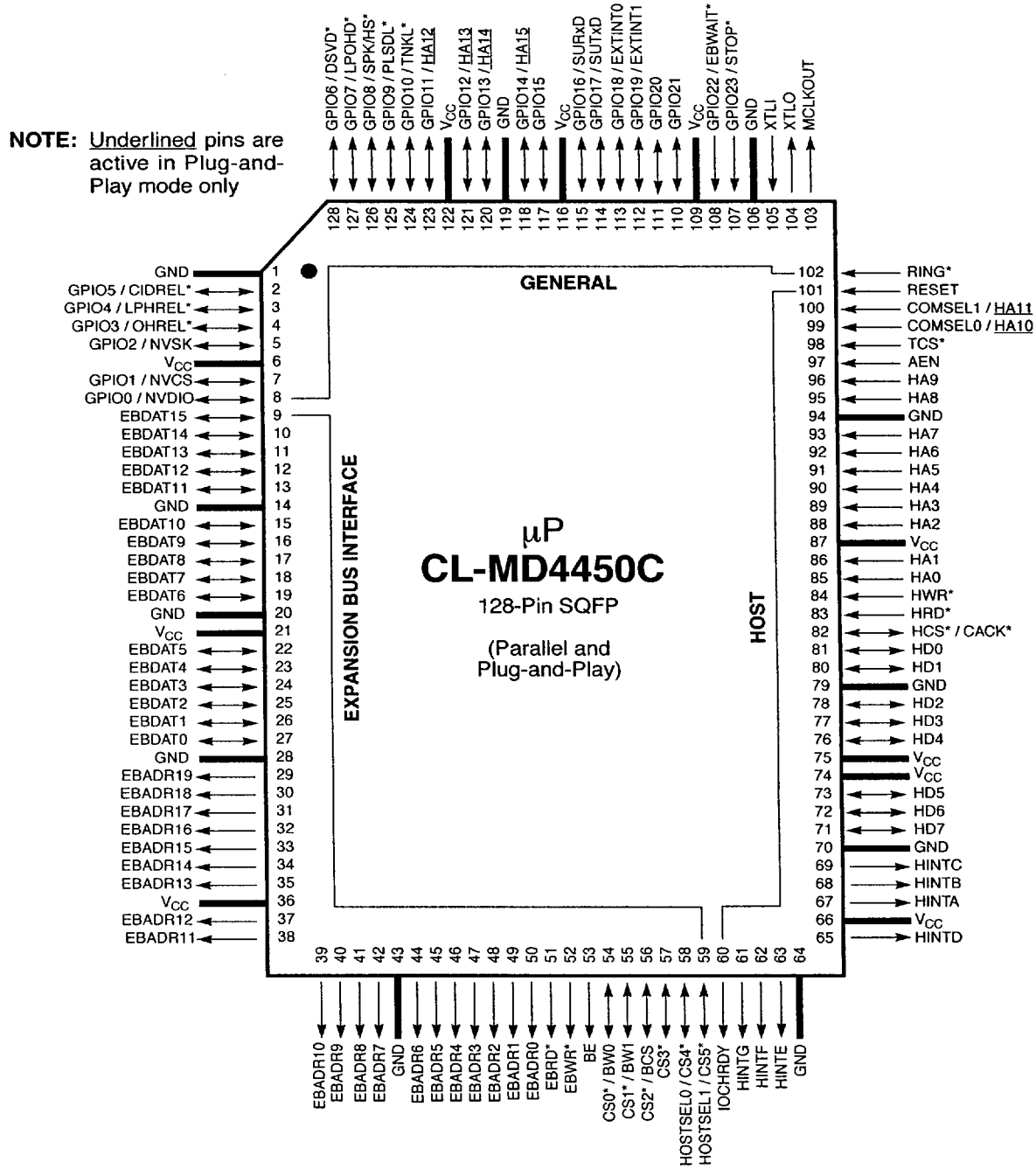
* Value saved in NVRAM.

NOTE: Default values for **#VGP0–2 =n** are dependent on board design.

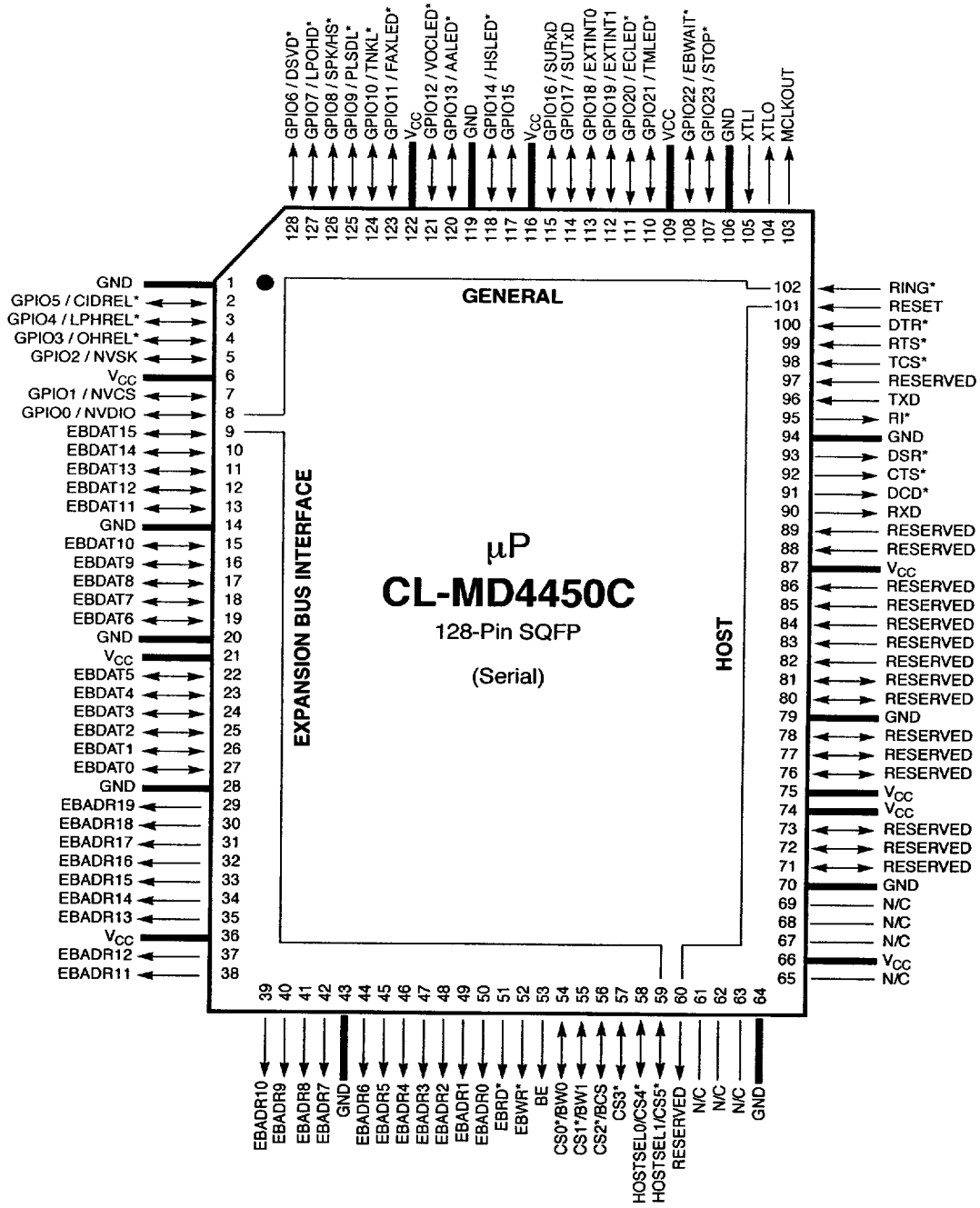
6. PIN DIAGRAMS

6.1 Microprocessor (μP) Pin Diagrams (CL-MD4450C)

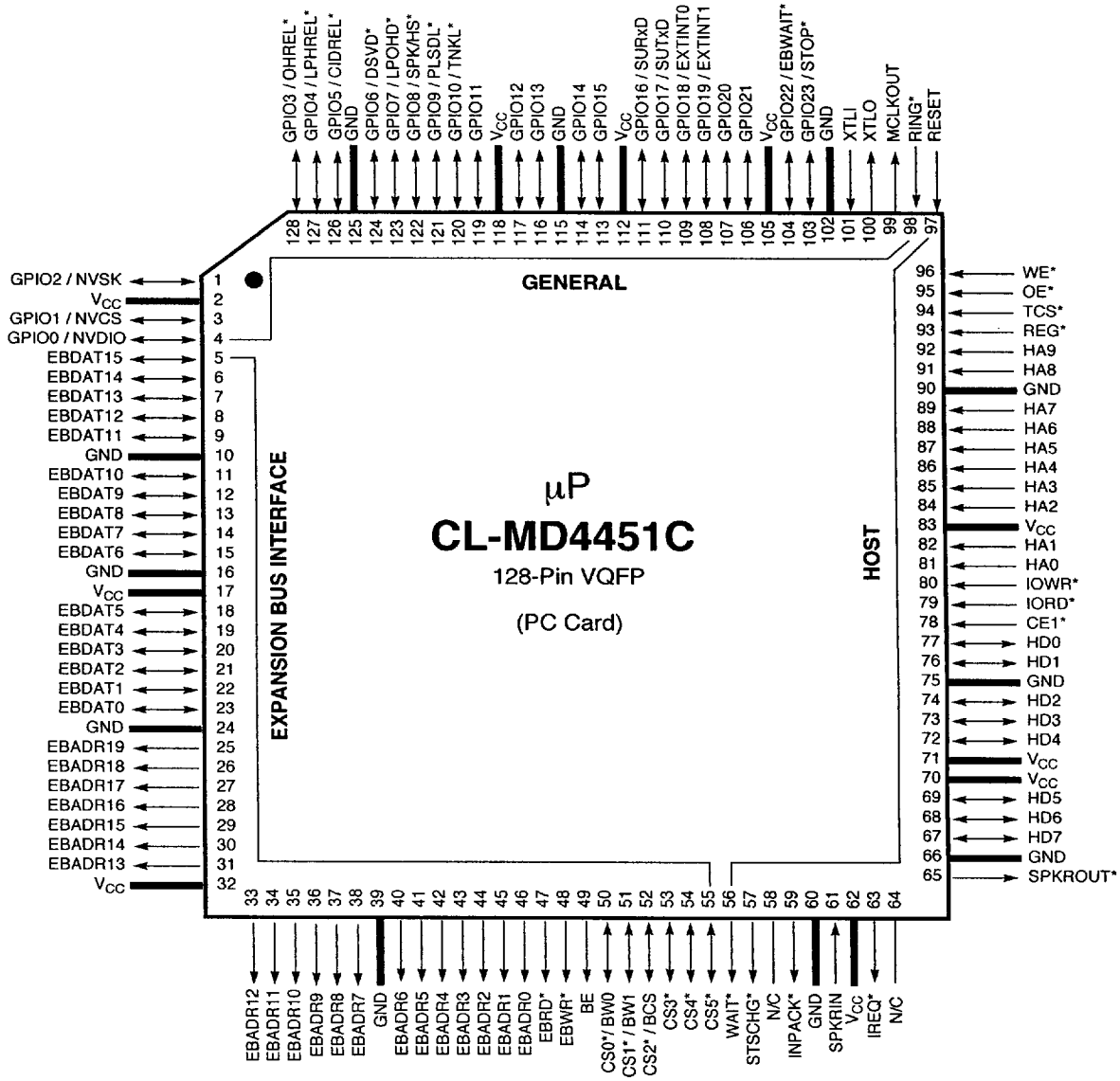
6.1.1 μP Parallel and Plug-and-Play (128-pin SQFP) Pin Diagram



6.1.2 µP Serial Pin Diagram (128-pin SQFP)

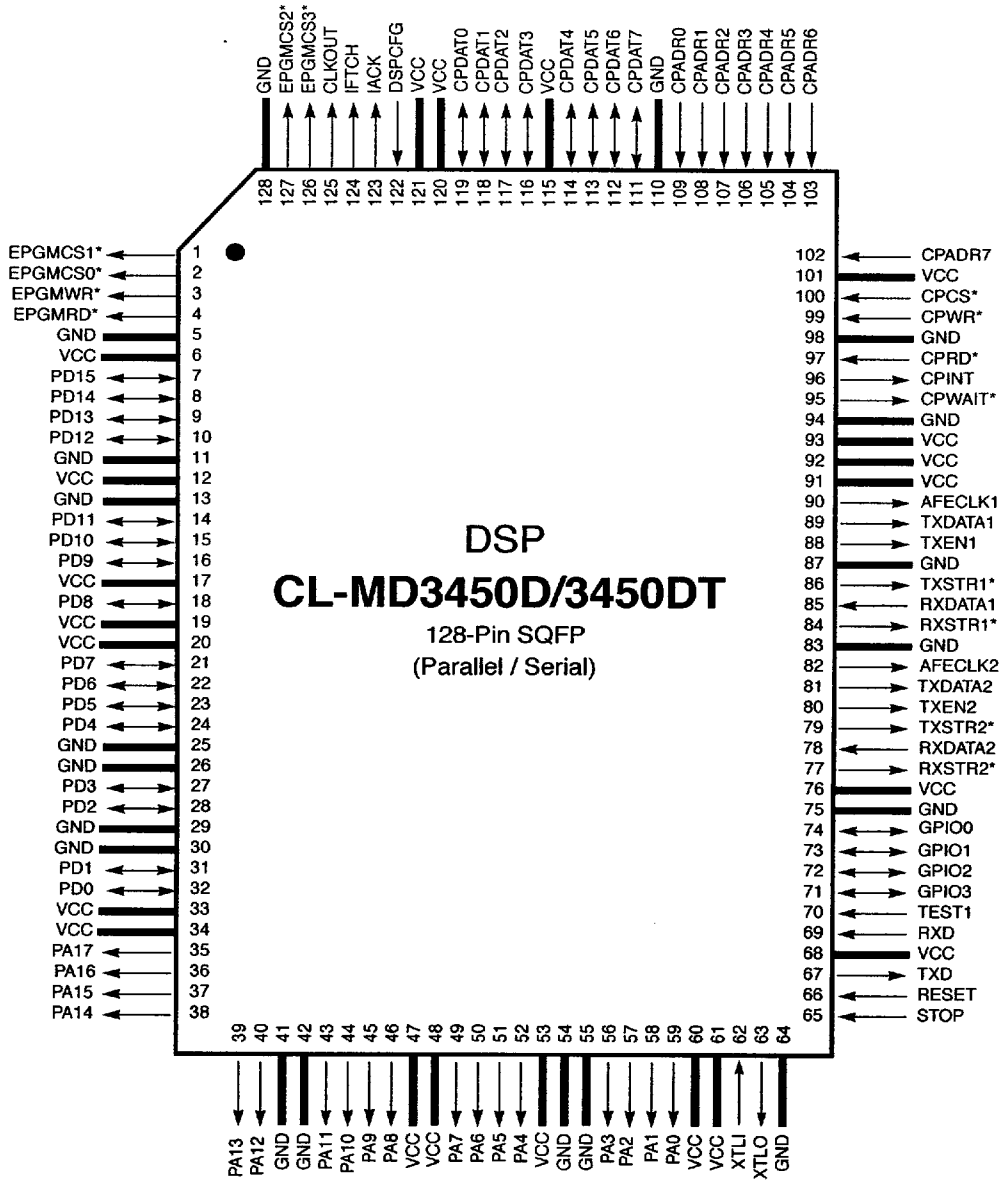


6.1.3 µP PC Card (PCMCIA) Pin Diagram (128-pin VQFP)

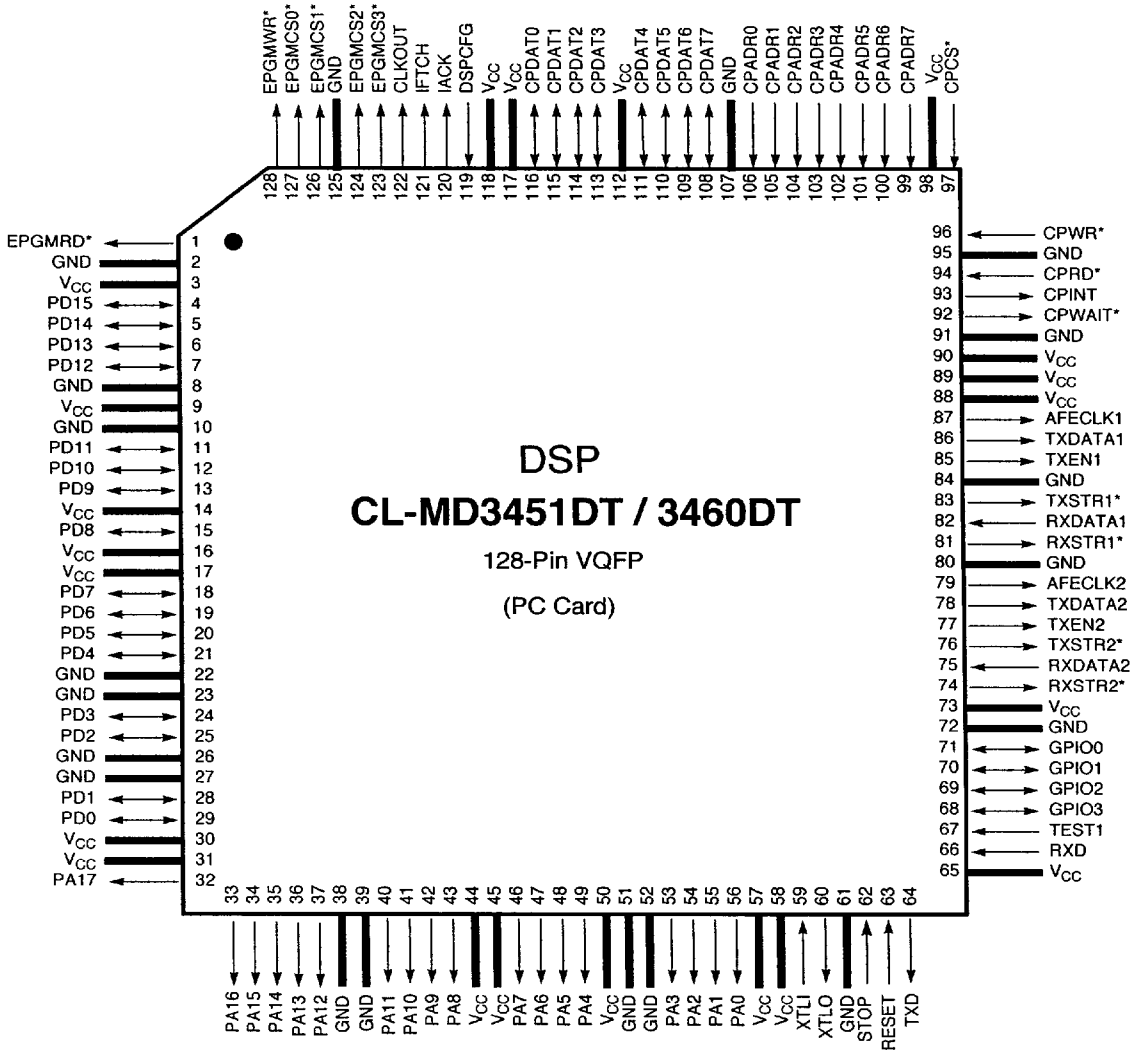


6.2 Digital Signal Processor (DSP) Pin Diagrams

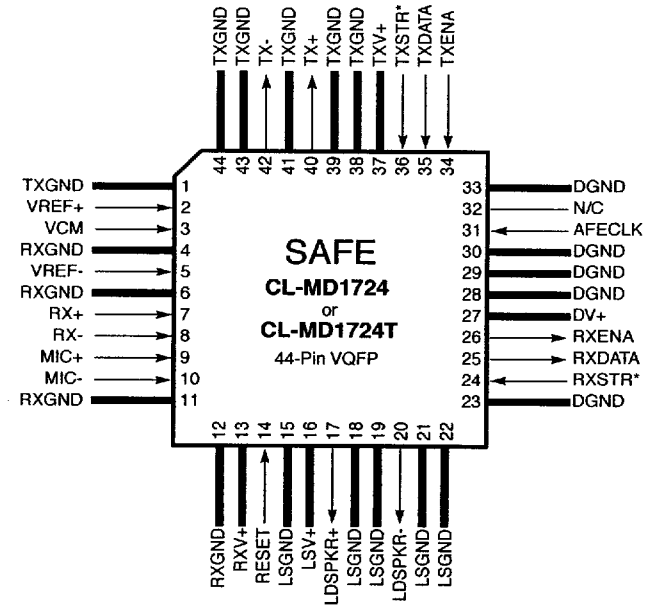
6.2.1 DSP CL-MD3450D/3450DT Pin Diagram (128-pin SQFP)



6.2.2 DSP PC Card CL-MD3451DT / 3460DT Pin Diagram (128-pin VQFP)



6.3 SAFE Pin Diagram (44-pin VQFP)



7. PIN DESCRIPTIONS

7.1 Microprocessor (μP) Pin Description

This section describes the microprocessor hardware pins. The following conventions are used in the pin assignment tables: (*) denotes an active-low signal (all other pin are active-high); I = input; I/O = input/output; O = output; OD = open-drain output; OT = open-collector output when function enabled and high-impedance when function disabled; GND = ground; AGND = analog ground; and PWR = power supply.

7.1.1 μP Host Interface Pin Descriptions

The function of these pins depends on the signal levels at HOSTSEL[0–1]. The pin requirements for serial interfaces and for ISA parallel and ISA parallel plug-and-play interfaces are provided in Table 7-1 on page 47. The PC Card interfaces use these pins differently (see Section 7.1.1.4 on page 53). Descriptions of the pins are given in the following sections.

Table 7-1. Pin Requirements for a Given Host Interface

Host Interface	µP Pins						
	HOST-SEL1	**HOST-SEL0**	**HCS*/ CACK***	**COM-SEL[0–1]**	**AEN, HA[0–9]**	**GPIO[11–14]/ HA[12–15]**	**GPIO20/ECLED* and GPIO21/TMLED***
Serial See Note 1)	0	0	Con-nected with 47 kΩ resistor	RTS*/ DTR*	HA [0–3] con-nected high	GPIO[11–14] or FAXLED*, VOCLED*, AALED*, HSLED*	GPIO[20–21] or ECLED*, TMLED*
Parallel with plug-and-play (internal address decode) See notes 2), 3) and 4)	0	1	No connect	HA[10–11]	AEN HA[0–9]	HA[12–15]	GPIO[20–21]
Parallel with exter-nal address decode See Note 4)	1	0	HCS*	See Note 5)	HA[0–2] See Note 6)	GPIO[11–14]	GPIO[20–21]
Parallel with inter-nal address decode See notes 3) and 4)	1	1	No connect	COM-SEL[0–1]	AEN, HA[0–9]	GPIO[11–14]	GPIO[20–21]]

NOTES:

1) The GPIO pins can be used as the LED drivers for HSLED*, AALED*, VOCLED*, FAXLED*, ECLED*, and TMLED*. Additional LEDs for off-hook (OH), carrier detect (CD), data terminal ready (TR), modem ready (MR), and DSVD can be connected to the RS-232 signals and the modem relay control signals (OHREL* and DSVD*).
2) For plug-and-play designs, as many as seven host interrupt pins are supported (HINTA–G).

   For plug-and-play designs, ISA HA[10] connects to COMSEL0, HA[11] connects to COMSEL1, and HA[12–15] connect to GPIO[11–14]/HA[12–15]. See the modem configuration utility to configure these pins for Plug-and-Play mode.
3) A single modem board can be designed to support both parallel non-Plug-and-Play mode and parallel Plug-and-Play mode. This is accomplished by connecting HOSTSEL0 through a resistor to V_{CC}. HOSTSEL1 then configures the modem for either Plug-and-Play or non-Plug-and-Play mode.
4) In parallel non-Plug-and-Play mode, all HINT lines [A–G] are connected together. In Plug-and-Play mode, the HINT lines are independent. When one interrupt is enabled, then the rest are tristated.
5) Connect COMSEL[0–1] to either V_{CC} or ground. Do not leave these pins unconnected.
6) Connect HA[0–2] to the PC bus; connect AEN and HA[3–9] pins to V_{CC} or ground. Do not leave these pins unconnected.

7.1.1.1 µP Host Interface Pin Descriptions — Parallel and Plug-and-Play

Symbol	SQFP	Type	Description
HOSTSEL1 / CS5*	59	I/O	**PARALLEL HOST INTERFACE SELECTION**: These pins provide dual functionality. While powering up or during modem reset, these pins are inputs (HOSTSEL0 and HOSTSEL1) and indicate the type of host interface. After the chip reset, these pins become output pins. These output pins can be used as chip selects for external devices. Host interface types include serial, parallel with external address decode, parallel with internal address decode, and parallel plug-and-play with internal address decode. These pins should be connected through a 47-K resistor to V_{CC} or GND. See Table 7-1 on page 47 for more information. OEMs can design a single modem ISA bus board to support both plug-and-play and non-plug-and-play applications. After the chip reset, these pins become external chip selects. The µP then pulls the CS4* or CS5* output pin low when the external address falls within the address range specified in the internal CSCR4 register or CSCR5 register, respectively.
HOSTSEL0 / CS4*	58		
RESET	101	I	**µP RESET**: The modem gets reset when this pin is pulled high. After the low-to-high transition, the RESET input pin signal must be high for at least 10 µs before the signal drops low. The modem requires 200 ms to initialize all modem functions before receiving any AT commands.
AEN	97	I	**PARALLEL ADDRESS ENABLE**: In Parallel mode, this pin is used for host address enable.
IOCHRDY	60	OD	**IOCHRDY**: This pin provides a wait-stated output for data, control, and status information reads and writes to the modem UART. This output can sink up to 20 mA.
HRD*	83	I	**HOST READ**: In any mode, if the chip is correctly addressed and if HRD* is low, the host can read the data, control, and status information from the selected UART registers.
HA[0–9]	85, 86, 88 89, 90, 91 92, 93, 95, 96	I	**HOST ADDRESS LINES [0–9]**: Pins HA 0–9 are used as host address lines 0–9. Host address lines 0–2 also are used to select the UART interface registers. For plug-and-play designs, ISA HA10 connects to COMSELO and HA11 connects to COMSEL1. The functions HA[12–15] connect to GPIO[11–14]/HA[12–15]. For more information about HA[12–15], see Table 7-1 on page 47 and the general pin descriptions starting on page 59.

7.1.1.1 µP Host Interface Pin Descriptions — Parallel and Plug-and-Play (cont.)

Symbol	SQFP	Type	Description
COMSEL0 / HA10	99	I	**COM PORT SELECTION LINES 0 & 1/ HOST ADDRESS LINES 10 & 11**: The function of the COMSEL0 and COMSEL1 pins are controlled by HOSTSEL0 and HOSTSEL1 input pins. In Parallel mode with both HOSTSEL0 and HOSTSEL1 high, the states of COMSEL0 and COMSEL1 are used to select a COM port. For plug-and-play designs, ISA HA10 connects to COMSELO and HA11 connects to COMSEL1. The functions HA[12–15] connect to GPIO[11–14]/HA[12–15]. For more information about HA[12–15], see Table 7-1 on page 47 and the general pin descriptions starting on page 59.
COMSEL1 / HA11	100	I	

HA[9:0]	COM Port	COMSEL1	COMSEL0
3F8–3FF	1	0	0
2F8–2FF	2	0	1
3E8–3EF	3	1	0
2E8–2EF	4	1	1

HCS* / CACK*	82	I/O	**HOST CHIP SELECT / CHIP ACKNOWLEDGE**: When configured for parallel external decode (HOSTSEL[1:0]= 1,0), this input pin provides the chip select for the modem UART interface. A low state on this pin allows the computer to read from or write to the UART interface registers. When the modem is configured for a serial interface, this pin should be connected to V_{CC} through a 47-K resistor. Additionally, when the modem is configured for the Plug-and-Play mode (HOSTSEL[1:0] = 0, 1) and parallel internal decode (HOSTSEL[1:0] = 1, 1), this pin behaves as an output. When the chip is accessed, this pin is asserted low. In Parallel and Plug-and-Play modes, this pin can be used for decoding purposes.
HWR*	84	I	**HOST WRITE**: In any mode, if the chip is correctly addressed and if HWR* is low, the host can write control information or data to the selected UART registers.

7.1.1.1 μP Host Interface Pin Descriptions — Parallel and Plug-and-Play (cont.)

Symbol	SQFP	Type	Description
HINTA	67	OT	**HOST INTERRUPT / HOST INTERRUPT A**: When enabled, this signal goes high whenever certain bits change within the UART registers. There are four possible interrupt sources that may be enabled or disabled using the UART IER register: receiver data available, transmitter holding register empty, receiver line status, and modem line status. The UART interface automatically drops the HINT signal level whenever the host performs the appropriate action for the interrupt source. When disabled, this output is in a high-impedance state. In Parallel Plug-and-Play mode, this function can be selected from up to seven interrupt output pins (HINTA–G) as the ISA bus HINT signal (that is, only one HINT output can be used at a time). In non-Plug-and-Play modes, HINTA–G are shorted together and are all asserted before the modem interrupts the host. This output can sink up to 20 mA.
HINTB HINTC HINTD HINTE HINTF HINTG	68 69 65 63 62 61	OT	**HOST INTERRUPTS (B–G)**: In Parallel Plug-and-Play mode, seven interrupt outputs are provided (A–G). Any one of these pins can be selected as the ISA bus HINT signal, but only one output is selected at a time. This feature permits a board to be designed that allows the end user to select the COM port IRQ from a list of seven different IRQs (IRQ7 to IRQ0). In non-Plug-and-Play modes, HINTA–G are shorted together and are all asserted when the modem interrupts the host. When enabled, the selected HINT signal goes high whenever certain bits change within the UART registers. There are four possible interrupt sources that may be enabled or disabled using the UART IER register: receiver data available, Transmitter Holding register empty, receiver line status, and modem line status. The UART interface automatically drops the HINT signal level whenever the host performs the appropriate action for the interrupt source. When disabled, this output is in a high-impedance state. This output can sink up to 20 mA.
HD[0–7]	81, 80 78:76 73:71	I/O	**PARALLEL DATA BUS LINES [0–7]**: These pins are used for the host data bus lines 0–7.
TCS*	98	I	**MANUFACTURING TEST PIN**: This pin is used during Cirrus Logic manufacturing for testing purposes. This pin should be pulled up to V_{CC} through a 47-kΩ resistor for all applications.

7.1.1.2 µP Host Interface Pin Descriptions — Serial

Some of the GPIO pins can be used as LED drivers for HSLED*, AALED*, VOCLED*, FAXLED*, ECLED*, and TMLED*. Additional LEDs for OH (off-hook), CD (carrier detect), TR (data terminal ready), MR (modem ready), and DSVD can be connected to the RS-232 signals and the modem relay control signals (OHREL* and DSVD*).

Symbol	SQFP	Type	Description
HOSTSEL1 / CS5* HOSTSEL0 / CS4*	59 58	I/O	**PARALLEL/SERIAL HOST INTERFACE SELECTION**: These pins serve dual functions. During powering up or modem reset, these pins are inputs (HOSTSEL0 and HOSTSEL1) and indicate the type of host interface. After the chip reset, these pins become external output chip selects. Host interface types include serial, parallel with external address decode, parallel with internal address decode, and parallel plug-and-play with internal address decode. For a serial host interface, both HOSTSEL0 and HOSTSEL1 should be connected through a 47-K resistor to GND. See Table 7-1 on page 47 for more information. After the µP initialization process, these pins become external chip selects. The µP then pulls the CS4* or CS5* output pin low when the external address falls within the address range specified in the internal CSCR4 or CSCR5 register, respectively.
RESET	101	I	**µP RESET**: The modem gets reset when this pin is pulled high. After the low-to-high transition, the RESET input pin signal must be high for at least 10 µs before the signal drops low. The modem requires 200 ms to initialize all modem functions before receiving any AT commands.
RTS*	99	I	**SERIAL REQUEST TO SEND**: In Serial mode, a low signal informs the modem that the DTE is ready to send data on TXD.
DTR*	100	I	**SERIAL DATA TERMINAL READY**: When this signal is low, it informs the modem that the DTE is ready to establish a communication link.
RXD	90	O	**SERIAL RECEIVE DATA**: In Parallel mode or Plug-and-Play mode, this pin is used for host address line 4. In Serial mode, this is the serial data output to the DTE.
RI*	95	O	**SERIAL RING INDICATOR**: When low in Serial mode, this signal informs the DTE that the modem has received a valid ring signal.
DSR*	93	O	**SERIAL DATA SET READY**: WHen low in Serial mode, this signal informs the DTE that the modem is ready to establish a communication link.

7.1.1.2 µP Host Interface Pin Descriptions — Serial (cont.)

Symbol	SQFP	Type	Description
TXD	96	I	**SERIAL TRANSMIT DATA**: In Serial mode, this signal is the serial data input from the DTE.
CTS*	92	O	**SERIAL CLEAR TO SEND**: When low in Serial mode, this signal informs the DTE that the modem is ready to receive data on TXD.
DCD*	91	O	**SERIAL DATA CARRIER DETECT**: When low in Serial mode, this signal informs the DTE that the modem has detected the remote modem data carrier.
RESERVED	60	OD	**RESERVED**: This pin is reserved. It should be left unconnected.
RESERVED	82, 83 84	I	**RESERVED**: These pins are reserved. They should be connected to V_{CC} through a 47-kΩ resistor.
RESERVED	81, 80 76–78, 71–73	I/O	**RESERVED**: These pins are reserved. They should be left unconnected.
RESERVED	85, 86 88, 89	I	**RESERVED**: These pins are reserved. They should be connected to V_{CC} through a 47-kΩ resistor.
RESERVED	97	I	**RESERVED**. This pin is reserved for future enhancements of the chipset and should be left unconnected.
N/C	61–63 65, 67–69	–	**NO CONNECT**: These pins should be left floating.
TCS*	98	I	**MANUFACTURING TEST PIN**: This pin is used during manufacturing for testing purposes. This pin should be pulled up to V_{CC} through a 47-kΩ resistor for all applications.

7.1.1.3 µP Power Pin Descriptions — Parallel/Plug-and-Play and Serial

Symbol	SQFP	Type	Description
VCC	6, 21 36, 66 74, 75 87, 109 116, 122	PWR	**+5-V POWER SUPPLY**: The µP requires only +5 V to perform all digital processing.
GND	1, 14 20, 28 43, 64 70, 79 94, 106 119	GND	**DIGITAL GROUND.**

7.1.1.4 µP Host Interface Pin Descriptions — PC Card (PCMCIA)

Symbol	VQFP	Type	Description
CS5* CS4*	55 54	I/O	**CHIP SELECTS 4 and 5**: After the µP initialization process, these pins becomes external chip selects. The µP then pulls the CS4* or CS5* output pin low when the external address falls within the address range specified in the internal CSCR4 or CSCR5 register, respectively. CS5* should be connected to V_{CC} through a 10-kΩ resistor. CS4* should be connected to ground through a 10-kΩ resistor.
RESET	97	I	**µP RESET**: The modem gets reset when this pin is pulled high. After the low-to-high transition, the RESET input pin signal must be high for at least 10 µs before the signal drops low. The modem requires 200 ms to initialize all modem functions before CE1 or CE2 be can asserted. After a reset, the host computer needs to configure the PC Card interface, since the modem card will be in an unconfigured state following a reset. An internal resistor-capacitor circuit causes the modem to be reset during a hot insertion (that is, when the computer power is on during installation of the PC Card).
WAIT*	56	O	**WAIT***: This pin provides a wait-stated output (similar to IOCHRDY for the ISA bus) for data, control, and status information while reading and writing to the modem's UART. This signal is asserted to delay the completion of read/write accesses to the chip from the host. The access could be either for OE*/WE* or IORD*/IOWR*. This output pin can sink up to 20 mA.
CE1*	78	I	**CARD ENABLE EVEN ADDRESS**: When CE1* and REG* are low, a low input signal at IORD*, IOWR*, OE*, or WE* allows the host to read or write to the modem's UART and configuration registers or to read the PC Card CIS.
HA[9:0]	92, 91 89:84 82, 81	I	**HOST ADDRESS LINES [9:0]**: Host address lines 9:0 are used to select the UART interface registers and the PC Card's CIS and configuration registers.
HD[0–7]	77, 76 74:72 69:67	I/O	**HOST DATA BUS LINES [0–7]**: These eight data bus lines are used to read from or write to the modem's UART and PC Card's CIS configuration registers or to read the PC Card's CIS.
INPACK*	59	O	**INPUT ACKNOWLEDGE**: This output signal will be asserted by the modem if the modem is selected and can respond to an I/O read cycle. This signal is inactive until configured within the modem's PC Card interface registers.

7.1.1.4 µP Host Interface Pin Descriptions — PC Card (PCMCIA) (cont.)

Symbol	VQFP	Type	Description
IREQ*	63	O	**HOST INTERRUPT**: When the PC Card's COR (Configuration Option register) CARD EN bit is set to '1', the interrupt structure is compatible with a 16C450/16C550 UART. When enabled by the appropriate UART bits, this signal goes low whenever certain bits change within the UART registers. There are four possible interrupt sources that can be enabled or disabled using the UART IER register: receiver data available, Transmitter Holding register empty, receiver line status, and modem line status. The UART interface automatically de-asserts the IREQ* signal level whenever the host performs the appropriate action for the interrupt source. This output can sink up to 20 mA.
OE*	95	I	**OUTPUT ENABLE**: When OE*, REG*, and CE1* are low, the host can read data from the PC Card CIS or card configuration registers.
IORD*	79	I	**HOST READ**: In any mode, if the chip is correctly addressed and if IORD* is low, the host can read the data, control, and status information from the selected UART registers.
IOWR*	80	I	**HOST WRITE**: In any mode, if the chip is correctly addressed and if IOWR* is low, the host can write control information or data to the selected UART registers.
WE*	96	I	**WRITE ENABLE**: When WE*, REG*, and CE1* are low, the host can write to the PC Card Configuration registers.
REG*	93	I	**ATTRIBUTE MEMORY SELECT**: When REG* and CE1* are low, a low input signal at IORD*, IOWR*, OE*, or WE* allows the host to read or write to the modem UART and PC Card Configuration registers or to read from the PC Card's CIS.
SPKROUT*	65	O	**DIGITAL SPEAKER OUTPUT**: When Audio Enable AUDIO is set to '1', the digital input signal at SPKRIN is transferred to SPKROUT*. Audio Enable is bit 3 in the Card Configuration Status register (CCSR). This signal is inactive until the card is configured.
SPKRIN	61	I	**DIGITAL SPEAKER INPUT**: The audio signal from the SAFE LDSPKR+ output pin should be connected to the SPKRIN pin. This digital signal is then connected to the SPKROUT* pin when the Card Configuration Status register (CCSR) Audio Enable bit (AUDIO) is set to '1'.

7.1.1.4 µP Host Interface Pin Descriptions — PC Card (PCMCIA) (cont.)

Symbol	VQFP	Type	Description
STSCHG*	57	O	**STATUS CHANGE**: This signal indicates that the modem's ring has been detected, provided that ringing is enabled and follows the new extended status register's protocol. This signal is inactive (high) until configured.
NO CONNECT	58 64	– –	**NO CONNECT**: These pins should be left floating.
TCS*	94	I	**MANUFACTURING TEST PIN**: This pin is used during Cirrus Logic manufacturing for testing purposes. This pin should be pulled up to V_{CC} through a 47-KΩ resistor for all applications.

7.1.1.5 µP Power Pin Descriptions — PC Card (PCMCIA)

Symbol	VQFP	Type	Description
V_{CC}	2, 17 32, 62 70, 71 83, 105 112, 118	PWR	**+5-V POWER SUPPLY**: The µP requires only +5 V to perform all digital processing.
GND	10, 16 24, 39 60, 66 75, 90 102, 115 125	GND	**DIGITAL GROUND**.

7.1.2 μP General Pin Descriptions

The V.34+ FastPath family provides 24 general-purpose pins that can be assigned by the modem firmware configuration utility to be either general purpose input/output pins, special function pins (for example, STOP*) or pin-functions (for example, LPHREL*). Pin-functions are functions that are relocatable to any one of the 24 general-purpose pins. These pin-functions include **LPHREL***, **OHREL***, **CIDREL***, **DSVD***, **LPOHD***,**SPK/HS***, **PLSDL***, **TNKL***, **NVSK**, **NVCS**, and **NVDIO**. Some functions require the use of multiple pin-functions (for example, using an NVRAM requires NVSK, NVCS, and NVDIO). Some of the GPIO pins can be used to drive LED circuits for common functions like AA (autoanswer) or HS (high speed). The selection of GPIOs is controlled by the modem μP's configuration utility. The default pin function assignments are listed below.

Symbol	SQFP	VQFP	Type	Description
GPIO0 / NVDIO	8	4	I/O	**GENERAL-PURPOSE I/O 0 / NON-VOLATILE RAM SERIAL DATA INPUT/OUTPUT:** This pin can be configured as a general-purpose I/O or as NVDIO. When configured for NVDIO, this pin receives the serial data stream from the NVRAM's DO pin and transmits the serial data stream into the NVRAM's DI pin. The NVDIO function can be relocated to any GPIO line by the configuration utility.
GPIO1 / NVCS	7	3	I/O	**GENERAL-PURPOSE I/O 1 / NON-VOLATILE RAM CHIP SELECT**: This pin can be configured as a general-purpose I/O or as NVCS. When configured for NVCS, this output pin provides the NVRAM chip select for reading and writing to the NVRAM. This signal should be connected to the NVRAM's CS pin. The NVCS function can be relocated to any GPIO line by the configuration utility.
GPIO2 / NVSK	5	1	I/O	**GENERAL-PURPOSE I/O 2 / NON-VOLATILE RAM SHIFT CLOCK**: This pin can be configured as a general-purpose I/O or as NVSK. When configured for NVSK, this output pin provides the clock for the NVRAM's serial data stream. This pin should be connected to the NVRAM's SK pin. The NVSK function can be relocated to any GPIO line by the configuration utility.

7.1.2 µP General Pin Descriptions (cont.)

Symbol	SQFP	VQFP	Type	Description
GPIO3 / OHREL*	4	128	I/O	**GENERAL-PURPOSE I/O 3 / OFF-HOOK RELAY CONTROL**: This pin can be configured as a general-purpose I/O or as OHREL*. When configured for OHREL*, this pin is used to control a relay connected to the telephone line. This output can sink up to 10 mA for a normally open relay. The OHREL* function can be relocated to any GPIO line by the configuration utility.
GPIO4 / LPHREL*	3	127	I/O	**GENERAL-PURPOSE I/O 4 / VOICE RELAY CONTROL**: This pin can be configured as a general-purpose I/O or as LPHREL*. The LPHREL* function is used to control a relay for recording and playing back a voice message through the local telephone. This output can sink up to 10 mA. The LPHREL* function can be relocated to any GPIO line by the configuration utility.
GPIO5 / CIDREL*	2	126	I/O	**GENERAL-PURPOSE I/O 5 / CALLER ID RELAY CONTROL** : This pin can be configured as a general-purpose I/O or as CIDREL*. When configured as CIDREL*, this output signal can control a relay for receiving Caller ID. This output can sink up to 10 mA and powers up as a high signal. The CIDREL* function can be relocated to any GPIO line by the configuration utility.
GPIO6 / DSVD*	128	124	I/O	**GENERAL-PURPOSE I/O 6 / DIGITAL SIMULTANEOUS VOICE AND DATA***: This pin can be configured as a general-purpose I/O or as DSVD*. When configured for DSVD*, this pin provides one of the several necessary relay controls for DSVD operation. The DSVD* function can be relocated to any GPIO line by the configuration utility.

7.1.2 µP General Pin Descriptions (cont.)

Symbol	SQFP	VQFP	Type	Description
GPIO7 / LPOHD*	127	123	I/O	**GENERAL-PURPOSE I/O 7 / LOCAL PHONE OFF-HOOK DETECT***: This pin can be configured as a general-purpose I/O or as LPOHD*. When configured for LPOHD*, this signal indicates the on-hook or off-hook condition of the local phone. When high, this indicates that the local phone is on-hook. When low, this indicates that the local phone is off-hook. The LPOHD* function can be relocated to any GPIO line by the configuration utility.
GPIO8 / SPK/HS*	126	122	I/O	**GENERAL-PURPOSE I/O 8 / SPEAKER/HEADSET*** : This pin can be configured as a general-purpose I/O or as SPK/HS*. When configured for SPK/HS*, this signal selects between the speaker and the headset. When high, the external speaker is used. When low, the headset speaker is used. The SPK/HS* function can be relocated to any GPIO line by the configuration utility.
GPIO9 / PLSDL*	125	121	I/O	**GENERAL-PURPOSE I/O 9 / PULSE DIAL*** : This pin can be configured as a general-purpose I/O or as PLSDL*. When configured for PLSDL*, this signal is used to do pulse dialing for some European applications. The PLSDL* function can be relocated to any GPIO line by the configuration utility.
GPIO10 / TNKL*	124	120	I/O	**GENERAL-PURPOSE I/O 10 / TINKLE*** : This pin can be configured as a general-purpose I/O or as TNKL*. When configured for TNKL*, this signal is used to suppress bell tinkling in some European applications. The TNKL* function can be relocated to any GPIO line by the configuration utility.

7.1.2 µP General Pin Descriptions (cont.)

Symbol	SQFP	VQFP	Type	Description
GPIO11 / HA12 / FAXLED*	123	119	I/O	**GENERAL-PURPOSE I/O 11 / HOST ADDRESS LINE 12 / FAXLED***: This pin can be configured as a general-purpose I/O for the parallel, serial, and PC Card chips. It can additionally be configured as host address line 12 for Plug-and-Play mode or as FAXLED* for serial mode. When configured for FAXLED*, a low signal indicates that the modem is in Fax mode. For plug-and-play information, see Table 7-1 on page 47. In Serial mode, the FAXLED* function can be relocated to any GPIO line by the configuration utility.
GPIO12 / HA13 / VOCLED*	121	117	I/O	**GENERAL-PURPOSE I/O 12 / HOST ADDRESS LINE 13 / VOCLED***: This pin can be configured as a general-purpose I/O for the parallel, serial, and PC Card chips. It can additionally be configured as host address line 13 for Plug-and-Play mode or as VOCLED* for serial mode. When configured for VOCLED*, a low signal indicates that the modem is in Voice mode. For plug-and-play information, see Table 7-1 on page 47. In Serial mode, the VOCLED* function can be relocated to any GPIO line by the configuration utility.
GPIO13 / HA14 / AALED*	120	116	I/O	**GENERAL-PURPOSE I/O 13 / HOST ADDRESS LINE 14 / AALED***: This pin can be configured as a general-purpose I/O for the parallel, serial, and PC Card chips. It can additionally be configured as host address line 14 for Plug-and-Play mode or as AALED* for Serial mode. When configured for AALED*, a low signal indicates that the modem is configured for Auto-answer mode (that is, **ATS0** is a non-zero value). For plug-and-play information, see Table 7-1 on page 47. In Serial mode, the AALED* function can be relocated to any GPIO line by the configuration utility.

7.1.2 µP General Pin Descriptions (cont.)

Symbol	SQFP	VQFP	Type	Description
GPIO14 / HA15 / HSLED*	118	114	I/O	**GENERAL-PURPOSE I/O 14 / HOST ADDRESS LINE 15 / HSLED***: This pin can be configured as a general-purpose I/O for the parallel, serial, and PC Card chips. It can additionally be configured as host address line 15 for Plug-and-Play mode or as HSLED* for Serial mode. When configured for HSLED*, a low signal indicates that the data modem connection rate is 19,200 bps or above or that the fax modem data rate is 14,400 bps. For plug-and-play information, see Table 7-1 on page 47. In Serial mode, the HSLED* function can be relocated to any GPIO line by the configuration utility.
GPIO15	117	113	I/O	**GENERAL-PURPOSE I/O 15** : This pin can be configured as a general-purpose I/O.
GPIO16 / SURxD	115	111	I/O	**GENERAL-PURPOSE I/O 16 / SOFT UART RECEIVE DATA** This pin can be configured as a general-purpose I/O or as SURxD. When configured for SURxD, this pin provides an RXD signal for extra channels of communication.
GPIO17 / SUTxD	114	110	I/O	**GENERAL-PURPOSE I/O 17 / SOFT UART TRANSMIT DATA**: This pin can be configured as a general-purpose I/O or as SUTxD. When configured for SUTxD, this pin provides a TXD signal for extra channels of communication.
GPIO18 / EXTINT0	113	109	I/O	**GENERAL-PURPOSE I/O 18 / EXTERNAL INTERRUPT INPUT 0**: This pin can be configured as a general-purpose I/O or as EXTINT0. EXTINT0 can be used to generate a µP internal interrupt. This input pin can be programmed to be positive, negative, or both edges, or the pin can be sensitive to high or low levels. When an interrupt has been generated, the µP can be programmed to provide an interrupt acknowledge on the GPIO20 output. This pin should be configured as a general-purpose pin when the EXTINT0 function is not being used.

7.1.2 µP General Pin Descriptions (cont.)

Symbol	SQFP	VQFP	Type	Description
GPIO19 / EXTINT1	112	108	I/O	**GENERAL-PURPOSE I/O 19 / EXTERNAL INTERRUPT INPUT 1**: This pin can be configured as a general-purpose I/O or as EXTINT1. EXTINT1 can be used to generate a µP internal interrupt. This input pin can be programmed to be positive, negative, or both edges, or the pin can be sensitive to high or low levels. When an interrupt has been generated, the µP can be programmed to provide an interrupt acknowledge on the GPIO21 output. This pin should be configured as a general-purpose pin when the EXTINT1 function is not being used.
GPIO20 / ECLED*	111	107	I/O	**GENERAL-PURPOSE I/O 20 / ECLED*** : This pin can be configured as a general-purpose I/O or as ECLED* for Serial mode. When configured for ECLED*, a low signal indicates that the modem is in Error Correction/Data Compression mode. In Serial mode, the ECLED* function can be relocated to any GPIO line by the configuration utility.
GPIO21 / TMLED*	110	106	I/O	**GENERAL-PURPOSE I/O 21 / TMLED***: This pin can be configured as a general-purpose I/O or as TMLED* for Serial mode. When configured for TMLED*, a low signal indicates that the modem is in a test mode (refer to the **&Tn** command). In Serial mode, the TMLED* function can be relocated to any GPIO line by the configuration utility.

7.1.2 µP General Pin Descriptions (cont.)

Symbol	SQFP	VQFP	Type	Description
GPIO22 / EBWAIT*	108	104	I/O	**GENERAL-PURPOSE I/O 22 / EBWAIT*** : This pin can be used as a general-purpose I/O or as EBWAIT*, a wait-stated output used to access the µP expansion bus. EBWAIT* extends the external read/write cycle as long as this signal is asserted. This signal is asserted by the external device, to which an access is currently in progress.
GPIO23 / STOP*	107	103	I/O	**GENERAL-PURPOSE I/O 23 / STOP MODE** : This pin can be configured as a general-purpose I/O or as STOP*. When the pin is configured for STOP*, a high input signal powers up the the chipset. A low input signal places the modem in Stop mode. The low input signal turns off all power usage by the chipset except for some internal control logic. When Stop mode is not needed, this input pin should be pulled up to V_{CC}.
MCLKOUT	103	99	O	**µP CLOCK OUT**: This pin provides a buffered µP clock output signal.
RING*	102	98	I	**RING SIGNAL**: The ring signal from the DAA is fed into this input pin for ring detection.
XTLI XTLO	105 104	101 100	I O	**µP CRYSTAL INPUT AND OUTPUT**: These two pins provide a feedback circuit for generating the chipset's system clock.

7.1.3 µP Expansion Bus Interface Pin Descriptions

Symbol	SQFP	VQFP	Type	Description
EBADR [19:0]	29–35 37–42 44–50	25–31 33–38 40–46	O	**MICROPROCESSOR EXPANSION BUS ADDRESS**: These pins provide the address necessary to access an external peripheral.
EBDAT[15:0]	9–13 15–19 22–27	5–9 11–15 18–23	I/O	**EXPANSION BUS ADDRESS LINES [0–15]**: These 16 data bus lines are used to read from or write to external memory or devices.
EBRD*	51	47	O	**EXPANSION BUS READ LINE**: The microprocessor sets this signal low when it reads from an external device.
EBWR*	52	48	O	**EXPANSION BUS WRITE LINE**: The microprocessor sets this signal low when it writes to an external device.
BE	53	49	O	**BYTE ENABLE**: The microprocessor sets this pin high when it accesses a byte from the external peripheral. This pin is low for all other data sizes.
CS0*/BW0	54	50	I/O	**CHIP SELECT 0 / BUS WIDTH 0**: This pin provides dual functionality. During powering up or modem reset, this pin is an input and indicates the expansion bus data bus width (BW0 and BW1). After the chip reset, this pin becomes an external chip select. The µP will then pull this output pin low when the external address falls within the address range specified in the internal CSCR0 register. This pin should be tied through a 10-K (or larger) resistor to either V_{CC} or GND, as defined by BW0 and BW1. BW1 latch will impact the GPPFR0 bit.

BW1	BW0	BUS WIDTH
0	0	8
0	1	16

7.1.3 µP Expansion Bus Interface Pin Descriptions (cont.)

Symbol	SQFP	VQFP	Type	Description
CS1* / BW1	55	51	I/O	**CHIP SELECT 1 / BUS WIDTH 1**: This pin provides dual functionality. During powering up or modem reset, this pin is an input and indicates the expansion bus data bus width (BW0 and BW1). After the chip reset, this pin becomes an external chip select. The µP will then pull this output pin low when the external address falls within the address range specified in the internal CSCR1 register. This pin should be connected to GND through a 10-K (or larger) resistor. See CS0*/BW0 for more information.
CS2* / BCS	56	52	I/O	**CHIP SELECT 2 / BOOT CHIP SELECT**: This pin provides dual functionality. During powering up or modem hardware reset, this pin is an input (BCS) and indicates whether chip select CS0 (turbo) or CS1 (normal) is used to start execution of the µP firmware. 1 = CS0, CS0 starts at 0h, and CS1 is defaulted to 80000h 0 = CS1,CS1 starts at 0h, and CS0 is disabled. After the chip reset, this pin becomes an external chip select. The µP will then pull this output pin low when the external address falls within the address range specified in the internal CSCR2 register. This pin should be connected through a 10-K resistor to either V_{CC} or GND based on BCS.
CS3*	57	53	I/O	**CHIP SELECT 3**: After the chip reset, this pin becomes an external chip select. The µP will then pull this output pin low when the external address falls within the address range specified in the internal CSCR3 register. This pin should be connected through a 47-K resistor to V_{CC}.

7.2 DSP Pin Descriptions

7.2.1 DSP Program Memory Interface Pin Descriptions

Symbol	SQFP	VQFP	Type	Description
PA[17:0]	35–40 43–46 49–52 56–59	32–37 40–43 46–49 53–56	O	**PROGRAM MEMORY ADDRESS BUS**: These pins provide the addresses necessary to address an external peripheral. Leave unconnected during normal setup.
PD[15:0]	7–10 14–16 18 21–24 27,28 31,32	4–7 11–13 15 18–21 24, 25 28, 29	I/O	**PROGRAM MEMORY DATA BUS**: These pins are used to read from or write to external memory or devices. Leave unconnected during normal setup.
EPGMCS0*	2	127	O	**EXTERNAL PROGRAM MEMORY CHIP SELECT 0:** This chip select is asserted (active low) when the chip is accessing external memory. The memory space for this chip select is configured through the DSP internal MCON and CCON registers. When not in use, leave this pin unconnected.
EPGMCS1*	1	126	O	**EXTERNAL PROGRAM MEMORY CHIP SELECT 1:** This chip select is asserted (active low) when the chip is accessing external memory. The memory space for this chip select is configured through the DSP internal MCON and CCON registers. When not in use, leave this pin unconnected.
EPGMCS2*	127	124	O	**EXTERNAL PROGRAM MEMORY CHIP SELECT 2:** This chip select is asserted (active low) when the chip is accessing external memory. The memory space for this chip select is configured through the DSP internal MCON and CCON registers. When not in use, leave this pin unconnected.
EPGMCS3*	126	123	O	**EXTERNAL PROGRAM MEMORY CHIP SELECT 3:** This chip select is asserted (active low) when the chip is accessing external memory. The memory space for this chip select is configured through the DSP's internal MCON and CCON registers. When not in use, leave this pin unconnected.

7.2.1 DSP Program Memory Interface Pin Descriptions (cont.)

Symbol	SQFP	VQFP	Type	Description
EPGMRD*	4	1	O	**EXTERNAL PROGRAM MEMORY READ ENABLE:** This signal is asserted low when the DSP is reading from the external program memory. When DSP is executing from internal program memory, this pin can be programmed to display an internal program memory read signal for debugging purposes. Leave unconnected during normal setup.
EPGMWR*	3	128	O	**EXTERNAL PROGRAM MEMORY READ ENABLE:** This signal is asserted low when the DSP is writing to the external program memory. When DSP is executing from internal program memory, this pin can be programmed to display an internal program memory write signal for debugging purposes. Leave unconnected during normal setup.
IFTCH	124	121	O	**INSTRUCTION FETCH**: This pin is used for diagnostic testing and indicates when the DSP is performing an instruction fetch. A high signal indicates an instruction fetch. This pin should be left unconnected for all modem designs.
IACK	123	120	O	**INTERRUPT ACKNOWLEDGE**: This output pin indicates when the DSP bus transaction is an interrupt acknowledge transaction. Leave unconnected during normal setup.
DSPCFG	122	119	I	**DSP CONFIGURATION**: During power-on or DSP hardware reset, the signal at this pin indicates whether the DSP will boot from internal memory or external memory. When DSPCFG is low, the DSP will boot from external program memory address at 0 FFFFh. When DSPCFG is high, the DSP will boot from internal program memory address at 0 0800h or 0 FFFFh, depending on the DSP internal CP logic control register bit. Connect this pin high in a normal setup.
CLKOUT	125	122	O	**CLOCK OUT**: This pin provides a buffered DSP clock output signal when enabled through BCON.

7.2.2 DSP Control Processor (CP) Interface Pin Descriptions

Symbol	SQFP	VQFP	Type	Description
CPADR[7:0]	102–109	99–106	I	**CONTROL PROCESSOR ADDRESS LINES [0–7]:** These pins are used for the DSP control processor interface registers address lines 0-7.
CPDAT[7:0]	111–114 116–119	108–111 113–116	I/O	**CONTROL PROCESSOR DATA BUS LINES [0–7]:** These pins are used for the DSP control processor interface registers data bus lines 0-7.
CPCS*	100	97	I	**CONTROL PROCESSOR CHIP SELECT**: This input pin provides a chip select for the DSP control processor interface registers. A low state on this pin allows the control processor (µP) to read from or write to the control processor interface registers.
CPRD*	97	94	I	**CONTROL PROCESSOR READ**: In any mode, if the chip is correctly addressed and if CPRD* and CPCS* are low, the control processor (µP) can read the data, control, and status information from the selected DSP control processor interface registers.
CPWR*	99	96	I	**CONTROL PROCESSOR WRITE**: In any mode, if the chip is correctly addressed and if CPWR* and CPCS* are low, the control processor (µP) can write control information or data to the selected interface registers.
CPWAIT*	95	92	O	**CONTROL PROCESSOR WAIT**: This pin provides a wait-stated output for data, control, and status information reads and writes to the DSP interface registers. When low, this pin indicates that the CP interface has not finished the CP transaction. This output can sink up to 20 mA.
CPINT	96	93	O	**CONTROL PROCESSOR INTERRUPT**: When enabled, this signal goes high whenever the DSP writes to the CP Interrupt register. The DSP drops the CPINT signal level whenever the host performs the appropriate action for the interrupt source. This output can sink up to 20 mA.

7.2.3 DSP Clock/Reset Interface Pin Descriptions

This group of pins contains UART, general-purpose I/O, and DSP test functions.

Symbol	SQFP	VQFP	Type	Description
TXD	67	64	O	**UART TRANSMIT DATA**: The UART transmits the output data through this register. Leave unconnected if not in use.
RXD	69	66	I	**UART RECEIVE DATA**: The UART receives the input data through this pin. Connect this pin low if not in use.
XTLI XTLO	62 63	59 60	I O	**DSP CRYSTAL INPUT AND OUTPUT:** These two pins provide a feedback circuit for generating the chipset system clock. If used with the µP, the µP's clock output drives XTLI.
RESET	66	63	I	**RESET**: This pin generates a modem reset. This is accomplished by pulsing the signal at the RESET pin from low to high to low. The RESET input pin must be high for at least 10 µs. After the high-to-low transition, the modem requires 200 ms to initialize all modem functions before receiving any AT commands.
STOP	65	62	I	**STOP MODE:** A low-input signal powers up the chipset. A high-input signal places the modem in Stop mode. This effectively turns off all device-set power usage except some internal control logic. When Stop mode is not needed, this input pin should be pulled down to ground.
TEST1	70	67	I	**MANUFACTURING TEST PIN**: This pin is used during Cirrus Logic manufacturing for testing purposes. This pin should be pulled down to ground for all applications.
GPIO[3:0]	71–74	68–71	I/O	**GENERAL-PURPOSE INPUT-OUTPUT:** The DSP provides four general-purpose I/O pins that the µP can use to control or monitor external circuitry. These pins are not currently used for smart modem designs and should be left unconnected.

7.2.4 DSP-SAFE Interface Pin Descriptions

The DSP provides two interfaces for SAFE devices. The CL-MD3450/3451T chipsets with a single SAFE device use interface 1, while the chipsets CL-MD3452/3453T/3462T/3463T with two SAFE devices use interfaces 1 and 2.

Symbol	SQFP	VQFP	Type	Description
AFECLK1 AFECLK2	90 82	87 79	O O	**SAFE CLOCK**: This pin provides the clock source for the SAFE device.
TXDATA1 TXDATA2	89 81	86 78	O O	**TX DATA**: This pin transmits serial data from the DSP to the SAFE device.

7.2.4 DSP-SAFE Interface Pin Descriptions (cont.)

Symbol	SQFP	VQFP	Type	Description
TXEN1 TXEN2	88 80	85 77	O O	**TX ENABLE**: This pin enables the transmittal of data from the DSP to the SAFE device. Polarity is programmable. Reset is active high.
TXSTR1* TXSTR2*	86 79	83 76	O O	**TRANSMIT STROBE**: This pin provides the DSP with the necessary clock signal required to send the serial transmit data from the DSP to the SAFE device. Polarity is programmable. Reset is active low.
RXDATA1 RXDATA2	85 78	82 75	I I	**RX DATA**: Through this pin the DSP receives serial data from the SAFE device.
RXSTR1* RXSTR2*	84 77	81 74	O O	**RECEIVE STROBE**: This pin provides the DSP with the necessary clock signal required to receive the serial receive data from the SAFE device. Polarity is programmable. Reset is active low.

7.2.5 DSP Power Pin Descriptions

Symbol	SQFP	VQFP	Type	Description
V_{CC}	6, 12 17, 19 20, 33 34, 47 48, 53 60, 61 68, 76 91, 92 93, 101 115 120 121	3, 9 14, 16 17, 30 31, 44 45, 50 57, 58 65, 73 88, 89 90, 98 112 117 118	PWR	**+5-V POWER SUPPLY**: The DSP requires only +5 V to perform all digital processing.
GND	5, 11 13, 25 26, 29 30, 41 42, 54 55, 64 75, 83 87, 94 98, 110 128	2, 8 10, 22 23, 26 27, 38 39, 51 52, 61 72, 80 84, 91 95, 107 125	GND	**DIGITAL GROUND.**

7.3 SAFE Pin Descriptions

7.3.1 SAFE General Pin Descriptions

Symbol	VQFP	Type	Description
LDSPKR+ LDSPKR-	17 20	O O	**LOUDSPEAKER OUTPUT**: These pins provide a differential output signal for driving an external loudspeaker. These pins can be connected directly to a ≥ 8-Ω speaker or a speaker amplifier.
MIC+	9	I	**MICROPHONE + INPUT**: This input pin is a single-ended amplifier input for a microphone. It requires a 10-kΩ pull-up resistor to the SAFE VCM pin. If the microphone function is not used, then connect this pin to analog ground.
MIC–	10	I	**MICROPHONE – INPUT**: This pin provides a switched ground connection that interrupts the microphone bias current during power down. If the microphone function is not used or if disabling the microphone bias current during power down is not desirable, then connect this pin to analog ground.
N/C	32	–	**NO CONNECT**: This pin should be left floating.
RESET	14	I	**SAFE RESET**: This pin is used to generate a SAFE reset. A reset is accomplished by pulsing the signal at the RESET pin from a low to high to low. The RESET input pin must be high for at least 10 µs. The SAFE requires 200 ms, after the high-to-low transition, before communicating with the DSP.

7.3.2 SAFE Power Supply Pin Descriptions (CL-MD1724 or CL-MD1724T)

Symbol	VQFP	Type	Description
DGND	23 28–30, 33	GND	**DIGITAL GROUND REFERENCE.**
DV+	27	PWR	**DIGITAL SUPPLY** (5 V ±5%).
LSGND	15,18 19, 21 22	AGND	**LOUDSPEAKER ANALOG GROUND REFERENCE.**
LSV+	16	PWR	**LOUDSPEAKER SUPPLY VOLTAGE** (5 V ±5%).
RXGND	4, 6, 11,12	AGND	**RECEIVER ANALOG GROUND REFERENCE.**
RXV+	13	PWR	**RECEIVER ANALOG SUPPLY VOLTAGE** (5 V ±5%).

7.3.2 SAFE Power Supply Pin Descriptions (CL-MD1724 or CL-MD1724T) (cont.)

Symbol	VQFP	Type	Description
TXGND	1, 38, 39, 41, 43, 44	AGND	**TRANSMITTER ANALOG GROUND REFERENCE.**
TXV+	37	PWR	**TRANSMITTER ANALOG SUPPLY VOLTAGE** (5 V ±5%).
VCM	3	I	**VOLTAGE COMMON MODE**: The SAFE provides an internal 2.5-V reference for the differential analog circuitry. This pin allows the reference to be bypassed using an external 1.0-µF capacitor.
VREF+ VREF-	2 5	I I	**VOLTAGE REFERENCE BUFFER**: The SAFE incorporates an internal differential voltage reference. These pins allow the internal differential reference to be bypassed using an external 1.0-µF capacitors.

7.3.3 SAFE–DAA Interface Pin Descriptions (CL-MD1724 or CL-MD1724T)

Symbol	VQFP	Type	Description
RX+ RX-	7 8	I I	**RECEIVE ANALOG DATA**: These input pins receive the analog differential signals from the DAA.
TX+ TX-	40 42	O O	**TRANSMIT ANALOG DATA**: These pins provide the analog transmitter differential output signals to the DAA.

7.3.4 SAFE–DSP Interface Pin Descriptions (CL-MD1724 or CL-MD1724T)

CAUTION: These pins provide the control/data/clock signals between the SAFE and the DSP. No external components should be connected to these pins.

Symbol	VQFP	Type	Description
AFECLK	31	I	**SAFE CLOCK**: This pin provides the clock source for the SAFE device.
TXSTR*	36	I	**TRANSMIT STROBE**: This pin provides the clock signal required for the SAFE device to receive the serial transmit data from the DSP.
TXDATA	35	I	**TX DATA**: Through this pin the SAFE device receives serial data transmitted from the DSP.
TXENA	34	I	**TX ENABLE**: This pin enables the transmittal of data from the DSP to the SAFE device.
RXSTR*	24	I	**RECEIVE STROBE**: This pin provides the clock signal required for the DSP to receive the serial receive data from the SAFE device.
RXDATA	25	O	**RX DATA**: This pin transmits the receive serial data from the SAFE device to the DSP.
RXENA	26	O	**RX ENABLE:** This pin should be left unconnected.

8. ELECTRICAL SPECIFICATIONS

Table 8-1. Absolute Maximum Ratings

Parameter	5 V	3.3 V
Supply voltage (V_{CC})	+6.0 V	+3.6 V
Input voltages, with respect to ground	−0.3 V to V_{CC} +0.5 V	−0.3 V to +6.0 V
Operating temperature (T_A)	0°C to 70°C	0°C to 70°C
Storage temperature	−65°C to 150°C	−65°C to 150°C

NOTE: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8-2. Recommended Operating Conditions

Parameter	5 V	3.3 V
Supply voltage (V_{CC})	5 V ± 5%	3.3 V ± 10%
Operating free air ambient temperature	0°C < T_A < 70°C	0°C < T_A < 70°C
Crystal frequencies	23.04 MHz	23.04 MHz

8.1 DSP 5-V DC Electrical Characteristics

(@ V_{CC} = 5 V ± 5%; T_A = 0°C to 70°C; V_{OL} for open-drain signals is 0.4 V @ 16 mA sinking; V_{IH} is 2.7 V minimum on RESET.)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
V_{IL}	Input low voltage	−0.5	–	0.8	V	
V_{IH}	Input high voltage	2.0	–	V_{CC}	V	
V_{OL}	Output low voltage		–	0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output high voltage	2.4	–		V	I_{OH} = −400 µA
I_{IL}	Input leakage current	−10	–	10	µA	0 < V_{IN} < V_{CC}
I_{LL}	Data bus tristate leakage current	−10	–	10	µA	0 < V_{OUT} < V_{CC}
I_{OC}	Open-drain output leakage current	−10	–	10	µA	0 < V_{OUT} < V_{CC}

8.1 DSP 5-V DC Electrical Characteristics (cont.)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
I_{CC}	Power supply current	–	160	240	mA	Operational mode CLK = 23.04 MHz
I_{CC-PD}	Power supply current (Power-down mode)	–	–	5	mA	
C_{IN}	Input capacitance	–	–	10	pF	
C_{OUT}	Output capacitance	–	–	10	pF	

8.2 DSP 3.3-V DC Electrical Characteristics

(@ V_{CC} = 3.3 V ± 10%; T_A = 0°C to 70°C; V_{OL} for open-drain signals is 0.4 V @ 16 mA sinking; V_{IH} is 2.7 V minimum on RESET.)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
V_{IL}	Input low voltage	-0.5	–	0.8	V	
V_{IH}	Input high voltage	2.0	–	5	V	
V_{OL}	Output low voltage		–	0.6	V	I_{OL} = 2.4 mA
V_{OH}	Output high voltage	2.4	–		V	I_{OH} = –400 µA
I_{IL}	Input leakage current	–10	–	10	µA	$0 < V_{IN} < V_{CC}$
I_{LL}	Data bus tristate leakage current	–10	–	10	µA	$0 < V_{OUT} < V_{CC}$
I_{OC}	Open-drain output leakage current	–10	–	10	µA	$0 < V_{OUT} < V_{CC}$
I_{CC}	Power supply current	–	110	165	mA	Operational mode CLK = 23.04 MHz
I_{CC-PD}	Power supply current (Power-down mode)	–	–	2	mA	
C_{IN}	Input capacitance	–	–	10	pF	
C_{OUT}	Output capacitance	–	–	10	pF	

8.3 µP 5-V DC Electrical Characteristics

(@ V_{CC} = 5 V ± 5%; T_A = 0°C to 70°C; V_{OL} for open-drain signals is 0.4 V @ 16 mA sinking; V_{IH} is 2.7 V minimum on RESET.)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
V_{IL}	Input low voltage	–0.5	–	0.8	V	
V_{IH}	Input high voltage	2.0	–	V_{CC}	V	
V_{OL}	Output low voltage		–	0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output high voltage	2.4	–		V	I_{OH} = –400 µA
I_{IL}	Input leakage current (except GPIO bus)	–10	–	10	µA	$0 < V_{IN} < V_{CC}$
I_{ILG}	Input leakage current for GPIO bus	–60	–	60	µA	$0 < V_{IN} < V_{CC}$
I_{LL}	Data bus tristate leakage current	–10	–	10	µA	$0 < V_{OUT} < V_{CC}$
I_{OC}	Open-drain output leakage current	–100	–	100	µA	$0 < V_{OUT} < V_{CC}$
I_{CC}	Power supply current	–	100	150	mA	Operational mode CLK = 23.04 MHz
I_{CC-PD}	Power supply current (Power-down mode)	–	–	6	mA	
$I_{HD[0-7]}$	Host data bus	–	–	16	mA	$0 < V_{OUT} < V_{CC}$
I_{OD} I_{OT}	IOCHRDY, WAIT* pin HINTA–G, IREQ pins	–	–	20	mA	$0 < V_{OUT} < V_{CC}$
C_{IN}	Input capacitance	–	–	10	pF	
C_{OUT}	Output capacitance	–	–	10	pF	
I_{GPIO}	GPIO	–	–	12	mA	$0 < V_{OUT} < V_{CC}$

8.4 AC/DC Electrical Characteristics — CL-MD1724 or CL-MD1724T (SAFE)

(@ V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
P_D	Power dissipation	–	130	195	mW	Operational mode
P_{D-PD}	Power dissipation (Power-down mode)	–	–	500	µW	Loudspeaker driver off
I_A	Analog current (TV+, RV+)	–	24	–	mA	Loudspeaker driver off
I_D	Digital current (DV+)	–	2	–	mA	
I_{IDS}	Loudspeaker current (LDSPKR+, LDSPKR–)	–	–	125	mA	
R_X	Loudspeaker impedance	8	–	100	Ω	

8.5 Index of Timing Information

Table 8-3. µP Parallel Host Interface-to-UART Timing (External Address Decode) — Write Cycle

Symbol	Parameter	MIN	MAX
t_1	HA[0–2] setup time to HCS* low	0 ns	–
t_2	HCS* low to HWR* low setup time	10 ns	–
t_3	HD[0–7] valid from HWR* low	–	10 ns
t_4	HWR* low to IOCHRDY low	–	30 ns
t_5	HWR* low to IOCHRDY tristate	–	250 ns
t_6	HWR* hold time after IOCHRDY high	0 ns	–
t_7	HD[0–7] hold time after HWR* high	0 ns	–
t_8	HCS* hold time after HWR* high	0 ns	–
t_9	HA[0–2] hold time after HWR* high	0 ns	–

NOTE: HOSTSEL0 = 0 and HOSTSEL1 = 1 for external decode.

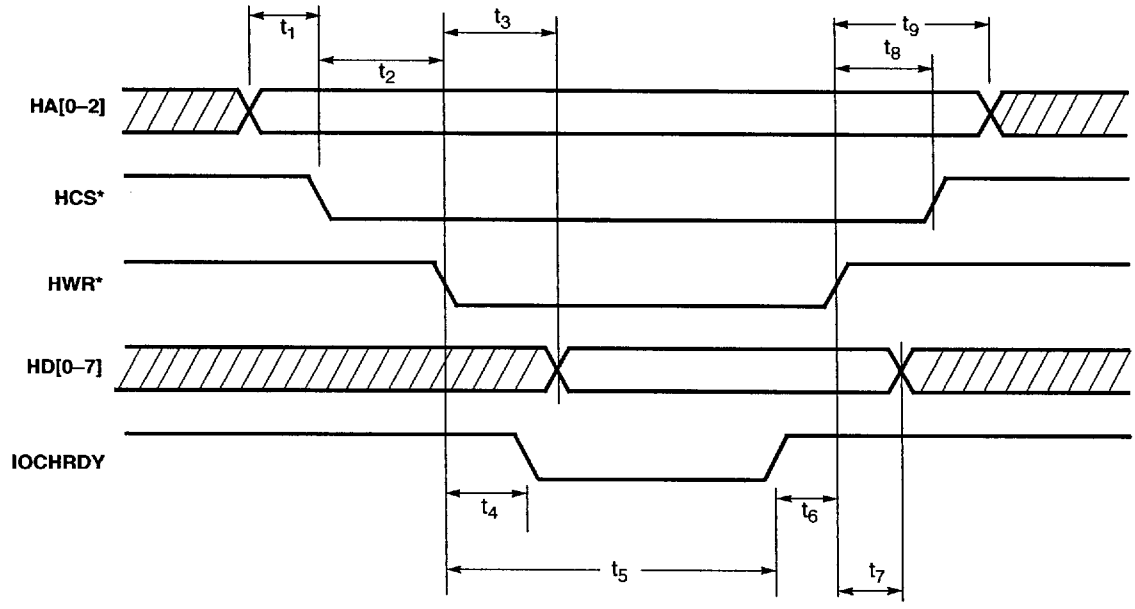


Figure 8-1. µP Parallel Host Interface-to-UART Timing (External Address Decode) — Write Cycle

Table 8-4. µP Parallel Host Interface-to-UART Timing (External Address Decode) — Read Cycle

Symbol	Parameter	MIN	MAX
t_1	HA[0–2] setup time to HCS* low	0 ns	–
t_2	HCS* setup time to HRD* low	10 ns	–
t_3	HD[0–7] valid after HRD* low	–	210 ns
t_4	HRD* low to IOCHRDY low	–	30 ns
t_5	HRD* low to IOCHRDY tristate	–	210 ns
t_6	HRD* hold time after IOCHRDY high	0 ns	–
t_7	HRD* high to HD[0–7] tristate	–	30 ns
t_8	HCS* hold time after HRD* high	0 ns	–
t_9	HA[0–2] hold time after HRD* high	0 ns	–

NOTE: HOSTSEL0 = 0 and HOSTSEL1 = 1 for external decode.

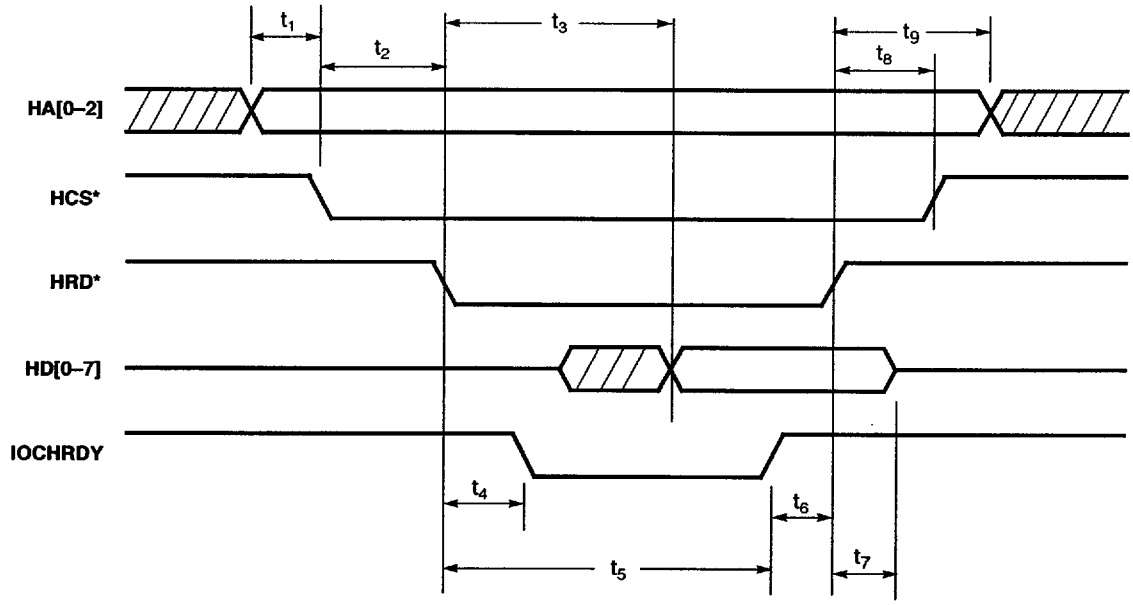


Figure 8-2. µP Parallel Host Interface-to-UART Timing (External Address Decode) — Read Cycle

Table 8-5. µP Parallel Host Interface-to-UART Timing (Internal Address Decode) — Write Cycle

Symbol	Parameter	MIN	MAX
t_1	HD[0–7] valid from HWR* low	–	10 ns
t_2	HWR* low to IOCHRDY low	–	30 ns
t_3	HWR* low to IOCHRDY tristate	–	250 ns
t_4	HWR* hold time after IOCHRDY high	0 ns	–
t_5	HD[0–7] hold time after HWR* high	0 ns	–
t_6	HA[0–9], AEN hold time after HWR* high	0 ns	–

NOTE: HOSTSEL0 = 1 and HOSTSEL1 = 1 for internal decode.

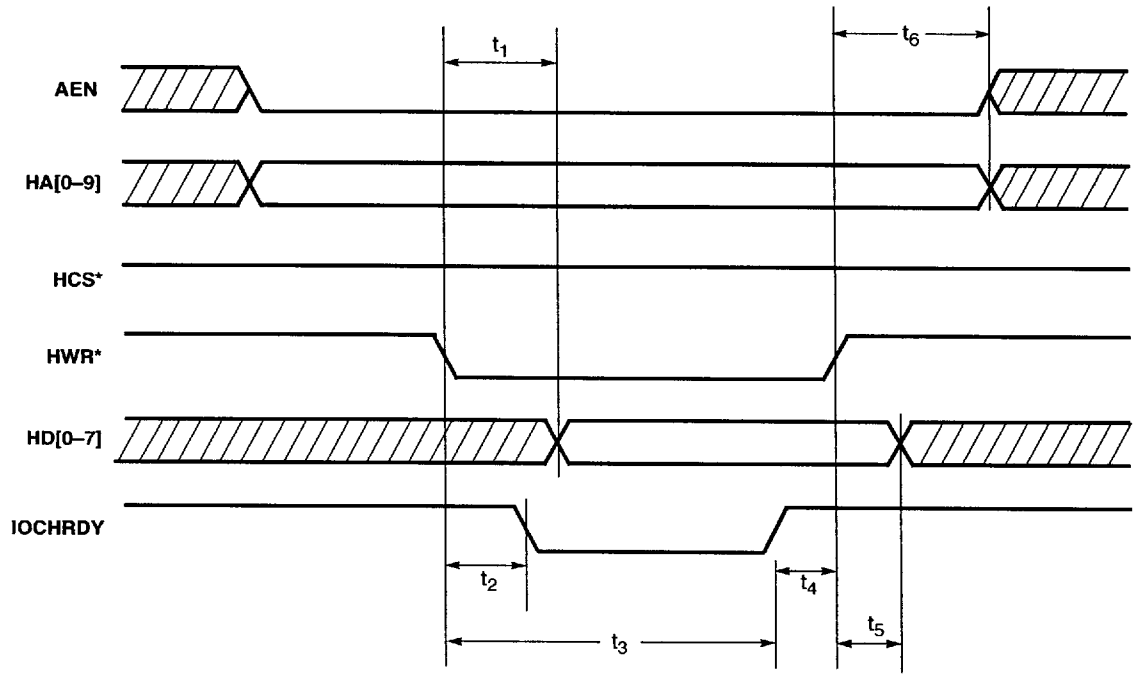


Figure 8-3. µP Parallel Host Interface-to-UART Timing (Internal Address Decode) — Write Cycle

Table 8-6. µP Parallel Host Interface-to-UART Timing (Internal Address Decode) — Read Cycle

Symbol	Parameter	MIN	MAX
t_1	HD[0–7] valid after HRD* low	–	210 ns
t_2	HRD* low to IOCHRDY low	–	30 ns
t_3	HRD* low to IOCHRDY tristate	–	210 ns
t_4	HRD* hold time after IOCHRDY high	0 ns	–
t_5	HRD* high to HD[0–7] tristate	–	30 ns
t_6	HA[0–9], AEN hold time after HRD* high	0 ns	–

NOTE: HOSTSEL0 = 1 and HOSTSEL1 = 1 for internal decode.

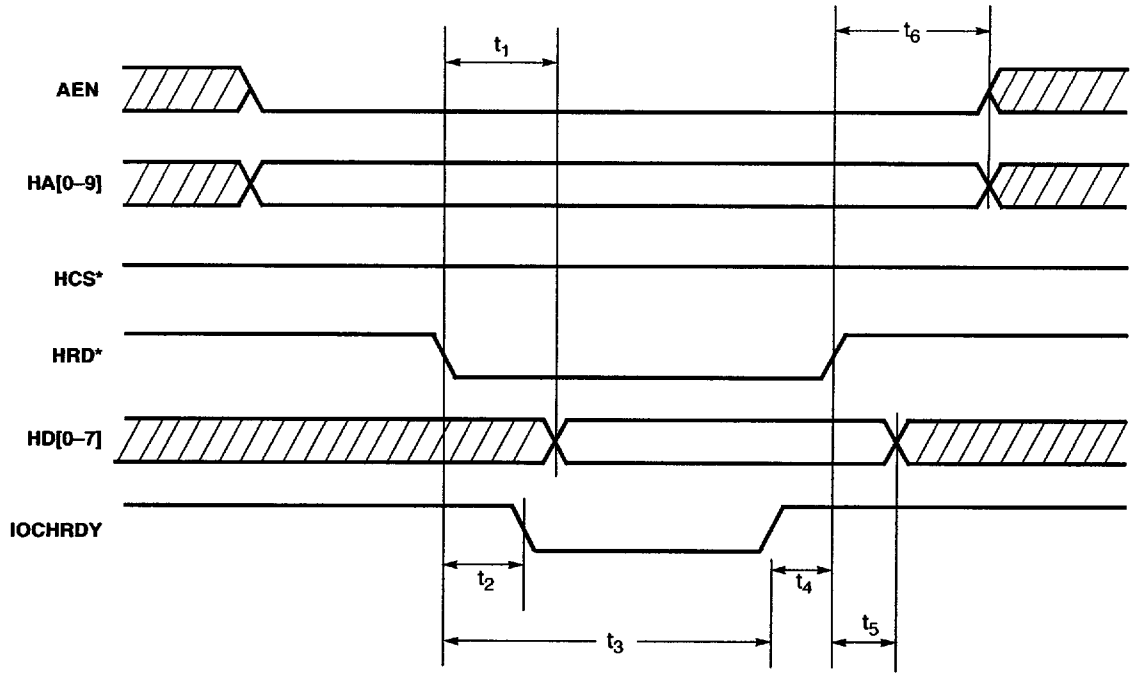


Figure 8-4. µP Parallel Host Interface-to-UART Timing (Internal Address Decode) — Read Cycle

Table 8-7. Plug-and-Play Port Accesses — Write Cycle

Symbol	Parameter	MIN	MAX
t_1	HA[0–15], AEN setup time to HWR* low	10 ns	–
t_2	HD[0–7] valid from HWR* low	–	80 ns
t_3	HD[0–7] hold time after HWR* high	10 ns	–
t_4	HA[0–15], AEN hold time after HWR* high	10 ns	–

NOTES:

1) HOSTSEL0 = 1 and HOSTSEL1 = 0 for Plug-and-Play mode.
2) IOCHRDY is not asserted for plug-and-play port accesses.

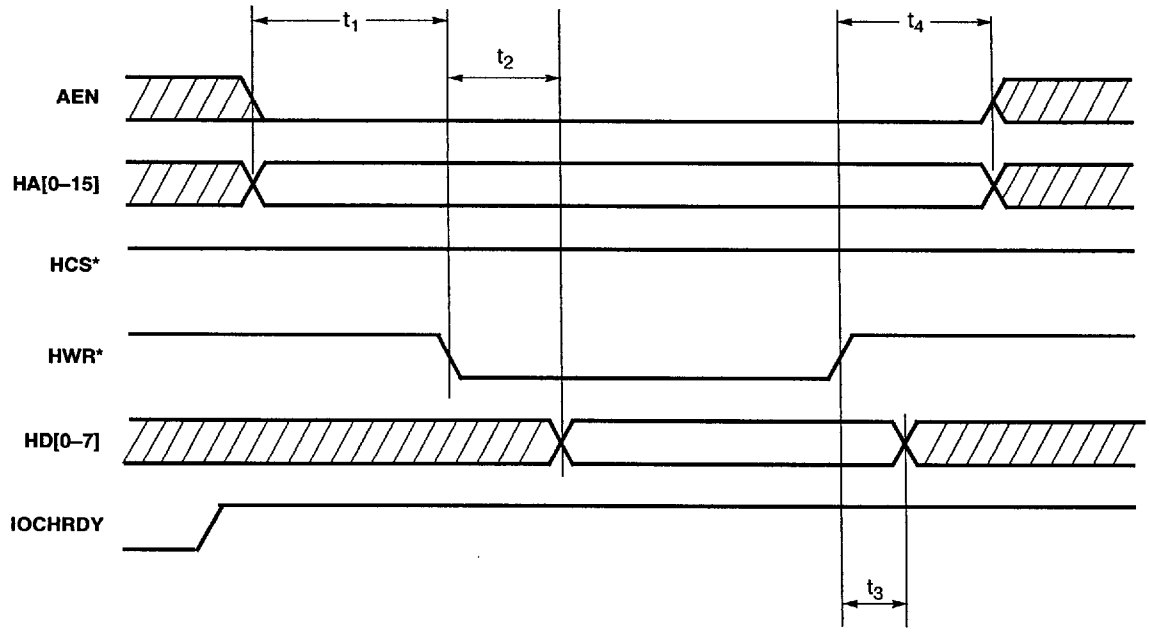


Figure 8-5. Plug and Play Port Accesses — Write Cycle

Table 8-8. Plug-and-Play Port Accesses — Read Cycle

Symbol	Parameter	MIN	MAX
t_1	HA[0–15], AEN setup time to HRD* low	10 ns	–
t_2	HD[0–7] valid after HRD* low	–	50 ns
t_3	HRD* high to HD[0–7] tristate	–	30 ns
t_4	HA[0–15], AEN hold time after HRD* high	0 ns	–

NOTES:

1) HOSTSEL0 = 1 and HOSTSEL1 = 0 for Plug-and-Play mode.
2) IOCHRDY is not asserted low for plug-and-play port accesses.

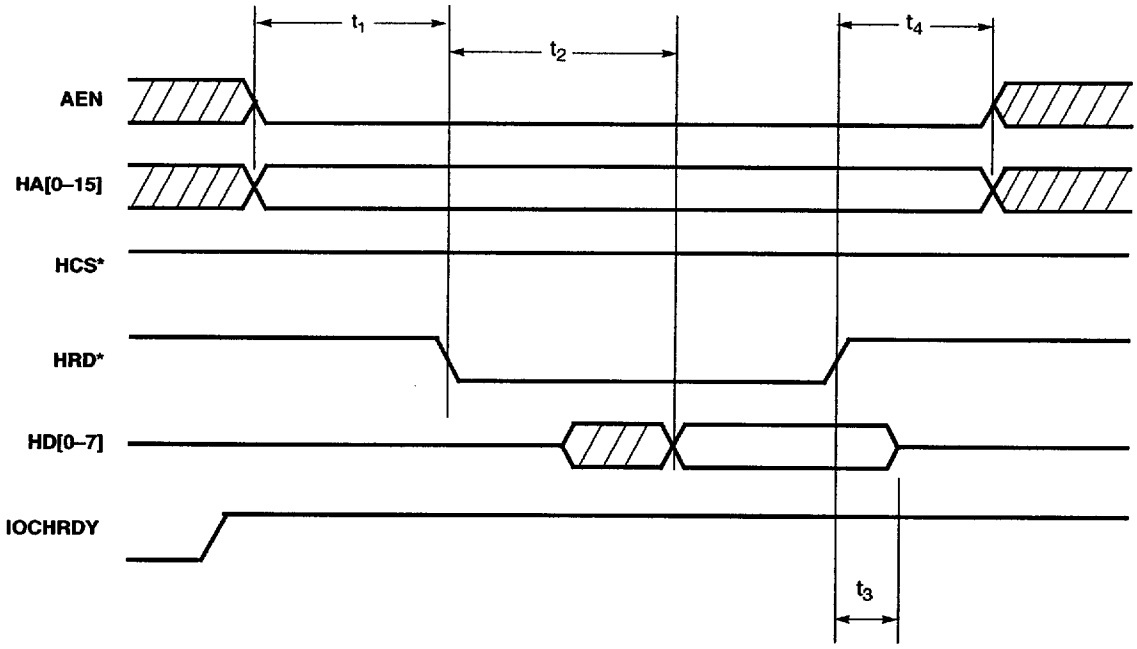


Figure 8-6. Plug and Play Port Accesses — Read Cycle

Table 8-9. µP Expansion Bus Timing Diagram — Write Cycle

Symbol	Parameter	Typical	Minimum
t_1	Setup time for CS* before EBWR* low	1/2 cycle	–
t_2	Hold time for CS* after EBWR* high	1/2 cycle – 5 ns	–
t_3	Setup time for EBADR before EBWR* low	1/2 cycle – 5 ns	–
t_4	Hold time for EBADR after EBWR* high	1 ns	–
t_5	EBDAT valid before EBWR* high	–	Write pulse width – 5 ns
t_6	EBDAT hold time after EBWR* high	–	1/2 cycle – 4 ns
t_7	Width of EBWR* pulse = 1+ the number of wait states		

NOTE: One cycle at 23.04 MHz = 43.40 ns.

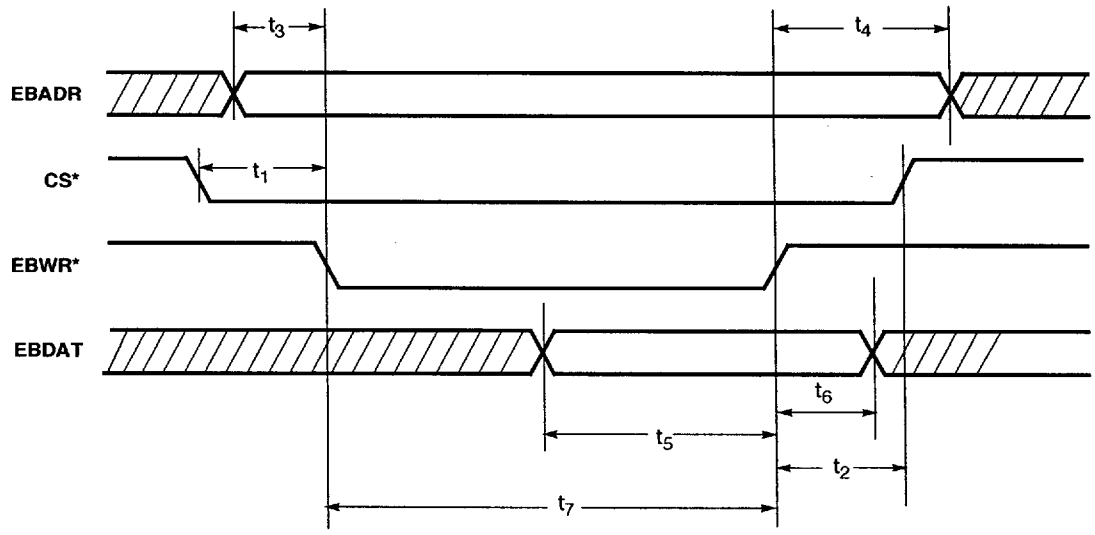


Figure 8-7. µP Expansion Bus Timing Diagram — Write Cycle

Table 8-10. µP Expansion Bus Timing Diagram — Read Cycle

Symbol	Parameter	Typical	Minimum
t_1	Setup time for CS* before EBRD* low	1/2 cycle	–
t_2	Hold time for CS* after EBRD* high	1/2 cycle	–
t_3	Setup time for EBADR before EBRD* low	1/2 cycle – 5 ns	–
t_4	Hold time for EBADR after EBRD* high	1 ns	–
t_5	EBDAT valid before EBRD* high	–	15 ns
t_6	EBDAT hold time after EBRD* high	–	0
t_7	Width of EBRD* pulse = 1/2+ the number of wait states		

NOTE: One cycle at 23.04 MHz = 43.40 ns.

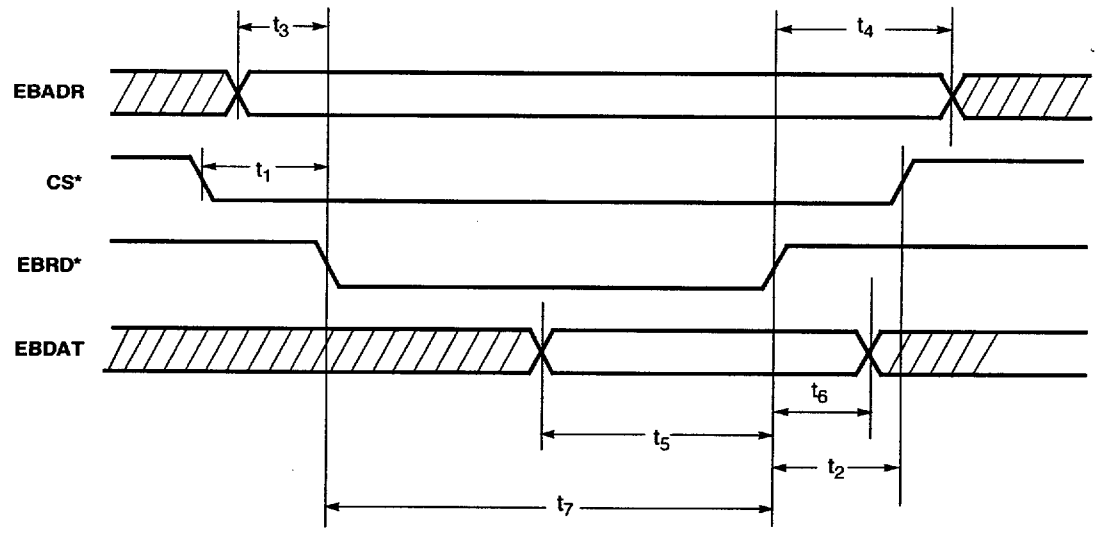


Figure 8-8. µP Expansion Bus Timing Diagram — Read Cycle

Table 8-11. µP PC Card UART Interface Timing Diagram — Write Cycle

Symbol	Parameter	MIN	MAX
t_1	HA[0–9] setup time to IOWR* low	10 ns	–
t_2	REG* and CE1* low to IOWR* low setup time	10 ns	–
t_3	HD[0–7] valid from IOWR* low	–	10 ns
t_4	IOWR* low to WAIT* low	–	30 ns
t_5	IOWR* low to WAIT* high	–	250 ns
t_6	IOWR* hold time after WAIT* high	0 ns	–
t_7	HD[0–7] hold time after IOWR* high	0 ns	–
t_8	REG* and CE1* hold time after IOWR* high	0 ns	–
t_9	HA[0–9] hold time after IOWR* high	0 ns	–
t_{10}	IOWR* low to INPACK* low	–	20 ns
t_{11}	INPACK* hold time after IOWR* high	–	5 ns

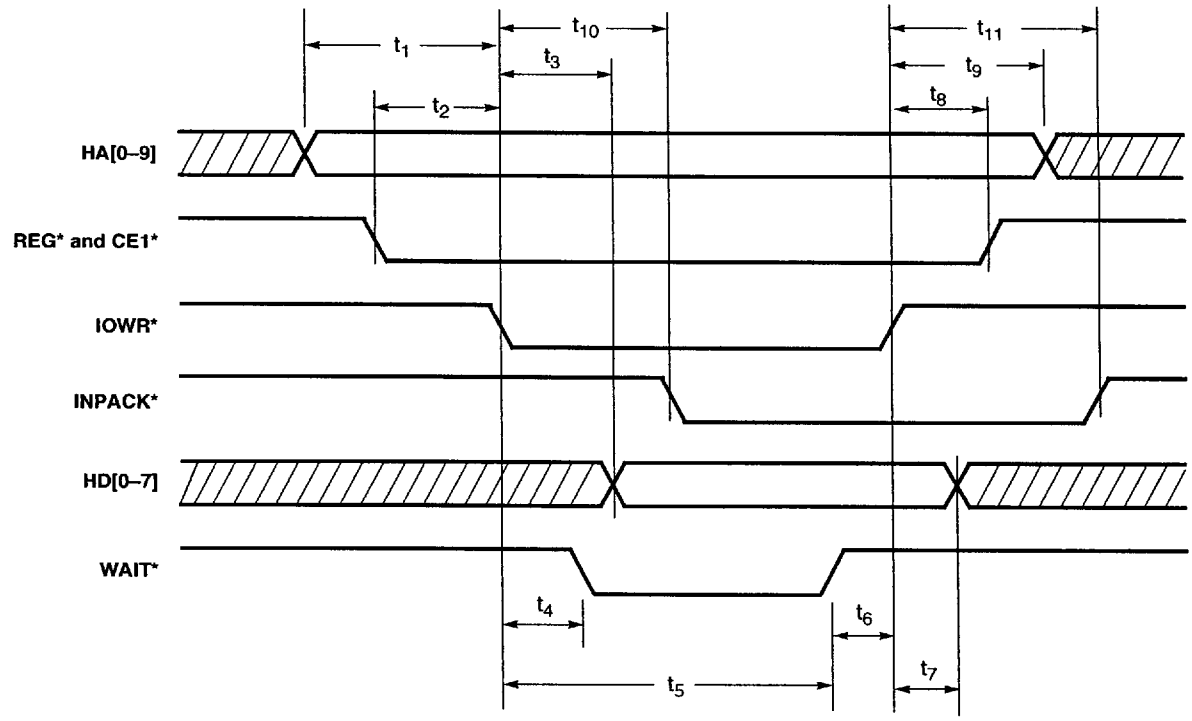


Figure 8-9. µP PC Card UART Interface Timing Diagram — Write Cycle

Table 8-12. µP PC Card UART Interface Timing Diagram — Read Cycle

Symbol	Parameter	MIN	MAX	
t_1	HA[0–9] setup time to IORD* low	10 ns	–	ns
t_2	REG* and CE1* setup time to IORD* low	10 ns	–	ns
t_3	HD[0–7] valid after IORD* low	–	210 ns	
t_4	IORD* low to WAIT* low	–	35 ns	
t_5	IORD* low to WAIT* high	–	210 ns	
t_6	IORD* hold time after WAIT* high	0 ns	–	
t_7	IORD* high to HD[0–7] tristate	–	30 ns	
t_8	REG* and CE1* hold time after IORD* high	0 ns	–	
t_9	HA[0–9] hold time after IORD* high	0 ns	–	
t_{10}	IORD* low to INPACK* low	–	20 ns	
t_{11}	INPACK* hold time after IORD* high	–	5 ns	

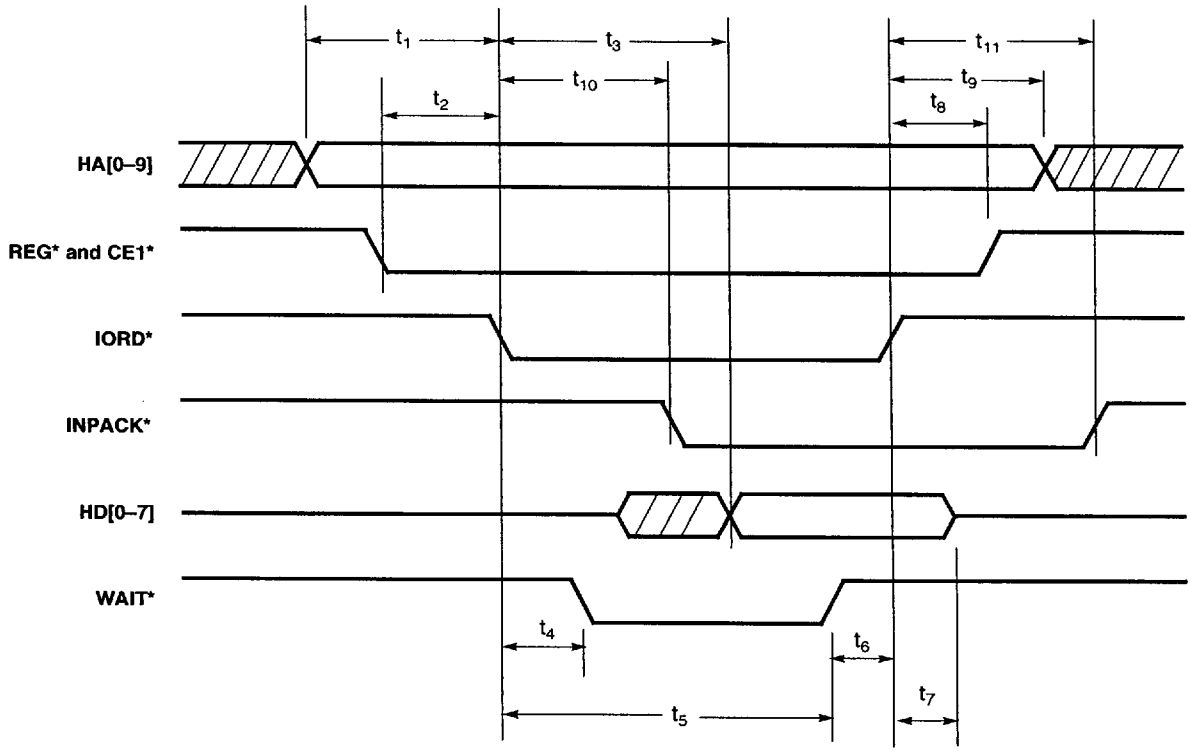


Figure 8-10. µP PC Card UART Interface Timing Diagram — Read Cycle

Table 8-13. µP PC Card Configuration Register Interface Timing — Write Cycle

Symbol	Parameter	MIN	MAX
t_1	HA[0–9] setup time to REG* and CE1* low	0 ns	–
t_2	REG* and CE1* low to WE* low setup time	10 ns	–
t_3	HD[0–7] valid before WE* high	40 ns	–
t_4	WE* active duration	60 ns	–
t_5	HD[0–7] hold time after WE* high	15 ns	–
t_6	REG* and CE1* hold time after WE* high	10 ns	–
t_7	HA[0–9] hold time after WE* high	15 ns	–
t_8	WE* low to INPACK* low	–	20 ns
t_9	INPACK* hold time after WE* high	–	5 ns

NOTE: WAIT* is not asserted for configuration register accesses.

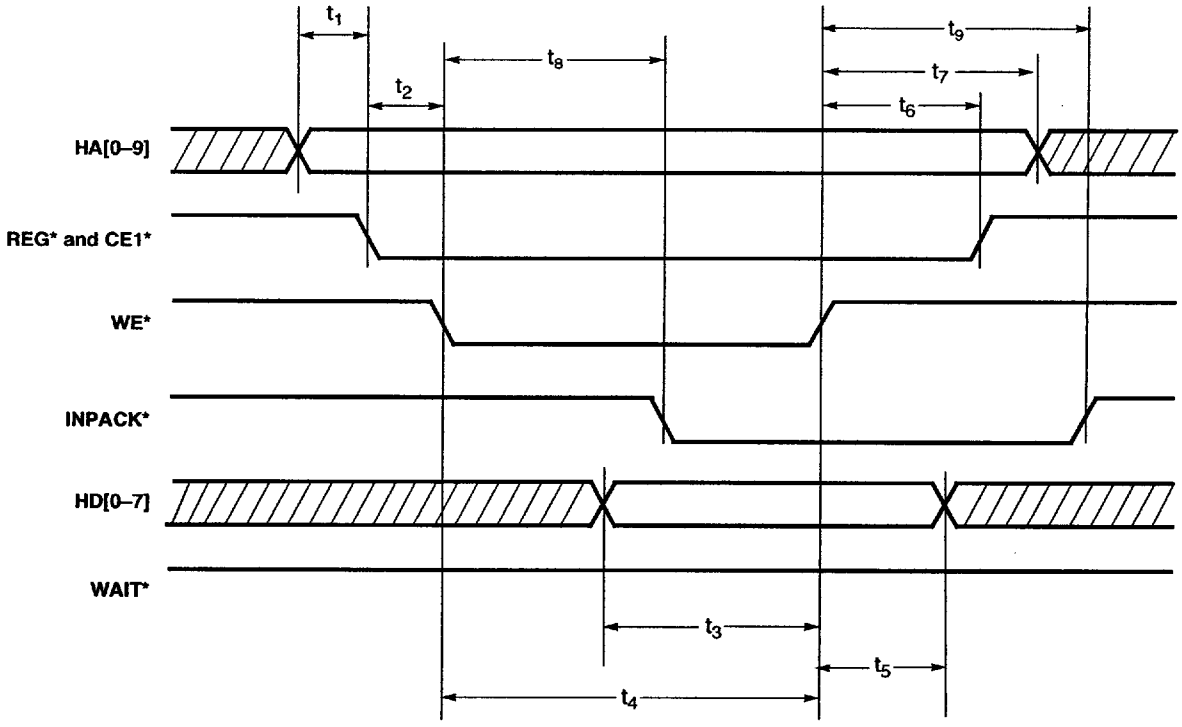


Figure 8-11. µP PC Card Configuration Register Interface Timing Diagram — Write Cycle

Table 8-14. µP PC Card Configuration Register Interface Timing — Read Cycle

Symbol	Parameter	MIN	MAX	
t_1	HA[0–9] setup time to REG* and CE1* low	0 ns	–	ns
t_2	REG* and CE1* low to OE* low setup time	10 ns	–	ns
t_3	HD[0–7] valid after OE* low	–	50 ns	
t_4	OE* active duration	60 ns	–	
t_5	HD[0–7] hold time after OE* high	–	40 ns	
t_6	REG* and CE1* hold time after OE* high	10 ns	–	
t_7	HA[0–9] hold time after OE* high	15 ns	–	
t_8	OE* low to INPACK* low	–	20 ns	
t_9	INPACK* hold time after OE* high	–	5 ns	

NOTE: WAIT* is not asserted for configuration register accesses.

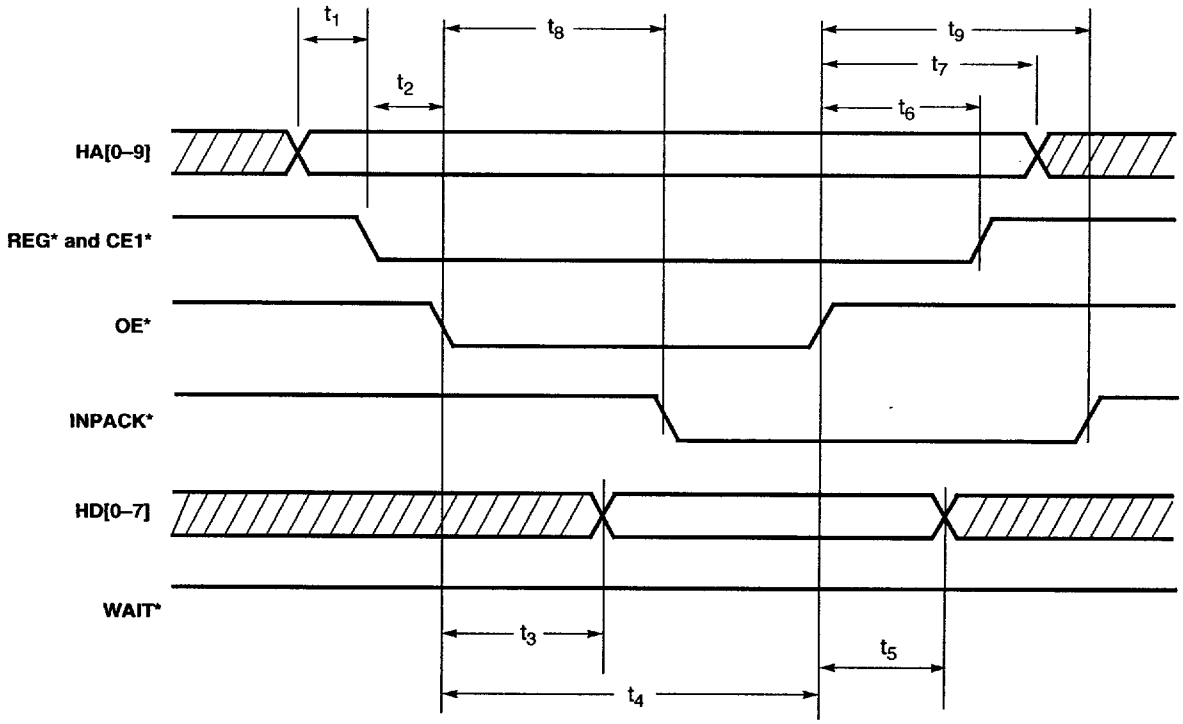


Figure 8-12. µP PC Card Configuration Register Interface Timing Diagram — Read Cycle

Table 8-15. µP PC Card CIS Access Timing Diagram — Read Cycle

Symbol	Parameter	MIN	MAX
t_1	HA[0–9] setup time to REG* and CE1* low	0 ns	–
t_2	REG* and CE1* setup time to OE* low	10 ns	–
t_3	HD[0–7] valid after OE* low	–	$\left(\left\{1+\left[\frac{32}{\text{Bus width}}\cdot n_w\right]\right\}\cdot 43.40\text{ ns}\right)+140\text{ ns}$
t_4	OE* low to WAIT* low	–	35 ns
t_5	OE* low to WAIT* high	–	$\left(\left\{1+\left[\frac{32}{\text{Bus width}}\cdot n_w\right]\right\}\cdot 43.40\text{ ns}\right)+150\text{ ns}$
t_6	OE* hold time after WAIT* high	0 ns	–
t_7	OE* high to HD[0–7] tristate	–	30 ns
t_8	REG* and CE1* hold time after OE* high	0 ns	–
t_9	HA[0–9] hold time after OE* high	0 ns	–
t_{10}	OE* low to INPACK* low	–	45 ns
t_{11}	INPACK* hold time after OE* high	–	45 ns

NOTES:

1) n_w = max [(w_s + 1), (external wait + 3)].
2) w_s = number of wait states.
3) Bus width = 8 or 16 bits.

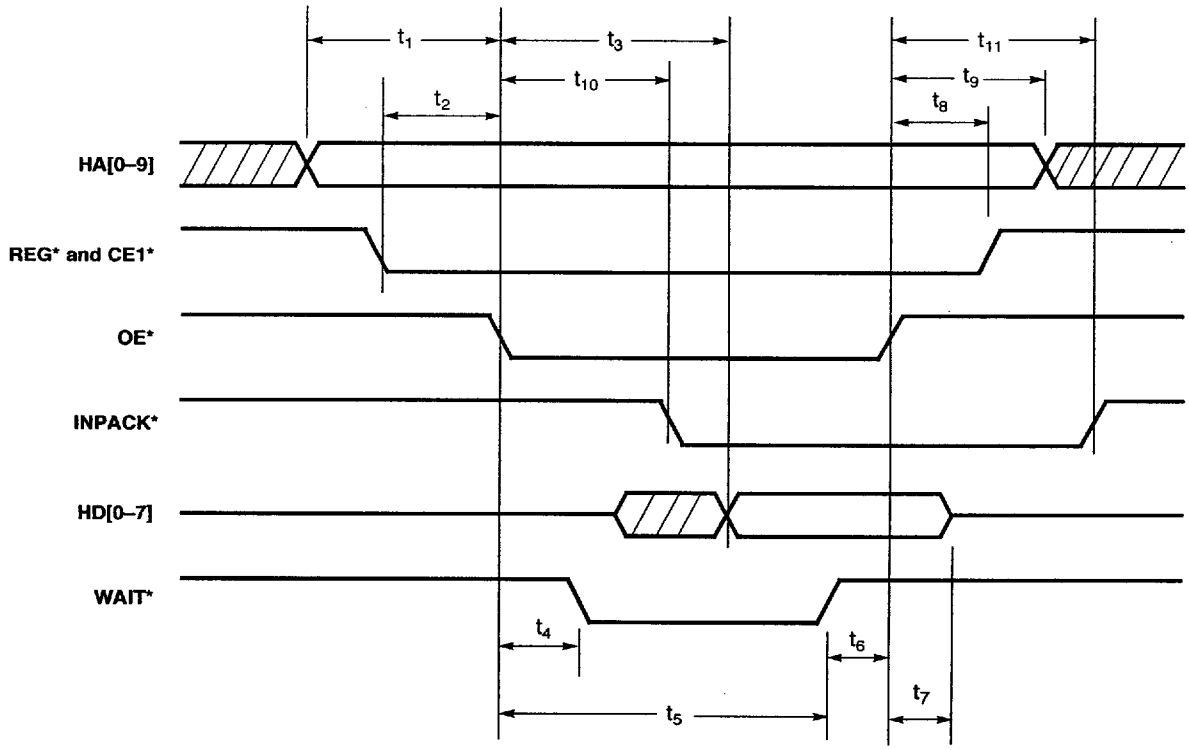


Figure 8-13. µP PC Card CIS Access Timing Diagram — Read Cycle

Table 8-16. µP External Memory Access Through Test Register — Write Cycle

Symbol	Parameter	MIN	MAX
t_1	HA[0–9], AEN setup time to HWR* low	10 ns	–
t_2	HD[0–7] valid from HWR* low	–	10 ns
t_3	HWR* low to IOCHRDY low	–	30 ns
t_4	HWR* low to IOCHRDY tristate	–	$\left(\left\{1+\left[\frac{32}{\text{Bus width}}\cdot n_w\right]\right\}\cdot 43.40\text{ ns}\right)+180\text{ ns}$
t_5	HWR* hold time after IOCHRDY high	0 ns	–
t_6	HD[0–7] hold time after HWR* high	0 ns	–
t_7	HA[0–9], AEN hold time after HWR* high	0 ns	–

NOTES:

1) n_w = max [(w_s + 1), (external wait + 3)].
2) w_s = number of wait states.
3) Bus width = 8 or 16 bits.

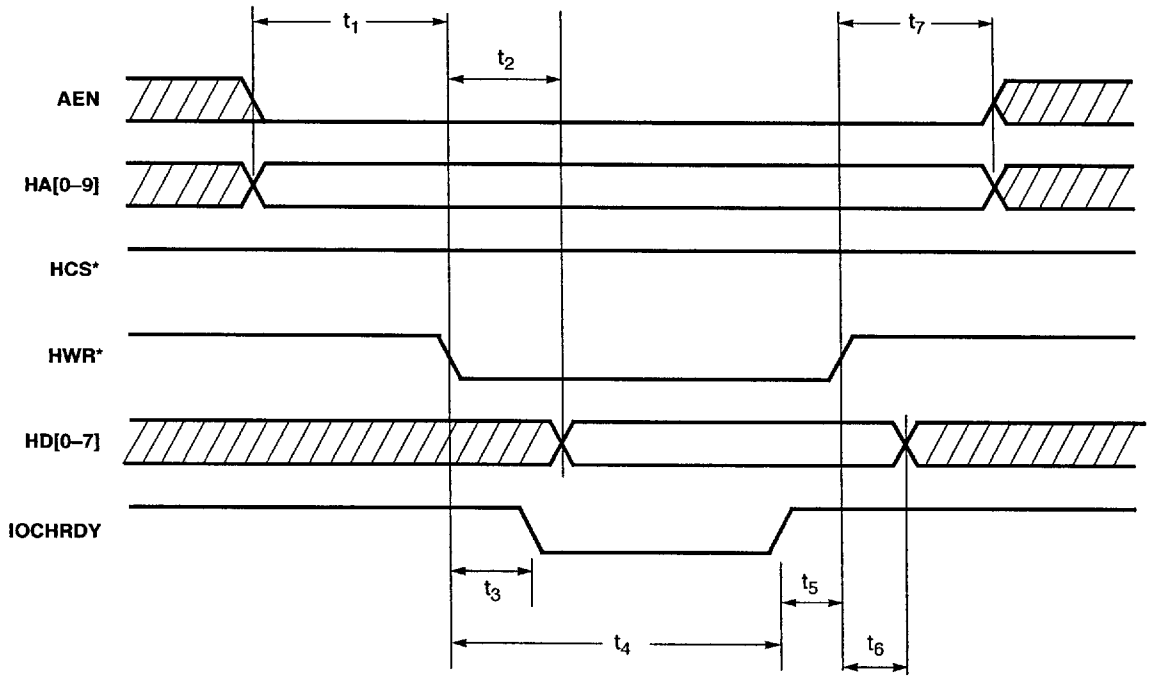


Figure 8-14. µP External Memory Access Through Test Register — Write Cycle

Table 8-17. µP External Memory Access Through Test Register — Read Cycle

Symbol	Parameter	MIN	MAX
t_1	HA[0–9], AEN setup time to HRD* low	10 ns	–
t_2	HD[0–7] valid after HRD* low	–	$\left(\left\{1+\left[\frac{32}{\text{Bus width}}\cdot n_w\right]\right\}\cdot 43.40\text{ ns}\right)+140\text{ ns}$
t_3	HRD* low to IOCHRDY low	–	30 ns
t_4	HRD* low to IOCHRDY tristate	–	$\left(\left\{1+\left[\frac{32}{\text{Bus width}}\cdot n_w\right]\right\}\cdot 43.40\text{ ns}\right)+150\text{ ns}$
t_5	HRD* hold time after IOCHRDY high	0 ns	–
t_6	HRD* high to HD[0–7] tristate	–	30 ns
t_7	HA[0–9], AEN hold time after HRD* high	0 ns	–

NOTES:

1) n_W = max [(w_s + 1), (external wait + 3)].
2) w_s = number of wait states.
3) Bus width = 8 or 16 bits.

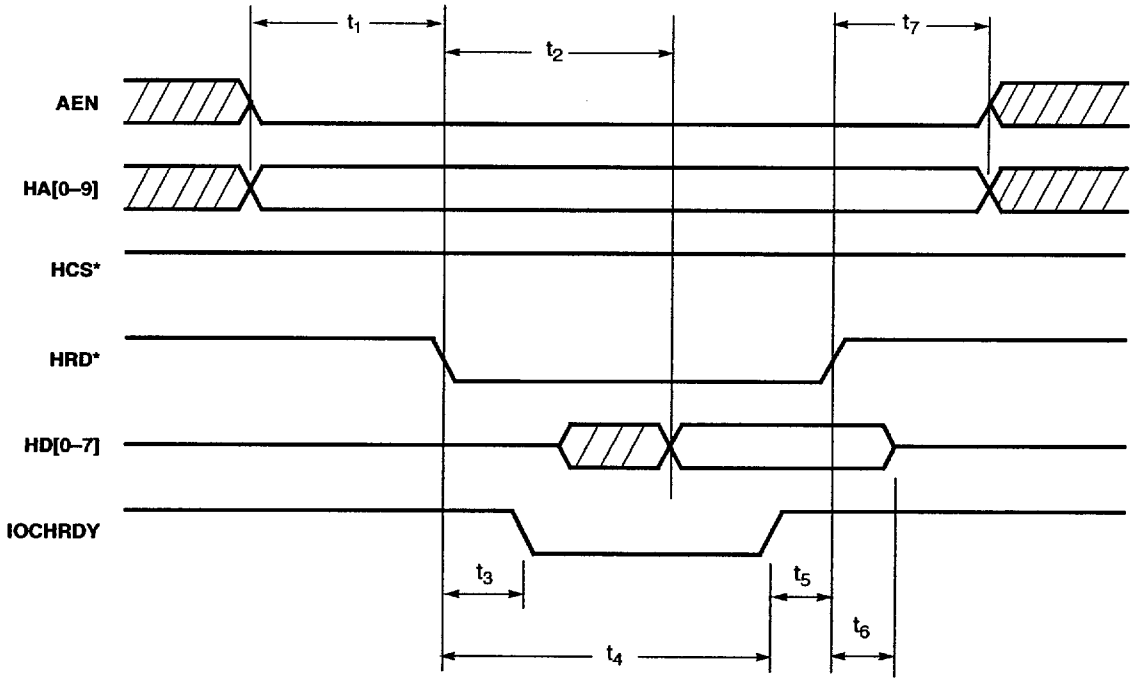


Figure 8-15. µP External Memory Access Through Test Register — Read Cycle

Table 8-18. DSP Control Processor Timings — Write Cycle

Symbol	Parameter	MIN	MAX
t_1	CPCS* low to CPWR* low setup time	0 ns	–
t_2	valid CPCS* low to CPADR[0–7]	–	20 ns
t_3	CPWR* low width	200 ns	–
t_4	CPDAT[0–7] valid from CPWR* low	–	20 ns
t_5	CPWR* low to CPWAIT low	–	25 ns
t_6	CPWAIT* low width	–	180 ns
t_7	CPADR[0–7] hold time after CPWR* high	0 ns	–
t_8	CPCS* hold time after CPWR* high	0 ns	–
t_9	CPDAT[0–7] hold time after CPWR* high	0 ns	–
t_{10}	CPWR* high width	50 ns	–

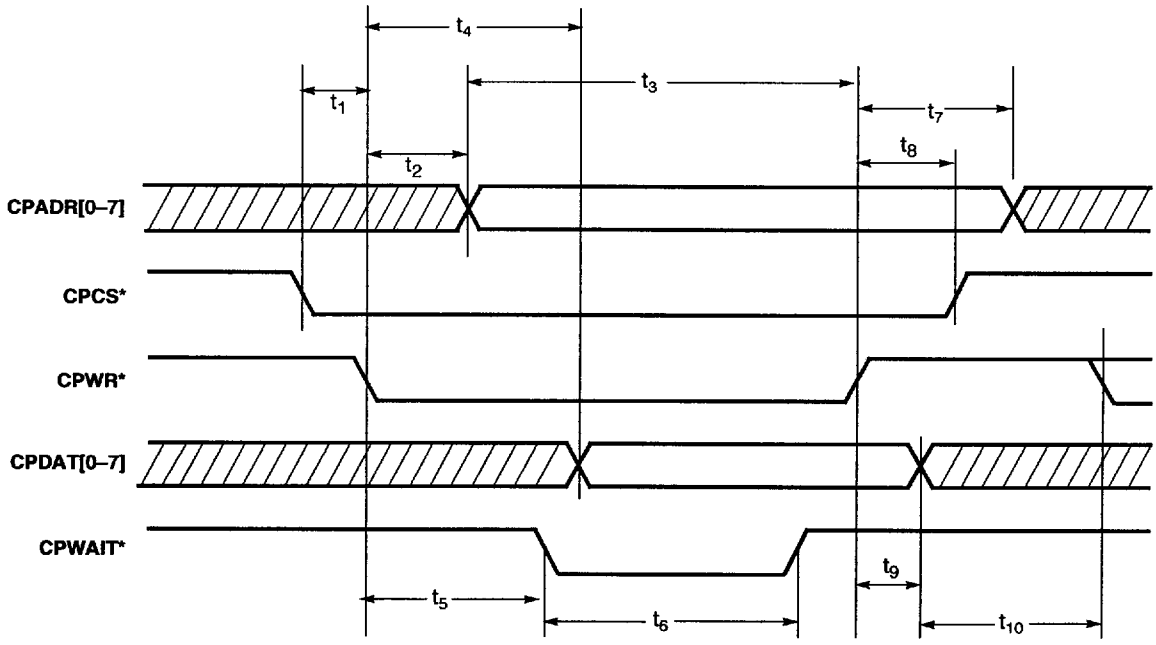


Figure 8-16. DSP Control Processor Timings — Write Cycle

Table 8-19. DSP Control Processor Timings — Read Cycle

Symbol	Parameter	MIN	MAX
t_1	CPCS* setup time to CPWR* low	0 ns	–
t_2	CPADR[0–7] valid after CPRD* low	–	20 ns
t_3	CPRD* low width	200 ns	–
t_4	CPDAT[0–7] valid after CPRD* low	–	180 ns
t_5	CPRD* low to CPWAIT* low	–	25 ns
t_6	CPWAIT* low width	–	180 ns
t_7	CPWAIT* high after valid CPDAT[0–7]	5 ns	–
t_8	CPCS* hold time after CPRD* high	0 ns	–
t_9	CPADR[0–7] hold time after HRD* high	0 ns	–
t_{10}	CPRD* high to HD[0–7] tristate	0 ns	–
t_{11}	CPRD* high width	40 ns	–

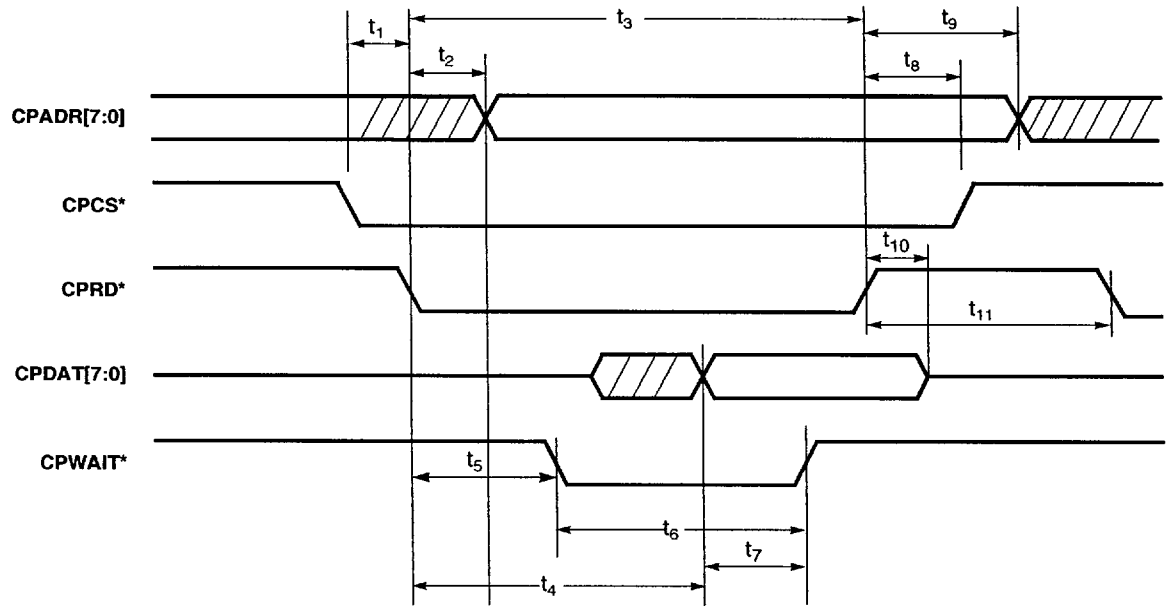


Figure 8-17. DSP Control Processor Timings — Read Cycle

Table 8-20. DSP Expansion Bus Timing Diagram — Write Cycle

Symbol	Parameter	MIN	MAX
t_1	PA[17:0] address setup time to EPGMWR* low	4 ns	–
t_2	EPGMCS* low to EPGMWR* low setup time	4 ns	–
t_3	PA[17:0] address hold time after EPGMWR* high	5 ns	–
t_4	EPGMWR* high pulse	7 ns	–
t_5	EPGMWR* high to PD[15:0] tristate	half-cycle, write high to tristate, or 4 ns	–
t_6	EPGMWR* low pulse	n + 1 cycles (n = 0–7), or 20 ns	–
t_7	PD[15:0] valid to EPGMWR* high	10 ns	–

NOTE: Expansion bus timing is based on a 40-MHz clock speed.

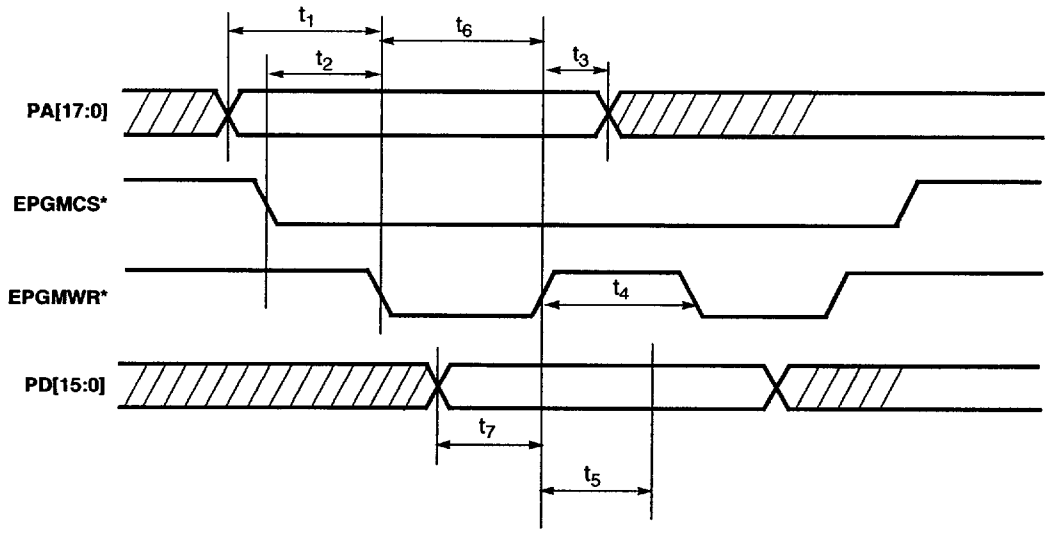


Figure 8-18. DSP Expansion Bus Timing Diagram — Write Cycle

Table 8-21. DSP Expansion Bus Timing Diagram — Read Cycle

Symbol	Parameter	MIN	MAX
t_1	PA[17:0] setup time before EPGRD* low	4 ns	–
t_2	EPGMCS* low to EPGMRD* low setup time	5 ns	–
t_3	PD[15:0] stable after EPGMRD* low	–	5 ns
t_4	PD[15:0] hold time after EPGRD* high	0 ns	–
t_5	PA[17:0] hold time after EPGRD* high	1 ns	–
t_6	EPGMRD* high to EPGMCS* high	1 ns	–

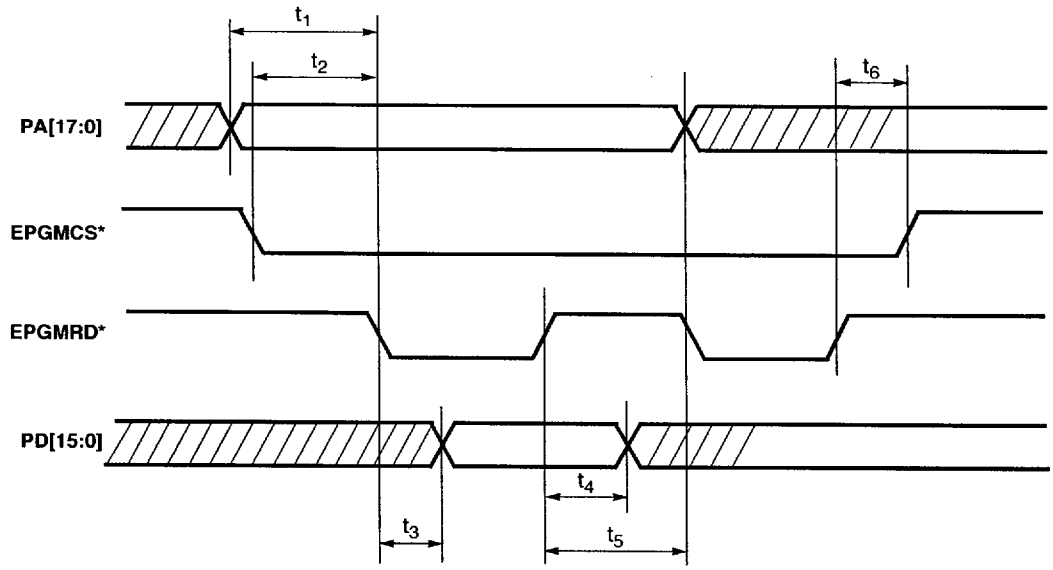


Figure 8-19. DSP Expansion Bus Timing Diagram — Read Cycle

Notes

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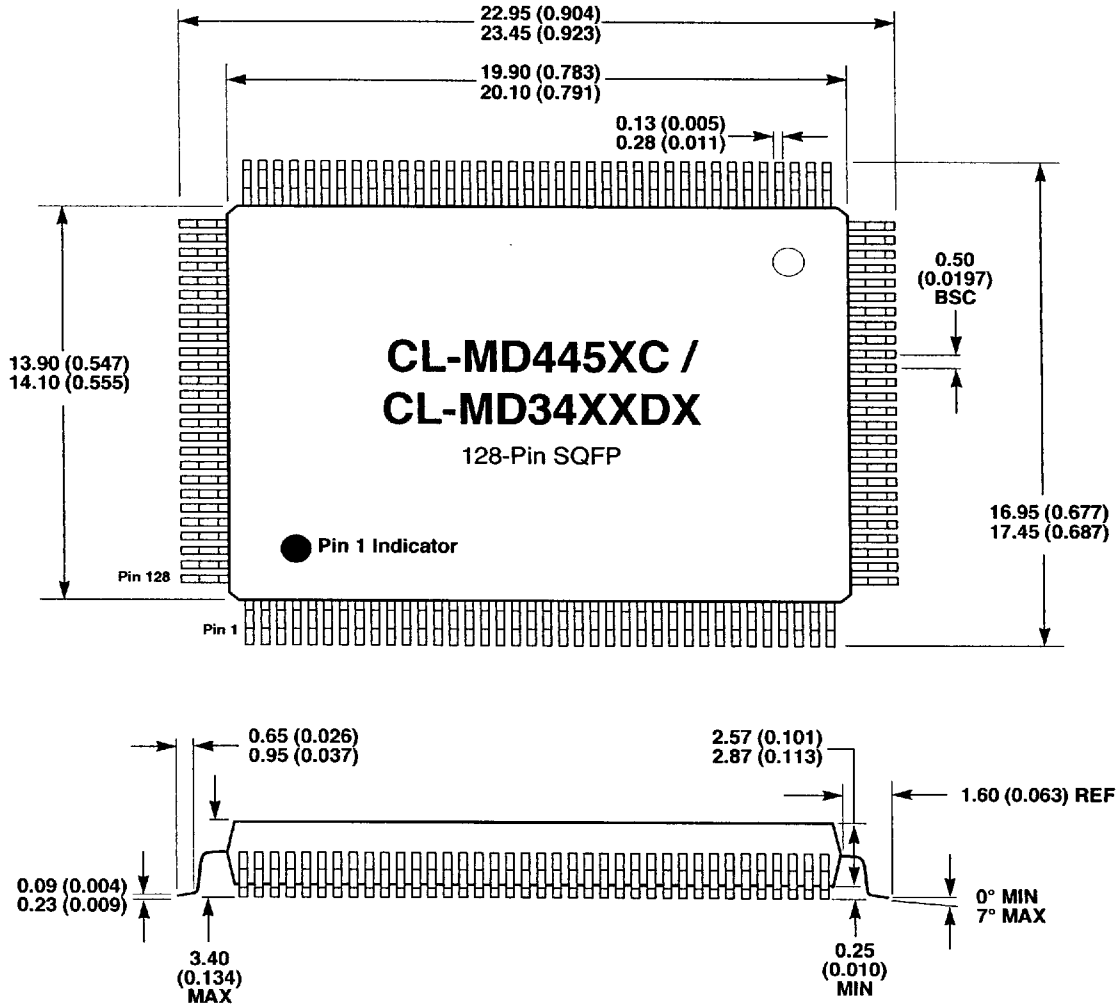
9. SAMPLE PACKAGE INFORMATION

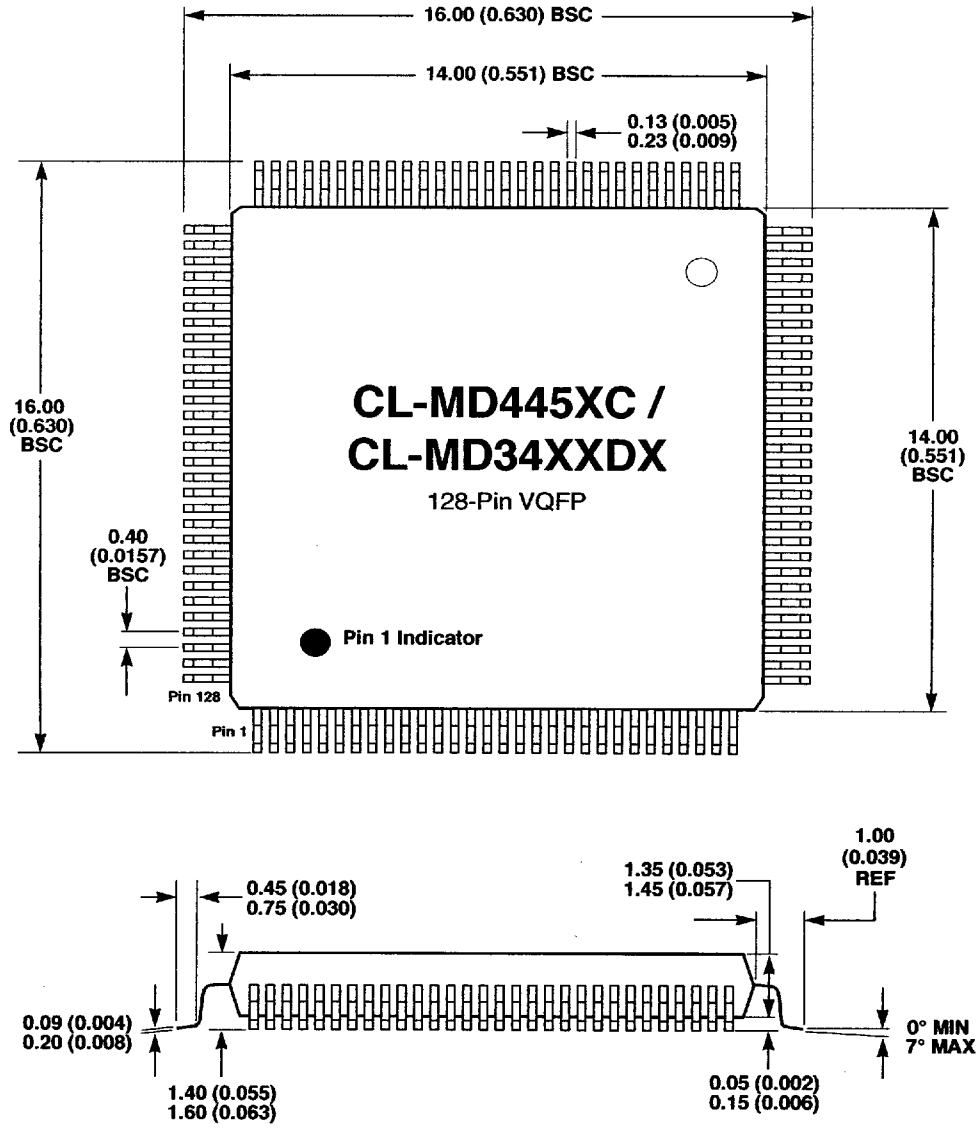
9.1 128-Pin SQFP Package Outline



NOTES:

1) Dimensions are in millimeters (inches); the controlling dimension is in millimeters.
2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

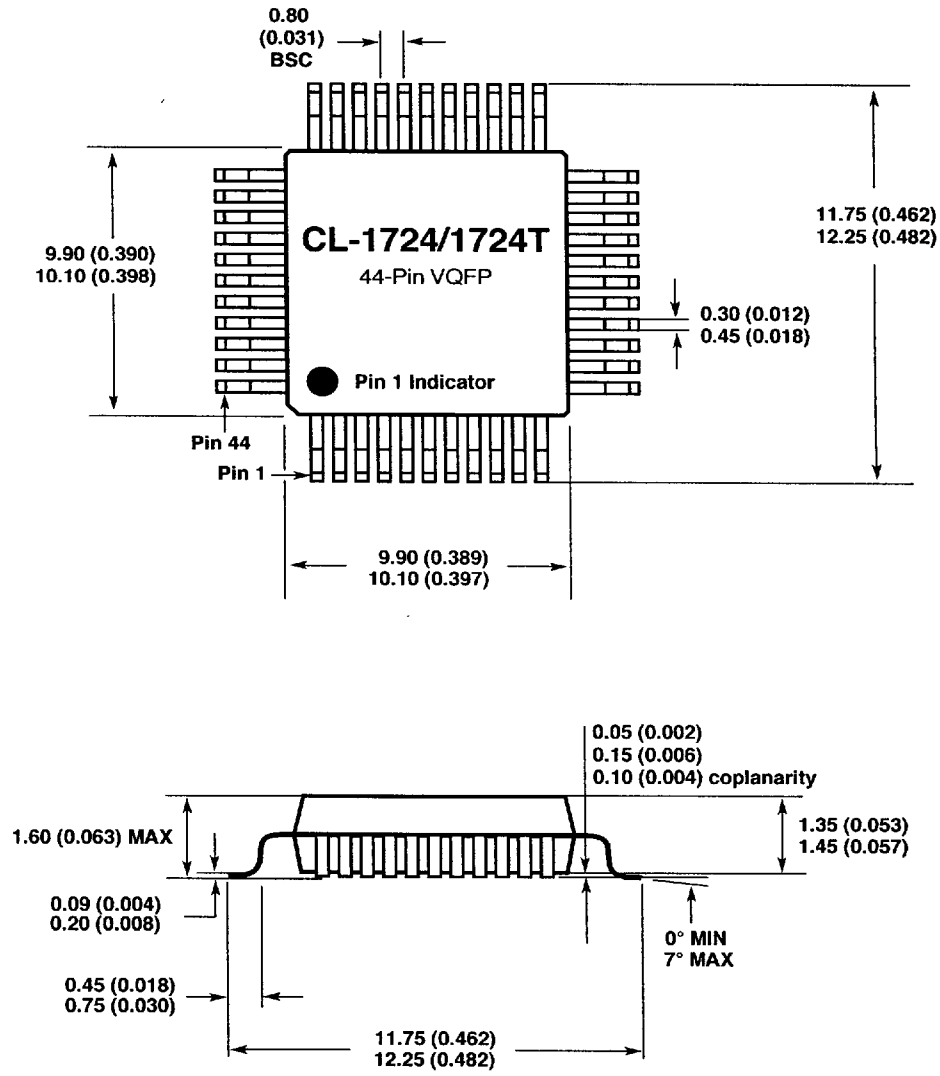
9.2 128-Pin VQFP Package Outline



NOTES:

1) Dimensions are in millimeters (inches); the controlling dimension is in millimeters.
2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

9.3 44-Pin VQFP Package Outline



NOTES:

1) Dimensions are in millimeters (inches); the controlling dimension is in millimeters.
2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

Notes

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10. ORDERING INFORMATION

Chipset Composition

Market	Parallel/Serial Host Interface	PC Card Host Interface
Data/fax voice	**CL-MD3450** µP: CL-MD4450C DSP: CL-MD3450D SAFE: CL-MD1724	**CL-MD3451T** µP: CL-MD4451C DSP: CL-MD3451DT SAFE: CL-MD1724T
Data/fax voice, full-duplex speaker-phone	**CL-MD3452** µP: CL-MD4450C DSP: CL-MD3450D SAFE: CL-MD1724 SAFE: CL-MD1724	**CL-MD3453T** µP: CL-MD4451C DSP: CL-MD3451DT SAFE: CL-MD1724T SAFE: CL-MD1724T
Data/fax voice, full-duplex speaker-phone, DSVD	**CL-MD3462T** µP: CL-MD4450C DSP: CL-MD3460DT SAFE: CL-MD1724T SAFE: CL-MD1724T	**CL-MD3463T** µP: CL-MD4451C DSP: CL-MD3460DT SAFE: CL-MD1724T SAFE: CL-MD1724T

Chipset Information

CL – MDXXXXX – NNN

- CL: Cirrus Logic Inc.
- MD: Modem, Data Communications
- XXXXX: Chipset Part Number:
  - MD3450
  - MD3451T
  - MD3452
  - MD3453T
  - MD3462T
  - MD3463T
- NNN: Chipset Top Assembly Number (contact your local Cirrus Logic sales office for the latest revision)

Device Information

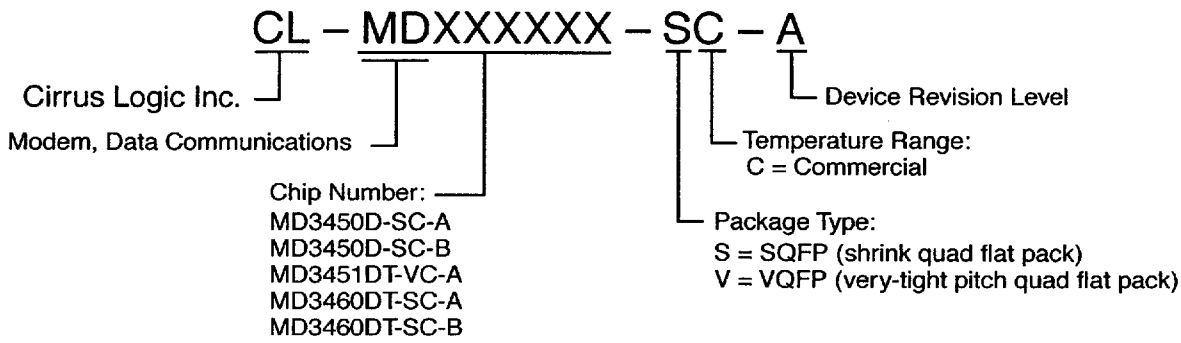

Table 10-1 on page 106 lists the currently available families of Cirrus Logic chipsets. A brief description of each chipset is provided.

Table 10-1. Cirrus Logic V.34+ FastPath™ Modem Products

Number of Devices	Chipset	Features
3	CL-MD3450	High-speed modem that provides 33,600-bps Data mode and 14,400-bps Fax mode. It includes three built-in DTE interfaces — a parallel 16C450A/16C550-compatible ISA bus interface, a Windows® 95-compatible ISA bus plug-and-play interface, and a serial RS-232 interface. Voice features include IS-101 Voice mode and Radish® VoiceView™ upgrade option.
	CL-MD3451T	Same features as the CL-MD3450, except the chipset adds a built-in PC Card interface and uses DSP and SAFE chips that are 3.3 V instead of 5 V. The PC Card interface has 16C450/16C550-compatible registers. This chipset does not support parallel ISA bus and serial RS-232 host interfaces.
4	CL-MD3452	Same features as the CL-MD3450, plus full-duplex Speakerphone mode with internal echo cancellation and an extra SAFE.
	CL-MD3453T	Same features as the CL-MD3452, except the chipset adds a built-in PC Card interface and uses DSP and SAFE chips that are 3.3 V instead of 5 V. The PC Card interface has 16C450/16C550-compatible registers. This chipset does not support parallel ISA bus and serial RS-232 host interfaces.
4	CL-MD3462T	Same features as the CL-MD3452, except the chipset adds DSVD (Digital Simultaneous Voice And Data) and uses DSP and SAFE chips that are 3.3 V instead of 5 V.
	CL-MD3463T	Same features as the CL-MD3462T, except the chipset adds a built-in PC Card interface that has 16C450/16C550-compatible registers. This chipset does not support parallel ISA bus and serial RS-232 host interfaces.

11. DAA AND TELEPHONY INTERFACE DESIGN NOTES

DAA components and telephone interfaces are essential parts of modem designs. The following circuits and text are important to consider while designing a modem.

11.1 Data Access Arrangement (DAA) Design

11.1.1 General Overview

The DAA (Data Access Arrangement) is the link between the communication equipment and the PSTN (Public Switched Telephone Network). The DAA must perform four basic functions:

1) Provide a path for DC loop current.
2) Provide an AC signal path.
3) Protect the telephone network and the user.
4) Detect ring signals.

All of these functions must be performed within the framework of the Code of Federal Regulations, Title 47, Part 15 and Part 68, to obtain the FCC certification required to sell a product in the United States. Other countries have their corresponding requirements. Communications products that are intended for a country other than the United States or for the international market (several different countries) must have DAAs designed to meet the requirements of each country in which they will be sold.

The four DAA functions cannot be entirely separated because of the interdependence of requirements. For example: Due to the interdependence of requirements, the AC signal path usually includes a transformer. The transient protection circuitry is limited since it must pass the 150-V_{rms} 'ring' signal, which 'rides' on the 48V Central-Office battery voltage. Because of the 1500V isolation 'barrier' that is required between tip and ring (the PSTN) and the 'equipment,' the DAA can be divided into the line (PSTN) side and the equipment side. Any device that crosses this barrier such as transformers, opto-isolators, solid-state switches, relays and the PC board must maintain the proper 1500V isolation between the PSTN and the equipment.

The following sections provide several design examples and discussion of their design. First, the design of the protective circuitry is discussed. Next, the DC loop current and AC signal current paths are examined. And finally, several ring-detect circuits are illustrated. These sections are tailored to:

- Inform the modem designer about FCC requirements, which must be met by a certifiable design.
- Help develop a design approach.
- Provide usable design examples and parts lists.

11.2 Fault Protection

There are two types of fault protection:

- Components such as the transformer, relays, opto-isolator, and RJ-11 jack are designed to operate under normal circuit conditions and withstand the specified fault conditions without sustaining damage or exposing the user to dangerous voltages.
- Other components such as the MOV (metal-oxide varistor) are designed to remain passive until a fault condition occurs. The MOV is designed to protect the rest of the circuitry and its enclosing system from any harmful effects of the fault. The MOV might become damaged or destroyed in the process.

There are two dangerous fault conditions that can occur on the phone lines:

- The first is a lightning strike on or near a phone line. This can result in a large transient voltage between Tip and Ring, or between Tip and Ring and ground.
- Telephone lines are often strung on power poles underneath power lines. Occurrences such as bad weather, automobile accidents, or earthquakes could cause the power lines to break and make contact with the phone lines, thus exposing telephone users to the second dangerous fault condition.

The Code of Federal Regulations Title 47, Part 68.302, specifies the following transient and leakage tests to simulate these potentially dangerous fault conditions:

11.2.1 Metallic Voltage Surge Test

The metallic voltage surge test specifies an 800-V, 10/560-μs pulse (of each polarity) current limited to no less than 100 A, to be applied between Tip and Ring. Protection against this fault is provided by the isolation of the transformer, relays, opto-isolator, and the RJ-11 jack, and the clamping action of the metal-oxide varistor.

11.2.2 Longitudinal Voltage Surge Test

The specification for the longitudinal surge waveform is a 1500-V peak surge current (of each polarity) limited to not less than 200 A, with a maximum rise time-to-crest of 10 μs and a minimum decay time-to-half crest of 160 μs (for a 1500-V, 10/160-μs pulse). This surge is applied between Tip and Ring, connected to each other and grounded.

11.2.3 Leakage Test

For this test, a 1000-V_{rms} 60-Hz voltage is applied between Tip and Ring, connected to each other and grounded. This voltage is gradually increased from zero to full value over a 30-second period, then applied continuously for 60 seconds. During this test the current drawn from the source may not exceed 10 mA at any time.

After the surge and leakage tests, the modem should still meet the on-hook impedance limitations in the Code of Federal Regulations, Title 47, Part 68.312.

11.3 Radiated- and Conducted-Emissions Suppression

Radiated-emissions refers to the electromagnetic energy lost by radiation from the modem/computer combination and the necessary interconnection wiring, such as the modular lines connecting the modem to the wall jack and to the local telephone. Conducted-emissions refers to energy lost from the modem by conduction on the phone line or power lines.

The Code of Federal Regulations, Title 47, Part 15, places stringent limitations on the emission of radiation from electronic devices. Equipment for this purpose are divided into two broad categories: intentional radiators and unintentional radiators. This modem is considered an unintentional radiator since the radio frequency energy is generated from processing data and is not intended to be broadcast.

There are two problems associated with minimizing conducted and radiated energy:

- First, it is important not to generate any unnecessary radio energy. This is accomplished by keeping lead lengths short and as direct as possible. This minimizes ringing, the lengths of any potential antennas, and the capacitive and transformer coupling of unwanted signals outside the computer enclosure.
- Second, any radio frequency energy necessary for the modem to function or other radiation generated within the computer must be contained. The computer enclosure itself serves as a containment device. Also, the

bracket must be securely connected to both the PC board ground and the computer chassis. L_6–L_8 and L_{12} are intended to block and dissipate unwanted high-frequency signals, thus preventing them from radiating from the modular line connecting the modem to the wall jack, the local phone, the cable connector, or the external speaker. The computer power supply is relied upon to block any radiation appearing on the power lines in the modem.

11.4 Ring Detection

The ring signal for a 'B-type' ringer consists of a 15.3–68.0-Hz, 40–150-V_{rms} sine wave between Tip and Ring. This signal is on for 2 seconds and off for 4 seconds. The ring signal on/off pattern (cadence) repeats until the line is answered or the caller hangs up. This signal is applied between R_1 and C_1, as illustrated in Figure 11-1. On the positive half-cycle (R_1 positive with respect to C_1), D_1 is forward-biased, D_2 breaks down at 18 V, and D_3 is forward-biased. The LED in U_1 is reverse-biased and therefore does not conduct. On the negative half-cycle (R_1 negative with respect to C_1), D_3 is reverse-biased, D_2 is forward-biased, and D_1 breaks down at 18 V. Since D_3 is reverse-biased, the LED in U_1 is forward-biased and provides base current to the opto-isolator transistor. This causes RING* to go to the low or logic '0' state. R_2 serves as a pull-up for RING*. The signal at RING* is approximately a 0–5-V square wave (the saturation voltage of the opto-isolator transistor is approximately 0.2 V) at the ring signal frequency, as illustrated in Figure 11-2 on page 110.

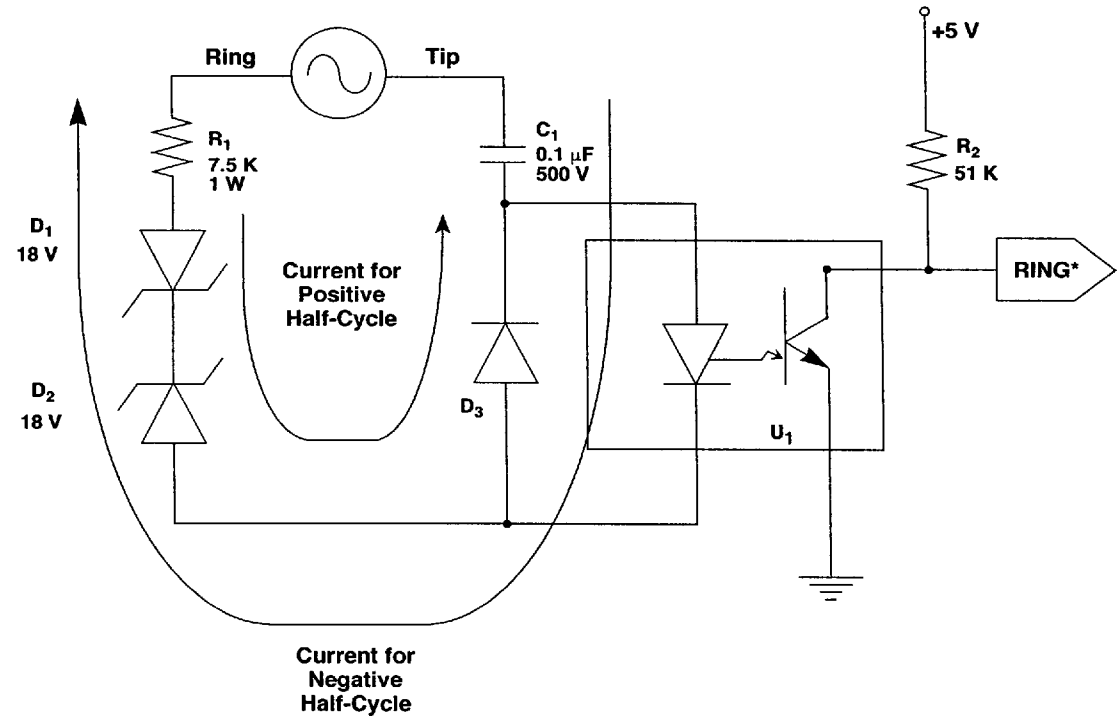

Figure 11-1. Ring Circuit

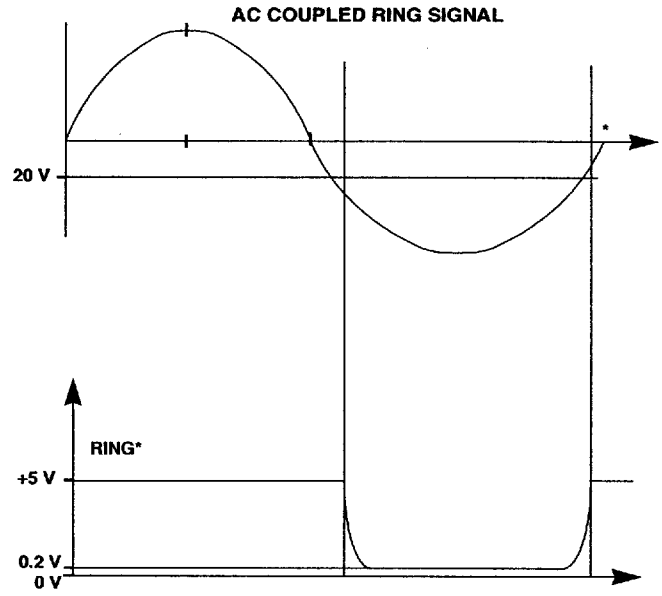

Figure 11-2. AC-Coupled Ring Signal and Ring*

11.5 Special Features and Functions

11.5.1 Caller ID

Caller ID is a service that allows the called party to know the number of the party calling before the call is answered. The information transmitted to the called party via caller ID includes the call date, the call time and the calling number. This service is not available everywhere due to Central-Office telephone equipment limitations and legal prohibition in some locations. The subscriber will have to invest in special equipment to receive the Caller ID message sent by the Central Office.

Caller-ID data is sent as Frequency Shift Keying (FSK) data between the first and second ring burst. Since the called party does not want to answer the call until the caller has been identified, the data must be made available to the modem (or other device) without the modem going to the off-hook state. In other words, no DC loop current can be drawn until the called party chooses to answer the call. For this reason, tip and ring must be capacitively coupled to the modem during the interval between the first and second ring burst so the modem can decode the Caller-ID signal without going off-hook.

A simplified circuit for implementing Caller ID is shown in Figure 11-3 on page 111. It functions as follows: After the first ring burst is decoded by the modem, the CIDREL* output is asserted low. This closes K_2, AC coupling tip to the transformer through C. The Caller-ID data is presented to the modem, no DC current

flows and the line remains in the on-hook (unanswered) condition. First, a 250-µs burst of 600-Hz carrier is sent by the Central Office followed by a 150-µs burst of 1200-Hz carrier to prepare the modem to receive the Caller-ID data. The 21 data words that comprise the Caller-ID message are transmitted according to the timing illustrated in Figure 11-4, and in the order shown in Table 11–1 on page 112. Each word consists of a start bit, eight data bits and a stop bit. The data must be received and K_2 opened prior to the start of the second ring burst. This is necessary to prevent the large-amplitude ring burst from being applied to the modem's receiver input. Once the data is received, it must be decoded and displayed for the called party to review. If the called party chooses to answer, K_1 closes, DC loop current flows and the line goes to the off-hook state.

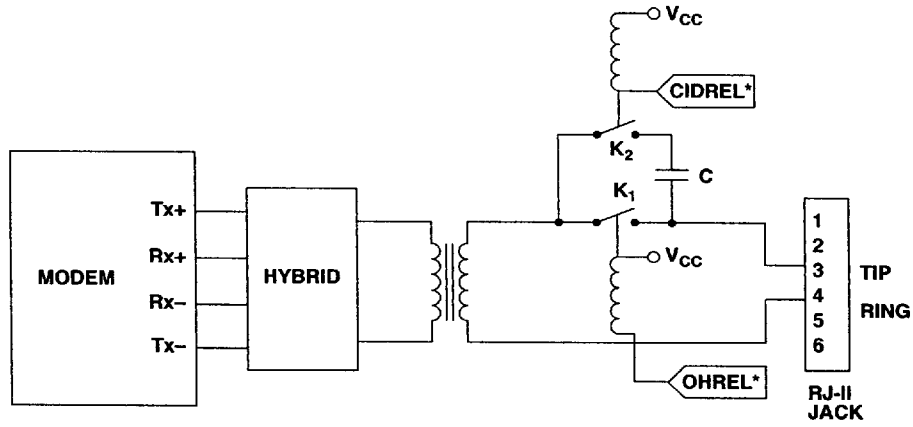

Figure 11-3. Caller ID Interface

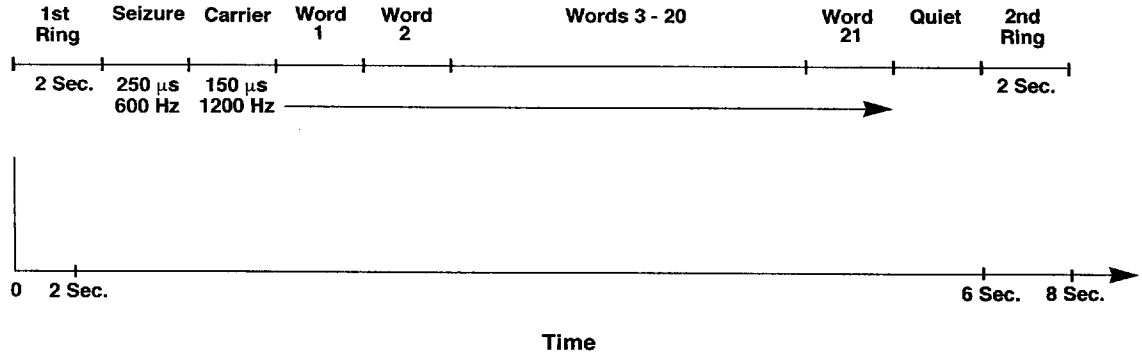

Figure 11-4. Caller ID Signal Timing

Table 11–1. Caller ID Message Transmission Order

Word Number	Word Description			Data Received 7	6	5	4	3	2	1	0
1	Message type — CND			0	0	0	0	0	1	0	0
2	Data words to follow — 18			0	0	0	1	0	0	1	0
3	Call Date	Month	0	0	0	0	0	0	0	0	0
4			2	0	0	0	0	0	0	1	0
5		Day	1	0	0	0	0	0	0	0	1
6			5	0	0	0	0	0	1	0	1
7	Call Time	Hour	1	0	0	0	0	0	0	0	1
8			0	0	0	0	0	0	0	0	0
9		Minute	1	0	0	0	0	0	0	0	1
10			5	0	0	0	0	0	1	0	1
11	Calling Number	Area Code	4	0	0	0	0	0	1	0	0
12			0	0	0	0	0	0	0	0	0
13			8	0	0	0	0	1	0	0	0
14		Number	9	0	0	0	0	1	0	0	1
15			4	0	0	0	0	0	1	0	0
16			5	0	0	0	0	0	1	0	1
17			8	0	0	0	0	1	0	0	0
18			3	0	0	0	0	0	0	1	1
19			0	0	0	0	0	0	0	0	0
20			0	0	0	0	0	0	0	0	0
			0								
21	Checksum			0	1	0	0	1	1	1	0

Several potentially useful options are possible in conjunction with Caller ID. The modem, computer and application software can be configured to maintain a running log of numbers calling the modem and indicate whether or not the call was completed, whether or not a message was left and how many times the phone rang. This information could be useful to determine peak hours of phone traffic, estimating staff efficiency, determining the desirability of an 800 number or allowing missed calls to be answered. The computer could be set up to screen calls. The ringer could be deactivated if an incoming call is not on the approved list. For example, if an important call was expected from a client, all other calls could be screened.

11.6 Voice Interface

There are several methods to provide a voice interface to Cirrus Logic data/fax/voice modems. Many of these impact the DAA design. This section will present several alternative voice interfaces. These will include interfacing a handset/headset with a CL-MD1624 (no microphone input), a CL-MD1724 (which includes a microphone input), interfacing the 'local' telephone and options for 'telephone emulation.' Remote voice interface using either the CL-MD1624 or the CL-MD1724 (recording and playing back voice messages from a remote phone) requires no circuitry in addition to the normal circuitry required for data/fax operation. Messages can always be played back through the speaker. The only pinout difference

between the CL-MD1624 and the CL-MD1724 (in a VQFP package) is the availability of microphone inputs on pins 9 and 10 on the CL-MD1724. These pins are grounds on the CL-MD1624. The microphone pins on the CL-MD1724 can be connected directly to ground. This makes the CL-MD1724 a direct pin-for-pin replacement for the CL-MD1624.

11.6.1 Local Phone Voice Interface

As illustrated in Figure 11-5, the local phone is biased when the modem is in the Local Voice mode. Current flows from the computer's +12V power supply, through the filter network consisting of L_3, R_{15}, C_{19}, and C_{20}, K_2 to the phone, T_1 and K_1 to ground. Most phones tested, including speakerphones, will function with a bias current of approximately 40 mA. At this current, 7-8V will appear across the phone. The filter component values were chosen empirically to minimize the audible noise due to the electrical noise on the computer's +12V power supply.

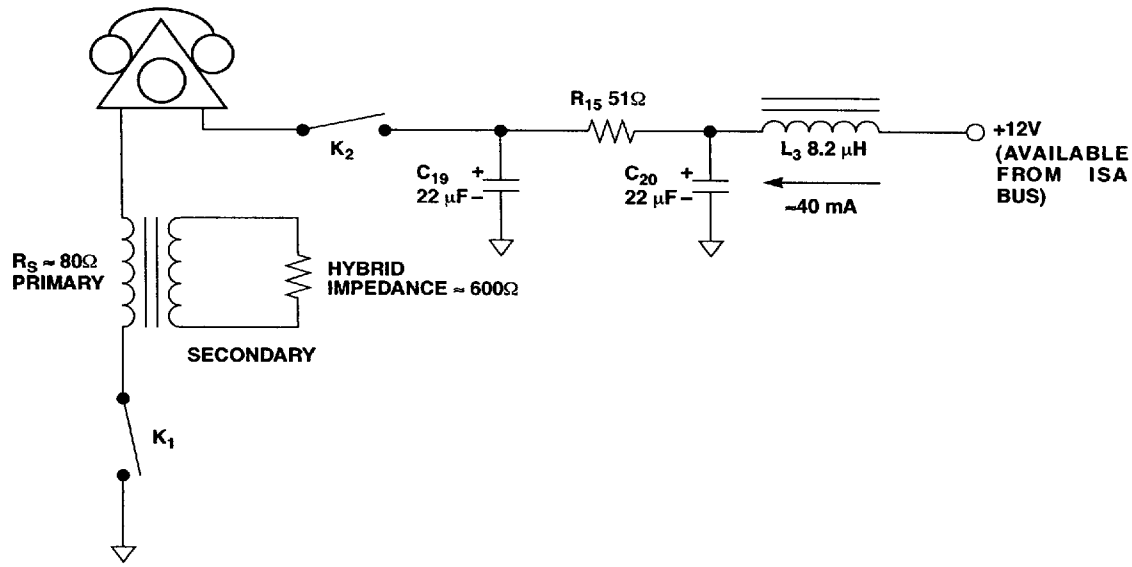

Figure 11-5. Local Phone in Voice Mode

Mechanical relays are required in this application because the local phone and the primary side of the transformer are being switched between tip and ring and the +12V and ground of the computer. 1500V of isolation must be maintained between the computer ground (and +12V) to pass the FCC Part 68 leakage test. The relay chosen for this application, therefore, must have a minimum contact-to-contact breakdown of 1500V. This requirement precludes the use of solid-state relays. Solid-state relays can be used in line-side applications only when switching tip and ring. In this case, the 1500V appears as a common mode voltage simultaneously on both sides of the switch. The high-voltage isolation is then between both switch contacts and the LED, which is the mode in which solid-state relays were intended to be used. Figure 11-6 illustrates a complete application for biasing the local phone for voice record and playback.

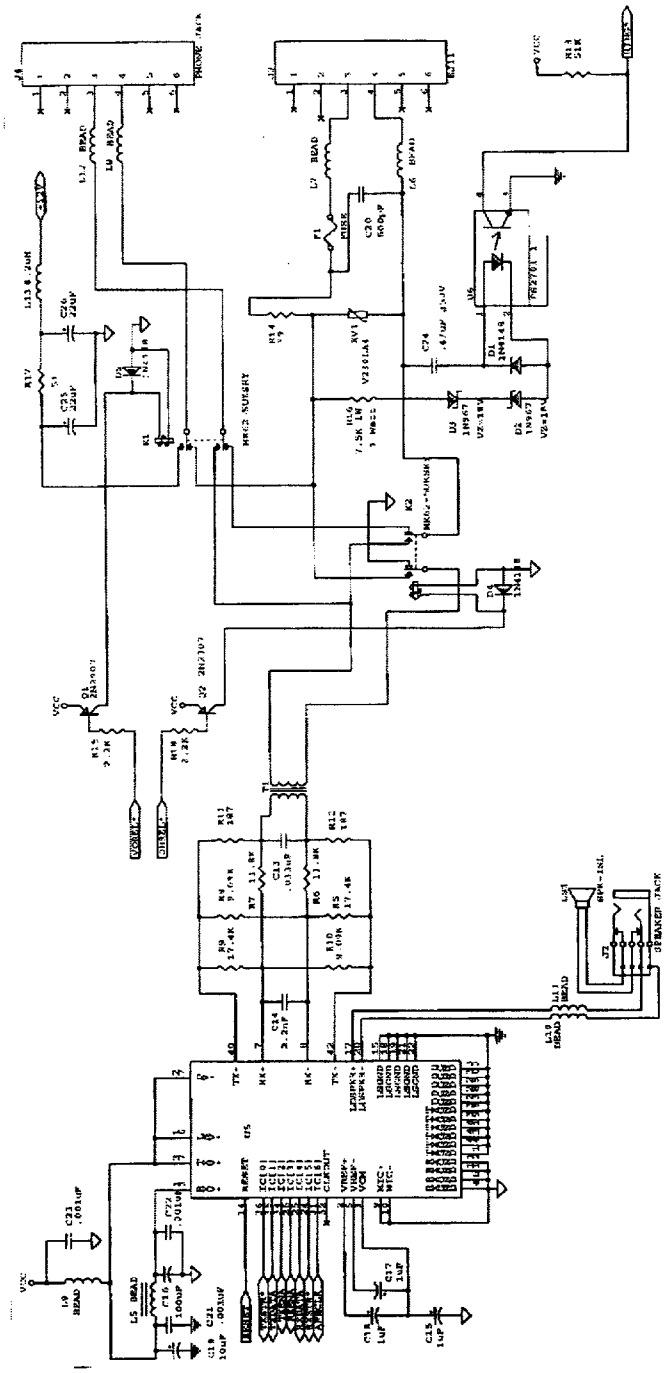

Figure 10-1. Complete Local Phone Voice Application — 'Wet' DAA

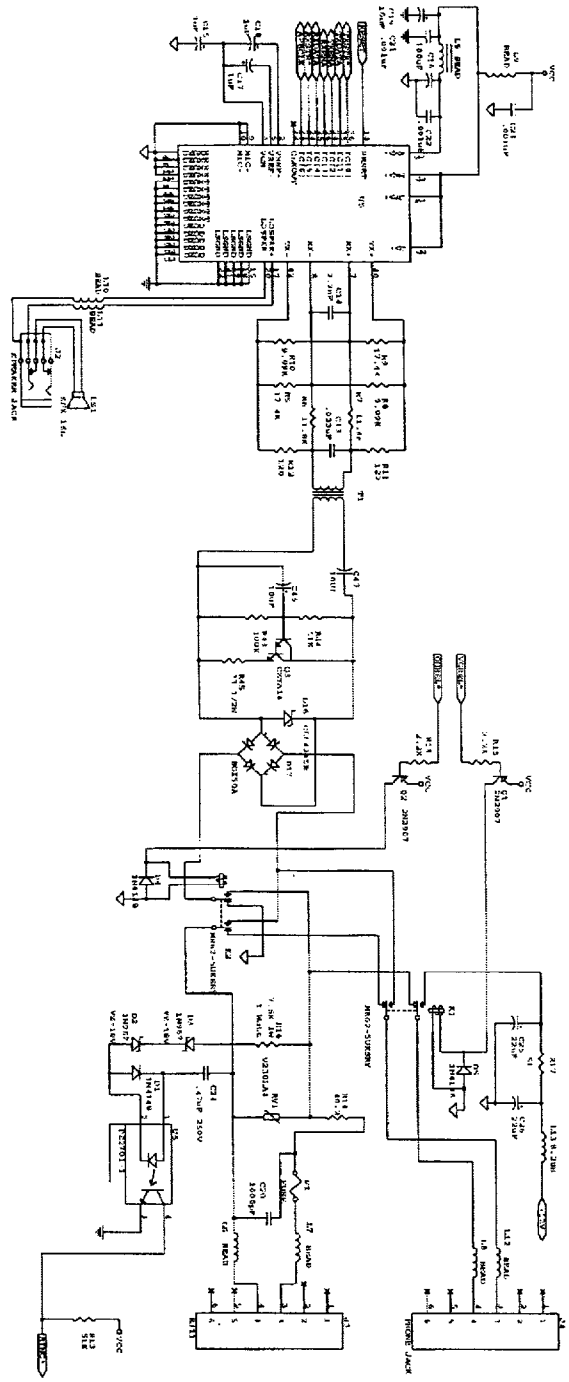

Figure 10-2. Complete Local Phone Voice Application — 'Dry' DAA

Notes

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12. V.34+ REFERENCE DESIGNS

This section provides reference schematics for the design of ISA, serial, and PC Card interfaces. Follow the steps shown below to select the attached schematics for the desired interface and feature set.

IMPORTANT: Schematics may change at any time. Contact the PC Telephony Applications Group at Cirrus Logic for current schematics.

12.1 Step 1

Select the desired interface. Find the names of the appropriate schematics from the following table:

Table 12-1. Interface Schematics

INTERFACE		
ISA	**Serial (RS-232)**	**PC Card (PCMCIA)**
ISA1.SCH ISA2.SCH ISA3.SCH	SER1.SCH SER2.SCH SER3.SCH	PCM1.SCH PCM2.SCH PCM3.SCH

12.2 Step 2

Refer to the table "Feature Sets" on the following page, which lists all the modes of operation that the CL-MD34XX chipsets support and some common feature sets that seemed attractive to us. If you desire a different combination of features, please contact the Applications Engineering Group at Cirrus Logic.

Select the feature set desired (for example, 1, 2, 3, 4, or 5). Use the appropriate schematics, according to the following table:

Table 12-2. Feature Set Schematics

Feature Set 1	Feature Set 2	Feature Set 3	Feature Set 4	Feature Set 5
AFE1.SCH DAA1.SCH	AFE2&3.SCH DAA2&4.SCH MICSP2&3.SCH	AFE2&3.SCH DAA3&5.SCH MICSP2&3.SCH	AFE4.SCH DAA2&4.SCH MICSP4&5.SCH	AFE5.SCH DAA3&5.SCH MICSP4&5.SCH

IMPORTANT: For PC Card interfaces, all AFEs should be of the 3.3-V CL-MD1724T type to achieve compatibility with the board's 3.3-V DSP.

Table 12-3. Feature Sets

#	Mode	Feature Sets				
		1	2	3	4	5
1	Data/Fax	✔	✔	✔	✔	✔
2	Voice		✔	✔	✔	✔
3	TAD — Local phone			✔		✔
4	TAD — MIC & SPKR		✔	✔	✔	✔
5	TAD — Headset		✔	✔	✔	✔
6	Telephone Emulation		✔	✔	✔	✔
7	CID		✔			
8	VoiceView™ Local Phone		✔	✔	✔	✔
The following modes need two AFEs						
9	VoiceView™ Speakerphone				✔	✔
10	VoiceView™ Headset				✔	✔
11	DSVD Local phone					✔
12	DSVD Speakerphone				✔	✔
13	DSVD Headset				✔	✔
14	Speakerphone				✔	✔

TAD: Telephone Answering Device
MIC: Microphone
CID: Caller ID